QLogic Corporation

ISP1040C Intelligent SCSI Processor

Data Sheet

Features

- *PCI Local Bus Specification* revision 2.1 compliant
- Compliance with ANSI SCSI standard X3.131-1994
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI X3T10/1071D Fast-20 standard
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.0 (PC97)
- Onboard RISC processor to execute operations at the I/O control block level from the host memory
- Supports fast, wide, and Ultra (Fast-20) SCSI data transfer rates
- SCSI initiator and target modes of operation
- 32-bit, intelligent bus master, DMA PCI bus interface
- Supports PCI dual-address cycle (64-bit addressing)
- SCSI operations executed from start to finish without host intervention
- Simultaneous, multiple logical threads
- JTAG boundary scan support

Product Description

The ISP1040C is a single-chip, highly integrated, bus master, SCSI I/O processor for use in SCSI initiator-type applications. The device interfaces the PCI bus to a wide, Ultra SCSI bus and contains an onboard RISC processor. The ISP1040C is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from initiation to completion without host CPU intervention. The ISP1040C provides power management feature support in accordance with the *PCI Bus Power Management Specification* while retaining full pin compatibility with the QLogic ISP1040B. The ISP1040C block diagram is illustrated in figure 1.

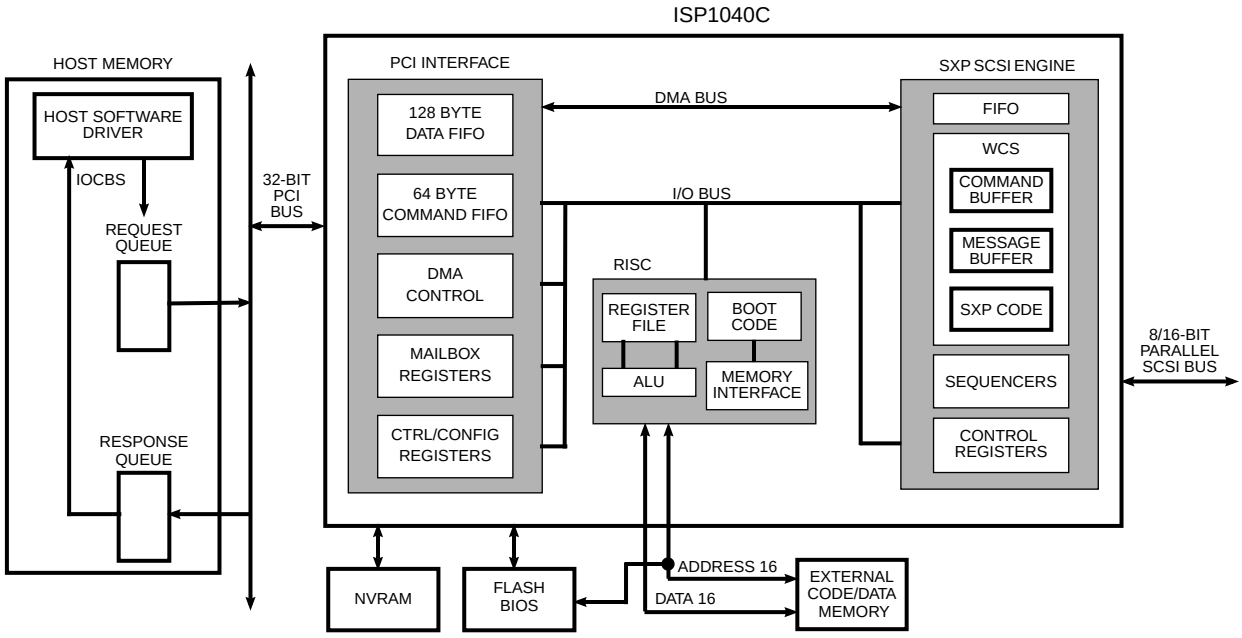

Figure 1. ISP1040C Block Diagram

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ISP Initiator and Target Firmware

The ISP1040C firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The ISP1040C firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery. The multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP1040C switches dynamically between initiator and target modes.

Software Drivers

BIOS firmware is available for the ISP1040C. Software drivers are available for the following operating systems:

- AIX
- I_2O
- DOS/Windows
- Novell NetWare
- OS/2
- SCO UNIX
- UnixWare
- Windows 95
- Windows NT

I/O Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1040C incorporates a high-speed, proprietary RISC processor; an intelligent SCSI bus controller (SCSI executive processor [SXP]); and a host bus, dual-channel DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under control of the onboard RISC processor for maximum system performance. The ISP1040C RISC interface requires external program data memory.

The complete I/O subsystem solution using the ISP1040C and associated supporting memory devices is shown in figure 2.

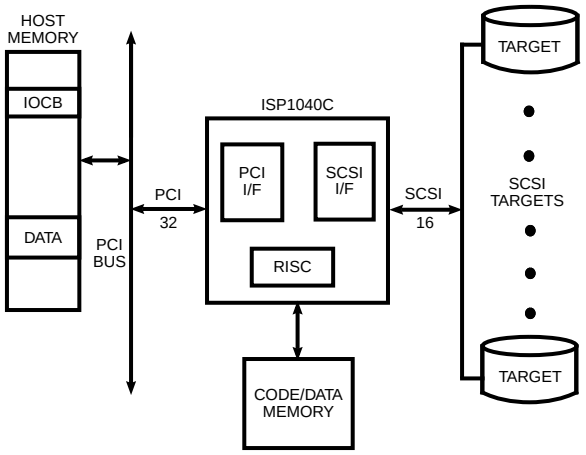

Figure 2. I/O Subsystem Design Using the ISP1040C

Interfaces

The ISP1040C supports the following interfaces:

- PCI bus
- RISC processor
- SCSI executive processor

Pins that support these interfaces and other chip operations are shown in figure 3.

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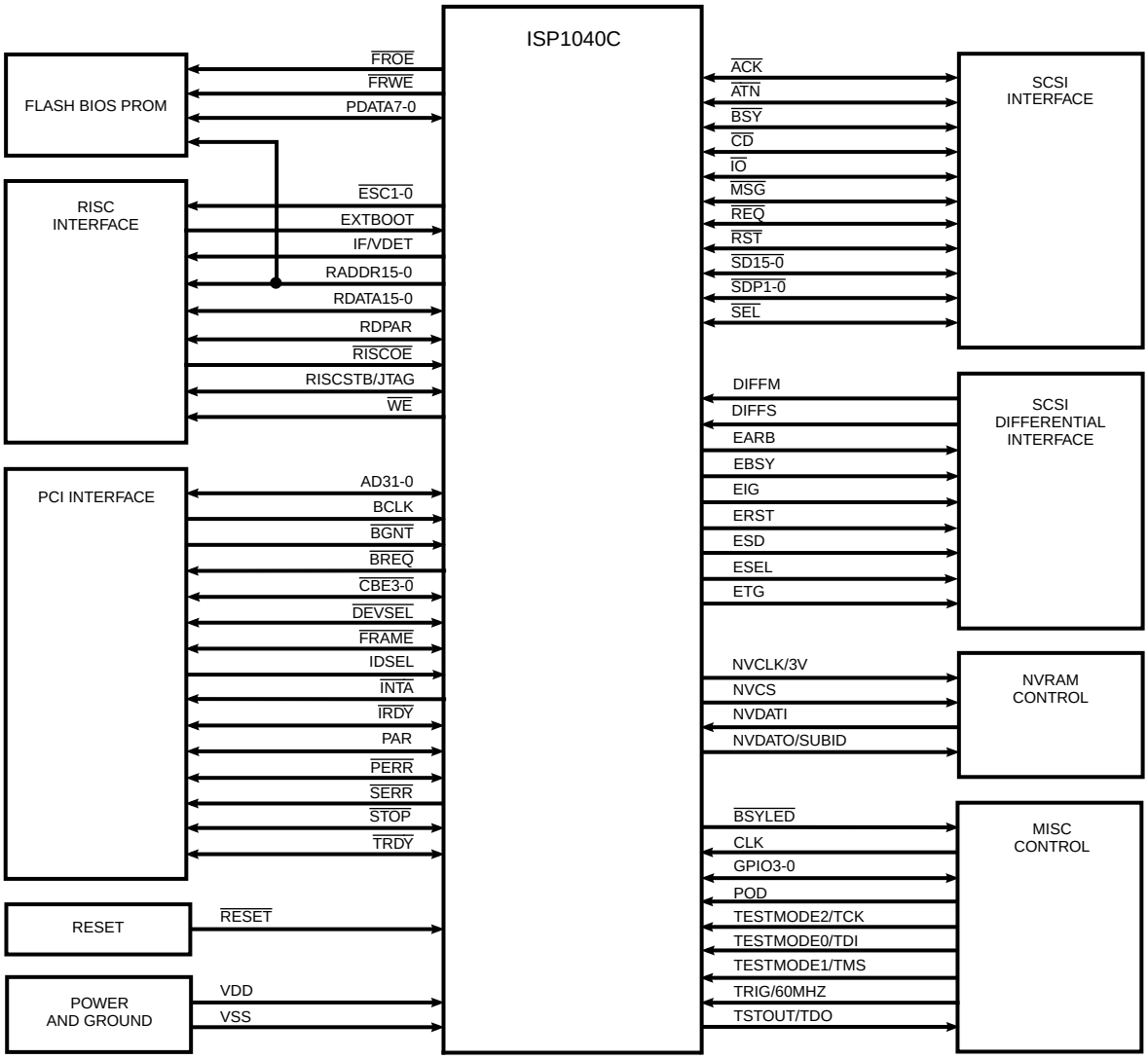

Figure 3. ISP1040C Functional Signal Grouping

PCI Bus Interface

The ISP1040C PCI bus interface supports the following:

- 32-bit, intelligent bus master, burst DMA host interface for fetching I/O control blocks and data transfers
- 16-bit slave mode for communication with host
- Two channel DMA controller
- 128-byte data DMA FIFO and 64-byte command DMA FIFO with threshold control
- Pipelined DMA registers for efficient scatter/gather operations
- Support for subsystem ID
- Supports PCI dual-address cycle (64-bit addressing)
- Support for PCI cache commands
- 3.3 V and 5.0 V tolerant PCI I/O buffers
- Support for flash BIOS PROM

The ISP1040C is designed to interface directly to the PCI local bus and operate as a 32-bit DMA master. This function is accomplished through the PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI bus control signals, generates host memory addresses, and facilitates data transfers between host memory and the onboard DMA FIFO. The PBIU also allows the host to access the ISP1040C internal registers and communicate with the onboard RISC processor through the PCI bus target mode operation.

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The ISP1040C onboard DMA controller consists of two independent DMA channels that initiate transactions on the PCI bus and transfer data between the memory and DMA FIFO. The two DMA channels are the command DMA channel and the data DMA channel. The command DMA channel is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channel transfers data between the SCSI bus and the PCI bus.

The PBIU internally arbitrates between the data DMA channel and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

RISC Processor Interface

The ISP1040C RISC processor interface supports the following:

- Programmable cycle time for external memory access
- Internal 16-bit wide data paths
- Execution of multiple I/O control blocks from the host memory
- Management of onboard host bus DMA controller and SCSI bus controller
- Reduced host intervention and interrupt overhead
- Capacity to generate one interrupt per I/O operation

The onboard RISC processor enables the ISP1040C to handle complete I/O transactions with no intervention from the host. The ISP1040C RISC processor controls the chip interfaces; executes simultaneous, multiple input/output control blocks (IOCBs); and maintains the required thread information for each transfer.

SCSI Executive Processor Interface

The ISP1040C SXP interface supports the following:

- 8- or 16-bit data transfers
- Ultra SCSI (Fast-20) synchronous data transfer rates up to 40 Mbytes/sec
- Asynchronous SCSI data transfer rates up to 12 Mbytes/sec
- Programmable SCSI processor
  - Specialized instruction set with 16-bit microword
  - 384-bit by 16-bit internal RAM control store
- 32-bit, configurable SCSI transfer counter
- Command, status, message in, and message out buffers
- Device information storage area
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Programmable active negation

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

Packaging

The ISP1040C is available in a 208-pin plastic quad flat pack (PQFP).

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