National Semiconductor

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# PC87338/PC97338
# ACPI 1.0 and PC98/99 Compliant SuperI/O

## General Description

The PC97338 is a fully ACPI 1.0 and PC98/99 compliant, ISA based Super I/O. It is functionally compatible with the PC87338. It includes a Floppy Disk Controller (FDC), two Serial Communication Controllers (SCC) for UART and Infrared support, one IEEE1284 compatible Parallel Port, and two general purpose Chip Select signals for game port support. The device supports power management as well as 3.3V and 5V mixed operation making it particularly suitable for notebook and sub-notebook applications.

The PC87338 and PC97338 are fully compliant to the Plug and Play specifications included in the "Hardware Design Guide for Microsoft Windows 95".

Differences between the PC87338 and PC97338 are indicated in italics. These differences are summarized in Appendix A.

## Features

- Meets ACPI 1.0 and PC98/99 requirements
- Backward compatible with PC87338
- 100% compatibility with Plug and Play requirements specified in the "*Hardware Design Guide for Microsoft Windows 95*", ISA, EISA, and MicroChannel architectures
- A special Plug and Play module includes:
  - Flexible IRQs, DMAs and base addresses
  - General Interrupt Requests (IRQs) that can be multiplexed to the ten supported IRQs

## Block Diagram

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- A new, high performance, on-chip Floppy Disk Controller (FDC) provides:
  - Software compatibility with the PC8477, which contains a superset of the floppy disk controller functions in the µDP8473, the NEC µPD765A and the N82077
  - A modifiable 13-bit address
  - Ten IRQ channel options
  - Four 8-bit DMA channel options
  - 16-byte FIFO
  - Burst and non-burst modes
  - Low-power CMOS with enhanced power-down mode
  - A new, high-performance, on-chip, digital data separator without external filter components
  - Support for 5.25"/3.5" floppy disk drives
  - Automatic media sense support
  - Perpendicular recording drive support
  - Three mode Floppy Disk Drive (FDD) support
  - Full support for IBM's Tape Drive Register (TDR) implementation
  - Support for new fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
  - Support for both *FM* and MFM modes.
- Two Serial Communication Controllers provide:
  - Software compatibility with the 16550A and the 16450
  - A modifiable 13-bit address
  - Ten IRQ channel options
  - MIDI baud rate support
  - Four 8-bit DMA channel options on SCC2
  - Shadow register support UART write-only bits
- A fast universal Infrared interface on SCC2 supports the following:
  - Data rates of up to 115.2 Kbps (SIR)
  - A data rate of 1.152 Mbps (MIR)
  - A data rate of 4.0 Mbps (FIR)
  - Selectable internal or external modulation/demodulation (Sharp-IR)
  - Consumer Electronic IR mode
- A bidirectional parallel port that includes:
  - A modifiable 13-bit address
  - Ten IRQ channel options
  - Four 8-bit DMA channel options
  - An Enhanced Parallel Port (EPP) compatible with version EPP 1.9 (IEEE1284 compliant), that also supports version EPP 1.7 of the Xircom specification.
  - An Extended Capabilities Port (ECP) that is IEEE1284 compliant, including level 2
  - Bidirectional data transfer under either software or hardware control
  - Compatibility with ISA, EISA, and MicroChannel parallel ports
  - Multiplexing of additional external FDC signals on parallel port pins that enables use of an external Floppy Disk Drive (FDD)
  - A protection circuit that prevents damage to the parallel port when an external printer powers up or operates at high voltages
  - 14 mA output drivers
- Two general purpose pins for two programmable chip select signals can be programmed for game port control.
- An address decoder that:
  - Selects all primary and secondary ISA addresses, including COM1-4 and LPT1-3
  - Decodes up to 16 address bits
- Clock source:
  - An internal clock multiplier generates all required internal frequencies.
  - A clock input source 14.318 MHz, 24 MHz, or 48 MHz may be selected
- Enhanced power management features:
  - Special power-down configuration registers
  - Enhanced programmable FDC command to trigger power down
  - Programmable power-down and wake-up modes
  - Two dedicated pins for FDC power management
  - Low power-down current consumption (typically for PC97338, 400 µA for 3.3V and 600 µA for 5V application)
  - Reduced pin leakage current
  - Low power CMOS technology
  - The ability to shut off clocks to either the entire chip or only to specific modules
- Mixed voltage support provides:
  - Standard 5 V operation
  - Low voltage 3.3 V operation
  - Simultaneous internal 3.3 V operation and reception or transmission to devices that have either 3.3 V or 5 V power supply
- 100-pin TQFP VJG package - PC87338/PC97338
- 100-pin PQFP VLJ package - PC87338/PC97338

## Basic Configuration

## Basic Configuration

# Table of Contents


## 1.0 Pin Descriptions

1.1 CONNECTION DIAGRAMS ..... 18

1.2 SIGNAL/PIN DESCRIPTIONS ..... 22

## 2.0 Configuration

2.1 OVERVIEW ..... 36

2.2 CONFIGURATION REGISTER SETUP ..... 36

2.2.1 Hardware Device Configuration ..... 36

2.2.2 Software Device Configuration ..... 38

2.2.3 Updating Configuration Registers ..... 38

2.2.4 Reserved Bits in Configuration Registers ..... 38

2.2.5 INDEX and DATA Register Locations ..... 38

2.2.6 Plug and Play Protocol ..... 39

2.3 THE CONFIGURATION REGISTERS ..... 40

2.3.1 Configuration Register Bitmaps ..... 41

2.3.2 Function Enable Register (FER), Index 00h ..... 45

2.3.3 Function Address Register (FAR), Index 01h ..... 47

2.3.4 Power and Test Register (PTR), Index 02h ..... 47

2.3.5 Function Control Register (FCR), Index 03h ..... 48

2.3.6 Printer Control Register (PCR), Index 04h ..... 49

2.3.7 Power Management Control Register (PMC), Index 06h ..... 50

2.3.8 Tape, SCCs and Parallel Port Configuration Register (TUP), Index 07h ..... 51

2.3.9 SuperI/O Chip Identification Register (SID), Index 08h ..... 52

2.3.10 Advanced SuperI/O Chip Configuration Register (ASC), Index 09h ..... 52

2.3.11 Chip Select 0 Low Address Register (CS0LA), Index 0Ah ..... 53

2.3.12 Chip Select 0 Configuration Register (CS0CF), Index 0Bh ..... 53

2.3.13 Chip Select 1 Low Address Register (CS1LA), Index 0Ch ..... 54

2.3.14 Chip Select 1 Configuration Register (CS1CF), Index 0Dh ..... 54

2.3.15 Chip Select 0 High Address Register (CS0HA), Index 10h ..... 55

2.3.16 Chip Select 1 High Address Register (CS1HA), Index 11h ..... 55

2.3.17 SuperI/O Chip Configuration Register 0 (SCF0), Index 12h ..... 55

2.3.18 SuperI/O Chip Configuration Register 1 (SCF1), Index 18h ..... 56

2.3.19 Plug and Play Configuration 0 Register (PNP0), Index 1Bh ..... 57

2.3.20 Plug and Play Configuration 1 Register (PNP1), Index 1Ch ..... 58

2.3.21 SuperI/O Chip Configuration Register 2 (SCF2), Index 40h ..... 58

2.3.22 Plug and Play Configuration 2 Register (PNP2), Index 41h ..... 59

2.3.23 Parallel Port Base Address Low Byte Register (PBAL), Index 42h ..... 60

2.3.24 Parallel Port Base Address High Byte Register (PBAH), Index 43h ..... 60

2.3.25 SCC1 Base Address Low Byte Register (S1BAL), Index 44h ..... 61

2.3.26 SCC1 Base Address High Byte Register (S1BAH), Index 45h ..... 61

2.3.27 SCC2 Base Address Low Byte Register (S2BAL), Index 46h ..... 61

2.3.28 SCC2 Base Address High Byte Register (S2BAH), Index 47h ..... 62

2.3.29 FDC Base Address Low Byte Register (FBAL), Index 48h ..... 62

2.3.30 FDC Base Address High Byte Register (FBAH,) Index 49h ..... 62

2.3.31 SIO Base Address Low Byte Register (SBAL), Index 4Ah ..... 63
2.3.32 SIO Base Address High Byte Register (SBAH), Index 4Bh ..... 63
2.3.33 System IRQ Input 1 Configuration Register (SIRQ1), Index 4Ch ..... 63
2.3.34 System IRQ Input 2 Configuration Register (SIRQ2), Index 4Dh ..... 64
2.3.35 System IRQ Input 3 Configuration Register (SIRQ3), Index 4Eh ..... 65
2.3.36 Plug-and-Play Configuration 3 Register (PNP3), Index 4Fh ..... 66
2.3.37 SuperI/O Configuration 3 Register (SCF3), Index 50h ..... 67
2.3.38 Clock Control Register (CLK), Index 51h ..... 68
2.3.39 Manufacturing Test Register (MTEST), Index 52h ..... 68

## 3.0 The Digital Floppy Disk Controller (FDC)

3.1 FDC FUNCTIONS ..... 69
3.1.1 Microprocessor Interface ..... 69
3.1.2 System Operation Modes ..... 70
3.2 DATA TRANSFER ..... 70
3.2.1 Data Rates ..... 70
3.2.2 The Data Separator ..... 70
3.2.3 Perpendicular Recording Mode Support ..... 71
3.2.4 Data Rate Selection ..... 72
3.2.5 Write Precompensation ..... 72
3.2.6 FDC Low-Power Mode Logic ..... 73
3.2.7 Reset ..... 73
3.3 THE REGISTERS OF THE FDC ..... 74
3.3.1 FDC Register Bitmaps ..... 74
3.3.2 Status Register A (SRA), Offset 000 ..... 75
3.3.3 Status Register B (SRB), Offset 001 ..... 76
3.3.4 Digital Output Register (DOR), Offset 010 ..... 77
3.3.5 Tape Drive Register (TDR), Offset 011 ..... 79
3.3.6 Main Status Register (MSR), Offset 100 ..... 80
3.3.7 Data Rate Select Register (DSR), Offset 100 ..... 82
3.3.8 Data Register (FIFO), Offset 101 ..... 83
3.3.9 Digital Input Register (DIR), Offset 111 ..... 83
3.3.10 Configuration Control Register (CCR), Offset 111 ..... 84
3.4 THE PHASES OF FDC COMMANDS ..... 85
3.4.1 Command Phase ..... 85
3.4.2 Execution Phase ..... 85
3.4.3 Result Phase ..... 87
3.4.4 Idle Phase ..... 88
3.4.5 Drive Polling Phase ..... 88
3.5 THE RESULT PHASE STATUS REGISTERS ..... 88
3.5.1 Result Phase Status Register 0 (ST0) ..... 88
3.5.2 Result Phase Status Register 1 (ST1) ..... 89
3.5.3 Result Phase Status Register 2 (ST2) ..... 90
3.5.4 Result Phase Status Register 3 (ST3) ..... 91
3.6 THE FDC COMMAND SET ..... 91
3.6.1 Abbreviations Used in FDC Commands ..... 92

3.6.2 The CONFIGURE Command ..... 94
3.6.3 The DUMPREG Command ..... 95
3.6.4 The FORMAT TRACK Command ..... 96
3.6.5 The INVALID Command ..... 99
3.6.6 The LOCK Command ..... 100
3.6.7 The MODE Command ..... 100
3.6.8 The NSC Command ..... 103
3.6.9 The PERPENDICULAR MODE Command ..... 103
3.6.10 The READ DATA Command ..... 105
3.6.11 The READ DELETED DATA Command ..... 108
3.6.12 The READ ID Command ..... 109
3.6.13 The READ A TRACK Command ..... 110
3.6.14 The RECALIBRATE Command ..... 110
3.6.15 The RELATIVE SEEK Command ..... 111
3.6.16 The SCAN EQUAL, the SCAN LOW OR EQUAL and the SCAN HIGH OR EQUAL Commands ..... 112
3.6.17 The SEEK Command ..... 113
3.6.18 The SENSE DRIVE STATUS Command ..... 114
3.6.19 The SENSE INTERRUPT Command ..... 114
3.6.20 The SET TRACK Command ..... 115
3.6.21 The SPECIFY Command ..... 116
3.6.22 The VERIFY Command ..... 118
3.6.23 The VERSION Command ..... 119
3.6.24 The WRITE DATA Command ..... 120
3.6.25 The WRITE DELETED DATA Command ..... 121

3.7 EXAMPLE OF A FOUR-DRIVE CIRCUIT USING THE PC87338/PC97338 ..... 121

## 4.0 Parallel Port

4.1 INTRODUCTION ..... 123
4.1.1 The Chip Parallel Port Modes ..... 123
4.1.2 Device Configuration ..... 123

4.2 STANDARD PARALLEL PORT MODES ..... 123
4.2.1 Standard Parallel Port (SPP) Modes Register Set ..... 124
4.2.2 SPP Mode Parallel Port Register Bitmaps ..... 124
4.2.3 Data Register (DTR), Offset 0 ..... 124
4.2.4 Status Register (STR), Offset 1 ..... 125
4.2.5 Control Register (CTR), Offset 2 ..... 126

4.3 ENHANCED PARALLEL PORT (EPP) MODES ..... 127
4.3.1 Enhanced Parallel Port (EPP) Modes Register Set ..... 128
4.3.2 EPP Modes Parallel Port Register Bitmaps ..... 128
4.3.3 SPP or EPP Data Register (DTR), Offset 0 ..... 129
4.3.4 SPP or EPP Status Register (STR), Offset 1 ..... 129
4.3.5 SPP or EPP Control Register (CTR), Offset 2 ..... 129
4.3.6 EPP Address Register, Offset 3 ..... 130
4.3.7 EPP Data Port 0, Offset 4 ..... 130
4.3.8 EPP Data Port 1, Offset 5 ..... 130
4.3.9 EPP Data Port 2, Offset 6 ..... 130

4.3.10 EPP Data Port 3, Offset 7 ..... 131
4.3.11 EPP Mode Transfer Operations ..... 131
4.4 EXTENDED CAPABILITIES PARALLEL PORT (ECP) MODES ..... 133
4.4.1 Accessing the ECP Registers ..... 134
4.4.2 Software Operation in ECP Modes ..... 134
4.4.3 Hardware Operation in ECP Modes ..... 134
4.4.4 ECP Modes Parallel Port Register Bitmaps ..... 135
4.4.5 ECP Data Register (DATAR), Bits 7-5 of ECR = 000 or 001, Offset 000h ..... 136
4.4.6 ECP Address FIFO (AFIFO) Register, Bits 7-5 of ECR = 011, Offset 000h ..... 137
4.4.7 ECP Status Register (DSR), Offset 001h ..... 137
4.4.8 ECP Control Register (DCR), Offset 002h ..... 137
4.4.9 Parallel Port Data FIFO (CFIFO) Register, Bits 7-5 of ECR = 010, Offset 400h ..... 138
4.4.10 ECP Data FIFO (DFIFO) Register, Bits 7-5 of ECR = 011, Offset 400h ..... 138
4.4.11 Test FIFO (TFIFO) Register, Bits 7-5 of ECR = 110, Offset 400h ..... 139
4.4.12 Configuration Register A (CNFGA), Bits 7-5 of ECR = 111, Offset 400h ..... 139
4.4.13 Configuration Register B (CNFGB), Bits 7-5 of ECR = 111, Offset 401h ..... 139
4.4.14 Extended Control Register (ECR), Offset 402h ..... 140
4.5 ECP MODE DESCRIPTIONS ..... 142
4.5.1 Software Controlled Data Transfer (Modes 000 and 001) ..... 142
4.5.2 Automatic Data Transfer (Modes 010 and 011) ..... 142
4.5.3 FIFO Test Access (Mode 110) ..... 143
4.5.4 Configuration Registers Access (Mode 111) ..... 143
4.5.5 Interrupt Generation ..... 143
4.6 THE PARALLEL PORT MULTIPLEXER (PPM) ..... 144
4.7 PARALLEL PORT PIN/SIGNAL LIST ..... 144

## 5.0 Serial Communications Controllers (SCC1 and SCC2)

5.1 FEATURES ..... 146
5.2 FUNCTIONAL MODES OVERVIEW ..... 146
5.3 UART MODE ..... 146
5.4 SHARP-IR MODE ..... 147
5.5 IRDA 1.0 SIR MODE ..... 147
5.6 IRDA 1.1 MIR AND FIR MODES ..... 147
5.6.1 High Speed Infrared Transmit Operation ..... 148
5.6.2 High Speed Infrared Receive Operation ..... 149
5.7 CONSUMER ELECTRONIC IR (CEIR) MODE ..... 149
5.7.1 CEIR Transmit Operation ..... 149
5.7.2 CEIR Receive Operation ..... 150
5.8 FIFO TIME-OUTS ..... 150
5.9 TRANSMIT DEFERRAL ..... 151
5.10 AUTOMATIC FALLBACK TO 16550 COMPATIBILITY MODE ..... 151
5.11 PIPELINING ..... 152
5.12 OPTICAL TRANSCEIVER INTERFACE ..... 152

5.13 ARCHITECTURAL DESCRIPTION ..... 153
5.14 BANK 0 ..... 153
5.14.1 TXD/RXD – Transmit/Receive Data Ports ..... 153
5.14.2 IER – Interrupt Enable Register ..... 154
5.14.3 EIR/FCR – Event Identification/FIFO Control Registers ..... 154
5.14.4 LCR/BSR – Link Control/Bank Select Register ..... 157
5.14.5 MCR – Modem/Mode Control Register ..... 159
5.14.6 LSR – Link Status Register ..... 160
5.14.7 MSR – Modem Status Register ..... 162
5.14.8 SPR/ASCR – Scratchpad/Auxiliary Status and Control Register ..... 162
5.15 BANK 1 ..... 163
5.15.1 LBGD – Legacy Baud Generator Divisor Port ..... 164
5.15.2 LCR/BSR – Link Control/Bank Select Registers ..... 164
5.16 BANK 2 ..... 164
5.16.1 BGD – Baud Generator Divisor Port ..... 164
5.16.2 EXCR1 – Extended Control Register 1 ..... 166
5.16.3 LCR/BSR – Link Control/Bank Select Registers ..... 167
5.16.4 EXCR2 – Extended Control Register 2 ..... 167
5.16.5 TXFLV – TX_FIFO Level, Read-Only ..... 168
5.16.6 RXFLV – RX_FIFO Level, Read-Only ..... 168
5.17 BANK 3 ..... 168
5.17.1 MID – Module Identification Register, Read Only ..... 168
5.17.2 SH_LCR – Link Control Register Shadow, Read Only ..... 168
5.17.3 SH_FCR – FIFO Control Register Shadow, Read-Only ..... 168
5.17.4 LCR/BSR – Link Control/Bank Select Registers ..... 168
5.18 BANK 4 ..... 169
5.18.1 TMR – Timer Register ..... 169
5.18.2 IRCR1 – Infrared Control Register 1 ..... 169
5.18.3 LCR/BSR – Link Control/Bank Select Registers ..... 169
5.18.4 TFRL/TFRCC – Transmitter Frame-Length/Current-Count ..... 170
5.18.5 RFRML/RFRCC – Receiver Frame Maximum-Length/Current-Count ..... 170
5.19 BANK 5 ..... 170
5.19.1 P_BGD – Pipelined Baud Generator Divisor Register ..... 170
5.19.2 P_MDR – Pipelined Mode Register ..... 170
5.19.3 LCR/BSR – Link Control/Bank Select Registers ..... 171
5.19.4 IRCR2 – Infrared Control Register 2 ..... 171
5.19.5 ST_FIFO – Status FIFO ..... 172
5.20 BANK 6 ..... 173
5.20.1 IRCR3 – Infrared Control Register 3 ..... 173
5.20.2 MIRPW – MIR Pulse Width Register ..... 173
5.20.3 SIR_PW – SIR Pulse Width Register ..... 174
5.20.4 LCR/BSR – Link Control/Bank Select Registers ..... 174
5.20.5 BFPL – Beginning Flags/Preamble Length Register ..... 174
5.21 BANK 7 ..... 175
5.21.1 IRRXDC – Infrared Receiver Demodulator Control Register ..... 175

5.21.2 IRTXMC – Infrared Transmitter Modulator Control Register ..... 178
5.21.3 RCCFG – CEIR Configuration Register ..... 179
5.21.4 LCR/BSR – Link Control/Bank Select Registers ..... 179
5.21.5 IRCFG [1–4] – Infrared Interface Configuration Registers ..... 179
5.22 SERIAL COMMUNICATION CONTROLLER2 REGISTER BITMAPS ..... 182

## 6.0 DMA and Interrupt Mapping

6.1 DMA SUPPORT ..... 190
6.1.1 Legacy Mode ..... 190
6.1.2 Plug and Play Mode ..... 190
6.2 INTERRUPT SUPPORT ..... 191
6.2.1 Legacy Mode ..... 191
6.2.2 Plug and Play Mode ..... 192

## 7.0 Power Management

7.1 POWER-DOWN STATE ..... 194
7.1.1 Recommended Power-Down Methods - Group 1 ..... 194
7.1.2 Recommended Power-Down Methods - Group 2 ..... 195
7.1.3 Special Power-Down Cases ..... 195
7.2 POWER-UP ..... 195
7.2.1 The Clock Multiplier ..... 195
7.2.2 Chip Power-Up Procedure ..... 195
7.2.3 SCC1 and SCC2 Power-Up ..... 196
7.2.4 FDC Power-Up ..... 196

## 8.0 Device Description

8.1 GENERAL ELECTRICAL CHARACTERISTICS ..... 197
8.1.1 Absolute Maximum Ratings ..... 197
8.1.2 Capacitance ..... 197
8.1.3 Electrical Characteristics ..... 197
8.2 DC CHARACTERISTICS OF PINS, BY GROUP ..... 198
8.2.1 Group 1 ..... 198
8.2.2 Group 2 ..... 198
8.2.3 Group 3 ..... 198
8.2.4 Group 4 ..... 199
8.2.5 Group 5 ..... 199
8.2.6 Group 6 ..... 199
8.2.7 Group 7 ..... 200
8.2.8 Group 8 ..... 200
8.2.9 Group 9 ..... 201
8.2.10 Group 10 ..... 201
8.2.11 Group 11 ..... 201
8.2.12 Group 12 ..... 202
8.2.13 Group 13 ..... 202

8.3 AC ELECTRICAL CHARACTERISTICS ..... 202
8.3.1 AC Test Conditions $T_A$ = 0° C to 70° C, $V_{DD}$ = 5.0 V ± 10%, 3.3 V ± 10% ..... 202
8.4 SWITCHING CHARACTERISTICS ..... 203
8.4.1 Timing Table ..... 203
8.4.2 Timing Diagrams ..... 207

## 9.0 Appendix A

COMPARISON OF PC87338 AND PC97338 ..... 216

# List of Figures

FIGURE 1 Plug and Play Protocol Flowchart ..... 39
FIGURE 2 LFSR Circuit ..... 40
FIGURE 3 FER Register Bitmap ..... 45
FIGURE 4 FAR Register Bitmap ..... 47
FIGURE 5 PTR Register Bitmap ..... 48
FIGURE 6 FCR Register Bitmap ..... 48
FIGURE 7 PCR Register Bitmap ..... 49
FIGURE 8 PMC Register Bitmap ..... 50
FIGURE 9 TUP Register Bitmap ..... 51
FIGURE 10 SID Register Bitmap ..... 52
FIGURE 11 ASC Register Bitmap ..... 52
FIGURE 12 CS0LA Register Bitmap ..... 53
FIGURE 13 CS0CF Register Bitmap ..... 53
FIGURE 14 CS1LA Register Bitmap ..... 54
FIGURE 15 CS1CF Register Bitmap ..... 54
FIGURE 16 CS0HA Register Bitmap ..... 55
FIGURE 17 CS1HA Register Bitmap ..... 55
FIGURE 18 SCF0 Register Bitmap ..... 55
FIGURE 19 SCF1 Register Bitmap ..... 56
FIGURE 20 PNP0 Register Bitmap ..... 57
FIGURE 21 PNP1 Register Bitmap ..... 58
FIGURE 22 SCF2 Register Bitmap ..... 58
FIGURE 23 Busy Flag Timing ..... 59
FIGURE 24 PNP2 Register Bitmap ..... 59
FIGURE 25 PBAL Register Bitmap ..... 60
FIGURE 26 PBAH Register Bitmap ..... 61
FIGURE 27 S1BAL Register Bitmap ..... 61
FIGURE 28 S1BAH Register Bitmap ..... 61
FIGURE 29 S2BAL Register Bitmap ..... 61
FIGURE 30 S2BAH Register Bitmap ..... 62
FIGURE 31 FBAL Register Bitmap ..... 62
FIGURE 32 FBAH Register Bitmap ..... 62
FIGURE 33 SBAL Register Bitmap ..... 63
FIGURE 34 SBAH Register Bitmap ..... 63
FIGURE 35 SIRQ1 Register Bitmap ..... 63
FIGURE 36 SIRQ2 Register Bitmap ..... 64
FIGURE 37 SIRQ3 Register Bitmap ..... 65
FIGURE 38 PNP3 Register Bitmap ..... 66
FIGURE 39 SCF3 Register Bitmap ..... 67
FIGURE 40 CLK Register Bitmap ..... 68
FIGURE 41 FDC Functional Block Diagram ..... 69
FIGURE 42 PC87338/PC97338 Dynamic Window Margin Performance ..... 70
FIGURE 43 Read Algorithm State Diagram ..... 71
FIGURE 44 Perpendicular Recording Drive Read/Write Head and Pre-Erase Head ..... 72
FIGURE 45 SRA Register Bitmap ..... 75
FIGURE 46 SRB Register Bitmap ..... 76
FIGURE 47 DOR Register Bitmap ..... 78
FIGURE 48 TDR Register Bitmap ..... 79
FIGURE 49 MSR Register Bitmap ..... 81

FIGURE 50 DSR Register Bitmap ..... 82
FIGURE 51 FDC Data Register Bitmap ..... 83
FIGURE 52 DIR Register Bitmap ..... 84
FIGURE 53 CCR Register Bitmap ..... 84
FIGURE 54 ST0 Result Phase Register Bitmap ..... 88
FIGURE 55 ST1 Result Phase Register Bitmap ..... 89
FIGURE 56 ST2 Result Phase Register Bitmap ..... 90
FIGURE 57 ST3 Result Phase Register ..... 91
FIGURE 58 IBM, Perpendicular, and ISO Formats Supported by FORMAT TRACK Command ..... 99
FIGURE 59 PC87338/PC97338 Four Floppy Disk Drive Circuit ..... 122
FIGURE 60 DTR Register Bitmap (SPP Mode) ..... 125
FIGURE 61 STR Register Bitmap (SPP Mode) ..... 125
FIGURE 62 CTR Register Bitmap (SPP Mode) in PC87338 ..... 126
FIGURE 63 CTR Register Bitmap (SPP Mode) in PC97338 ..... 126
FIGURE 64 DTR Register Bitmap (EPP Mode) ..... 129
FIGURE 65 STR Register Bitmap (EPP Mode) ..... 129
FIGURE 66 CTR Register Bitmap (EPP Mode) ..... 130
FIGURE 67 DTR Register Bitmap (EPP Mode) ..... 130
FIGURE 68 DTR Register Bitmap (EPP Mode) ..... 130
FIGURE 69 DTR Register Bitmap (EPP Mode) ..... 130
FIGURE 70 EPP Data Port 2 Bitmap ..... 130
FIGURE 71 EPP Data Port 3 Bitmap ..... 131
FIGURE 72 EPP 1.7 Address Write ..... 131
FIGURE 73 EPP 1.7 Address Read ..... 132
FIGURE 74 EPP Write with Zero Wait States ..... 132
FIGURE 75 EPP 1.9 Address Write ..... 133
FIGURE 76 EPP 1.9 Address Read ..... 133
FIGURE 77 DATAR Register Bitmap ..... 136
FIGURE 78 AFIFO Register Bitmap ..... 137
FIGURE 79 ECP DSR Register Bitmap ..... 137
FIGURE 80 DCR Register Bitmap ..... 137
FIGURE 81 CFIFO Register Bitmap ..... 138
FIGURE 82 DFIFO Register Bitmap ..... 139
FIGURE 83 TFIFO Register Bitmap ..... 139
FIGURE 84 CNFGA Register Bitmap ..... 139
FIGURE 85 CNFGB Register Bitmap ..... 140
FIGURE 86 ECR Register Bitmap ..... 140
FIGURE 87 ECP Forward Write Cycle ..... 142
FIGURE 88 ECP (Reverse) Read Cycle ..... 143
FIGURE 88 Composite Serial Data ..... 146
FIGURE 88 Register Bank Architecture ..... 153
FIGURE 88 Interrupt Enable Register ..... 154
FIGURE 88 Event Identification Register, Non-Extended Mode ..... 155
FIGURE 88 Event Identification Register, Extended Mode ..... 156
FIGURE 88 FIFO Control Register ..... 157
FIGURE 88 Link Control Register ..... 158
FIGURE 88 Modem Control Register, Non-Extended Mode ..... 159
FIGURE 88 Modem Control Register, Extended Modes ..... 159
FIGURE 88 Link Status Register ..... 160
FIGURE 88 Modem Status Register ..... 162
FIGURE 88 Auxillary Status and Control Register ..... 162

FIGURE 88 Extended Control Register 1 ..... 166
FIGURE 88 DMA Control Signals Routing ..... 167
FIGURE 88 Extended Control Register 2 ..... 167
FIGURE 88 Transmit FIFO Level ..... 168
FIGURE 88 Receive FIFO Level ..... 168
FIGURE 88 Infrared Control Register 1 ..... 169
FIGURE 88 Pipelined Mode Register ..... 171
FIGURE 88 IInfrared Control Register 2 ..... 171
FIGURE 88 Frame Status Byte Register ..... 172
FIGURE 88 Infrared Control Register 3 ..... 173
FIGURE 88 MIR Pulse Width Register ..... 173
FIGURE 88 SIR Pulse Width Register ..... 174
FIGURE 88 Beginning Flags/Preamble Length Register ..... 174
FIGURE 88 Intrared Receiver Demodulator Control Register ..... 175
FIGURE 88 Intrared Transmitter Modulator Control Register ..... 178
FIGURE 88 CEIR Configuration Register ..... 179
FIGURE 88 Infrared Configuration Register 1 ..... 180
FIGURE 88 Infrared Configuration Register 2 ..... 180
FIGURE 88 Infrared Configuration Register 3 ..... 181
FIGURE 88 Infrared Configuration Register 4 ..... 181
FIGURE 89 Load Circuit ..... 202
FIGURE 90 Testing Specification Standard ..... 203
FIGURE 91 Clock Timing ..... 207
FIGURE 92 CPU Read Timing ..... 208
FIGURE 93 CPU Write Timing ..... 208
FIGURE 94 DMA Access Timing ..... 209
FIGURE 95 UART, Sharp-IR and CEIR Timing ..... 209
FIGURE 96 SIR, MIR and FIR Timing ..... 210
FIGURE 97 IRSLn Write Timing ..... 210
FIGURE 98 Modem Control Timing ..... 211
FIGURE 99 FDC Write Data Timing ..... 211
FIGURE 100 FDC Read Data Timing ..... 211
FIGURE 101 FDC Control Signals Timing ..... 212
FIGURE 102 Parallel Port Interrupt Timing (Compatible Mode) ..... 212
FIGURE 103 Parallel Port Interrupt Timing (Extended Mode) ..... 212
FIGURE 104 Parallel Port Data Transfer Timing (Compatible Mode) ..... 213
FIGURE 105 Parallel Port Data Transfer Timing (EPP 1.7 Mode) ..... 213
FIGURE 106 Parallel Port Data Transfer Timing (EPP 1.9 Mode) ..... 214
FIGURE 107 Parallel Port Forward Transfer Timing (ECP Mode) ..... 214
FIGURE 108 Parallel Port Reverse Transfer Timing (ECP Mode) ..... 215
FIGURE 109 System Interrupts Timing ..... 215
FIGURE 110 CS1-0 Signals Timing ..... 215
FIGURE 111 Reset Timing ..... 215

# List of Tables


TABLE 1 Signal/Pin Description Table ..... 22
TABLE 2 Multi-Function Pins (Excluding Strap Pins) ..... 34
TABLE 3 IRQ12, A15-11 / SCC2 / Infrared Pin Allocation ..... 35
TABLE 4 SCC2 Mode Configurations 1 ..... 35
TABLE 5 SCC2 Mode Configurations 2 ..... 35
TABLE 6 Default Configurations Controlled by Hardware ..... 36
TABLE 7 Configuration Registers ..... 36
TABLE 8 INDEX and DATA Register Address Options and Configuration Register Accessibility ..... 38
TABLE 9 Primary and Secondary Drive Address Selection ..... 46
TABLE 10 Encoded Drive and Motor Pin Information (Bit 4 of FER = 1) ..... 46
TABLE 11 Parallel Port Addresses ..... 47
TABLE 12 COM Port Selection for SCC1 ..... 47
TABLE 13 COM Port Selection for SCC2 ..... 47
TABLE 14 Address Selection for COM3 and COM4 ..... 47
TABLE 15 Parallel Port Mode ..... 49
TABLE 16 Bit Settings to Enable $\overline{\text{MRT1}}$, IDLE or IRSL2 ..... 51
TABLE 17 Bit Settings to Enable $\overline{\text{DR1}}$ or PD ..... 51
TABLE 18 ECP DMA Option Selection ..... 56
TABLE 19 Parallel Port Plug and Play DMA Settings ..... 56
TABLE 20 Parallel Port Plug and Play Interrupt Assignment ..... 57
TABLE 21 Parallel Port Plug and Play Interrupt Mapping ..... 57
TABLE 22 TDR Bit 5 Values ..... 58
TABLE 23 FDC Plug and Play Interrupt Mapping ..... 59
TABLE 24 FDC Plug and Play DMA Settings ..... 60
TABLE 25 SBAL Reset Values ..... 63
TABLE 26 SBAH Reset Values ..... 63
TABLE 27 SIRQI1 Plug and Play Interrupt Mapping ..... 64
TABLE 28 SIRQ1 Interrupt Settings 64
TABLE 29 SIRQI2 Plug and Play Interrupt Mapping ..... 65
TABLE 30 Selecting MSEN1, DRATE1, $\overline{\text{CS0}}$ or SIRQI2 ..... 65
TABLE 31 SIRQI3 Plug and Play Interrupt Mapping ..... 66
TABLE 32 Selecting $\overline{\text{DRV2}}$, $\overline{\text{DR23}}$, PNF or SIRQI3 ..... 66
TABLE 33 SCC2 Receiver Channel Selection ..... 67
TABLE 34 SCC2 Transmission Channel Selection ..... 67
TABLE 35 The FDC Registers and Their Addresses ..... 74
TABLE 36 Drive and Motor Pin Encoding When FER 4 = 1 ..... 77
TABLE 37 Drive Enable Hexadecimal Values ..... 77
TABLE 38 TDR Bit Utilization and Reset Values in Different Drive Modes ..... 79
TABLE 39 Media Type Bit Settings ..... 80
TABLE 40 Data Transfer Rate Encoding ..... 82
TABLE 41 Write Precompensation Delays ..... 82
TABLE 42 Default Precompensation Delays ..... 82
TABLE 43 FDC Command Set Summary ..... 92
TABLE 44 Bytes per Sector Codes ..... 97
TABLE 45 Typical Values for PC Compatible Diskette Media ..... 97
TABLE 46 Typical Gap Values ..... 98
TABLE 47 Multipliers and Head Settle Time Ranges for Different Data Transfer Rates ..... 102
TABLE 48 DENSEL Encoding ..... 102
TABLE 49 Effect of Drive Mode and Data Rate on FORMAT TRACK and WRITE DATA Commands ..... 104

TABLE 50 Effect of GDC Bits on FORMAT TRACK and WRITE DATA Commands ..... 104
TABLE 51 Skip Control Effect on READ DATA Command ..... 107
TABLE 52 Result Phase Termination Values with No Error ..... 108
TABLE 53 SK Effect on READ DELETED DATA Command ..... 108
TABLE 54 Maximum RECALIBRATE Step Pulses for Values of R255 and ETR ..... 111
TABLE 55 The Effect of Scan Commands on the ST2 Register ..... 113
TABLE 56 Interrupt Causes Reported by SENSE INTERRUPT ..... 114
TABLE 57 Defining Bytes to Read or Write Using SET TRACK ..... 116
TABLE 58 Constant Multipliers for Delay After Processing Factor and Delay Ranges ..... 117
TABLE 59 Constant Multipliers for Delay Before Processing Factor and Delay Ranges ..... 117
TABLE 60 $\overline{\text{STEP}}$ Time Interval Calculation ..... 117
TABLE 61 VERIFY Command Termination Conditions ..... 119
TABLE 62 Parallel Port Reset States ..... 124
TABLE 63 Standard Parallel Port Registers ..... 124
TABLE 64 SPP Data Register Read and Write Modes ..... 125
TABLE 65 EPP Revision Selection ..... 127
TABLE 66 Parallel Port Registers in EPP Modes ..... 128
TABLE 67 ECP Modes Encoding ..... 133
TABLE 68 Parallel Port Registers in ECP Modes ..... 134
TABLE 69 ECP Mode DMA Selection ..... 140
TABLE 70 ECP Mode Interrupt Selection ..... 140
TABLE 71 ECP Modes ..... 141
TABLE 72 Parallel Port Pin Out ..... 144
TABLE 73 Register Bank Summary ..... 153
TABLE 74 Bank 0 Serial Controller Base Registers þ ..... 153
TABLE 75 Non-Extended Mode Interrupt Priorities ..... 155
TABLE 76 TX_FIFO Level Selection ..... 157
TABLE 77 RX_FIFO Level Selection ..... 157
TABLE 78 Word Length Select Encoding ..... 158
TABLE 79 Bit Settings for Parity Control ..... 158
TABLE 80 Bank Selection Encoding ..... 159
TABLE 81 The Module Operation Modes ..... 160
TABLE 82 Bank 1 Register Set ..... 163
TABLE 83 Bank 2 Register Set ..... 164
TABLE 84 Baud Generator Divisor Settings ..... 165
TABLE 85 Bank 3 Register Set ..... 168
TABLE 86 Bank 4 Register Set ..... 169
TABLE 87 Bank 5 Register ..... 170
TABLE 88 Bank 6 Register Set ..... 173
TABLE 89 MIR Pulse Width Settings ..... 174
TABLE 90 FIR Preamble Length ..... 174
TABLE 91 MIR Beginning Flags ..... 175
TABLE 92 Bank 7 Register Set ..... 175
TABLE 93 CEIR, Low Speed Demodulator (RXHSC = 0) (Frequency Ranges in kHz)þ ..... 176
TABLE 94 Consumer IR High Speed Demodulator Frequency Ranges in kHz (RXHSC = 1) ..... 177
TABLE 95 Sharp-IR Demodulator Frequency Ranges in kHz ..... 177
TABLE 96 CEIR Carrier Frequency Encoding ..... 178
TABLE 97 Infrared Receiver Input Selection ..... 182
TABLE 98 DMA Support in Legacy Mode ..... 190
TABLE 99 DMA Support in Plug and Play Mode ..... 190
TABLE 100 Interrupt Support in Legacy Mode for IRQ3, 4, 6, 7, 9 10 and 11 ..... 191

TABLE 101 Interrupt Support in Legacy Mode for IRQ 5, 12 and 15 ..... 191
TABLE 102 TRI-STATE Condition for Interrupts in Legacy Mode ..... 192
TABLE 103 Interrupt Support in Plug and Play Mode for IRQ3, 4, 6, 7, 9, 10 or 11 ..... 193
TABLE 104 Interrupt Support in Plug and Play Mode for IRQ 5, 12 or 15 ..... 193
TABLE 105 TRI-STATE Conditions for Interrupts in Plug and Play Mode ..... 193
TABLE 106 Group 1 Power-Down ..... 194
TABLE 107 Clock Multiplier Encoding Options ..... 196
TABLE 108 Capacitance: $T_A$ 0°C to 70°C, $V_{DD}$ = 5V +/- 10% or 3.3V +/- 10%, $V_{SS}$ = 0V ..... 197
TABLE 109 Power Consumption ..... 197
TABLE 110 DC Characteristics of Group 1 Pins ..... 198
TABLE 111 DC Characteristics of Group 2 Pins ..... 198
TABLE 112 DC Characteristics of Group 3 Pins ..... 199
TABLE 113 DC Characteristics of Group 4 Pins ..... 199
TABLE 114 DC Characteristics of Group 5 Pins ..... 199
TABLE 115 DC Characteristics of Group 6 Input Pins ..... 200
TABLE 116 DC Characteristics of Group 6 Output Pins ..... 200
TABLE 117 DC Characteristics of Group 7 Pins ..... 200
TABLE 118 DC Characteristics of Group 8 Pins ..... 200
TABLE 119 DC Characteristics of Group 9 Pins ..... 201
TABLE 120 DC Characteristics of Group 10 Pins ..... 201
TABLE 121 DC Characteristics of Group 11 Pins ..... 201
TABLE 122 DC Characteristics of Group 12 Pins ..... 202
TABLE 123 DC Characteristics of Group 13 Pins ..... 202

# 1.0 Pin Descriptions

## 1.1 CONNECTION DIAGRAMS

**Plastic Quad Flatpack (PQFP), EIAJ**

**Order Number PC87338VLJ**
**See NS Package Number VLJ100A**

**Thin Quad Flatpack (TQFP), JEDEC**

**Order Number PC87338VJG**
**See NS Package Number VJG100A**

**Plastic Quad Flatpack (PQFP), EIAJ**

**Order Number PC97338VLJ**
**See NS Package Number VLJ100A**

**Thin Quad Flatpack (TQFP), JEDEC**

**Order Number PC97338VJG**
**See NS Package Number VJG100A**

## 1.2 SIGNAL/PIN DESCRIPTIONS

Table 1 lists the signals of the Chip in alphabetical order. It also shows the pin associated with each signal for the Plastic Quad Flatpack, (PQFP) and Thin Quad Flatpack (TQFP) options. The I/O column describes whether the pin is an input, output, or bidirectional pin (marked as I, O or I/O, respectively). This column also specifies which group in Section 8.2 describes the pin's DC characteristics.

Refer to the glossary for an explanation of abbreviations and terms used in this table and throughout this document. Use the Table of Contents to find more information about each register.

**TABLE 1. Signal/Pin Description Table**

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| A0<br>A1<br>A2<br>A3<br>A4<br>A5<br>A6<br>A7<br>A8<br>A9<br>A10<br>A11<br>A12<br>A13<br>A14<br>A15 | 30<br>29<br>28<br>27<br>26<br>25<br>24<br>23<br>22<br>21<br>31<br>62<br>63<br>64<br>66<br>69 | 28<br>27<br>26<br>25<br>24<br>23<br>22<br>21<br>20<br>19<br>29<br>60<br>61<br>62<br>64<br>67 | I<br>Group 1 | **Address.** These address lines from the microprocessor determine which internal register is accessed. The values of A15-0 have no effect during DMA transfers.<br>If CFG0 = 0 during reset, A15-0 are used for address decoding.<br>If CFG0 = 1 during reset, only A10-0 are used for address decoding, and A15-11 are ignored (masked to 0).<br>In Legacy mode, A10 is used only for ECP decoding.<br>A15-11 are multiplexed with SCC2's signals. |
| $\overline{\text{ACK}}$ | 85 | 83 | I<br>Group 3 | **Acknowledge.** This parallel port input signal is pulsed low by an external printer to indicate it received data from the parallel port.<br>This pin is internally connected to a nominal 25 KΩ pull-up resistor.<br>$\overline{\text{ACK}}$ is multiplexed with $\overline{\text{DR1}}$. (See Table 72 for more information). |
| ADRATE0<br>ADRATE1 | 98<br>48 | 96<br>46 | O<br>Group 10 | **Additional Data Rate signals 0 and 1.** These FDC output signals are provided in addition to DRATE1,0 and have a similar function. They reflect the currently selected FDC data rate, (bits 0 and 1 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last).<br>ADRATE0 is configured when bit 0 of ASC is 1. ADRATE1 is configured when bit 4 of ASC is 1.<br>ADRATE0 is multiplexed with IRQ5 and ADRATE1 is multiplexed with DENSEL. |
| AEN | 20 | 18 | I<br>Group 1 | **Address Enable.** When set to 1, this pin enables DMA addressing and disables the microprocessor Address. The address lines disabled will be A15-0 or A10-0, depending on whether CFG0 was set to 0 or 1 during reset (respectively).<br>Access during DMA transfer is NOT affected by this pin. |
| $\overline{\text{AFD}}$ | 78 | 76 | O<br>Group 11 | **Automatic Feed XT.** When low this parallel port signal indicates to the external printer that it should automatically line feed after each Carriage Return byte. This signal enters a TRI-STATE® condition within 10 nsec after a 0 is loaded into the Control Register bit.<br>An external 4.7 KΩ pull-up resistor should be attached to this pin.<br>$\overline{\text{AFD}}$ is multiplexed with $\overline{\text{DSTRB}}$ and DENSEL. See Table 72 for more information. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| $\overline{\text{ASTRB}}$ | 81 | 79 | O<br>Group 11 | **Address Strobe.** This active-low signal is used in EPP mode as an address strobe.<br>$\overline{\text{ASTRB}}$ is multiplexed with $\overline{\text{SLIN}}$ and $\overline{\text{STEP}}$. See Table 72 for more information. |
| BADDR0<br>BADDR1 | 74<br>73 | 72<br>71 | I<br>Group 1 | **SIO Base Address Straps 0 and 1.** These bits must be externally strapped to determine which one of four base address options for the INDEX and DATA registers will be used by the system after reset. See Table 8.<br>If BADDR1 = 0 and BADDR0 = 1 during reset, the chip "wakes up" without a base address and the Plug and Play protocol should be applied. For more details see Section 2.<br>These pins are internally grounded by a 30 KΩ pull-down resistor. To strap these pins high, pull them up to $V_{cc}$ with a 10 KΩ resistor.<br>BADDR0 is multiplexed with $\overline{\text{RTS1}}$, and BADDR1 is multiplexed with SOUT1 (and BOUT1 in PC87338 only). |
| BOUT1<br>BOUT2 | 73*(71)*<br>65*(63)* | 71*(69)*<br>63*(61)* | O<br>Group 7 | **SCC Baud Output signals 1 and 2.** These multi-function pins provide the associated serial channel Baud Rate generator output signal for SCC1 or SCC2, if test mode is selected in the Power and Test Configuration Register (PTR) and the DLAB bit (LCR7) is set.<br>BOUT1 is multiplexed with SOUT1 and BADDR1. BOUT2 is multiplexed with SOUT2, IRTX and CFG0 (in PC87338 only).<br>*BOUT1 is multiplexed with $\overline{\text{DTR1}}$. BOUT2 is multiplexed with $\overline{\text{DTR2}}$ and A12 (in PC97338 only).* |
| BUSY | 84 | 82 | I<br>Group 2 | **Busy.** This parallel port signal is set high by the external printer when it cannot accept another character.<br>This pin is internally grounded by a nominal 25 KΩ pull-down resistor.<br>BUSY is multiplexed with $\overline{\text{MTR1}}$ and $\overline{\text{WAIT}}$. (See Table 72 for more information). |
| CFG0 | 65 | 63 | I<br>Group 9 | **Configuration.** This CMOS input signal is externally strapped to select one of two default configurations in which the Chip powers up (see Table 6).<br>This pin is internally grounded by a 30 KΩ pull-down resistor. To strap this pin high, pull it up to $V_{CC}$ with a 10 KΩ resistor.<br>CFG0 is multiplexed with SOUT2 and IRTX. |
| $\overline{\text{CS0}}$<br>$\overline{\text{CS1}}$ | 51<br>3 | 49<br>1 | O<br>Group 8 | **Programmable Chip Select signals 0 and 1.** $\overline{\text{CS1,0}}$ are programmable chip select and/or latch enable and/or output enable signals that can be used as game port, I/O expander, etc.<br>The decoded address and the assertion conditions are configured via the Chip configuration registers, indexed by 0Ah-0Dh, 10h-11h, 03h and 4Dh.<br>$\overline{\text{CS1,0}}$ are push-pull output signals.<br>$\overline{\text{CS0}}$ is multiplexed with DRATE1, MSEN1, SIRQI2 and $\overline{\text{DACK3}}$.<br>$\overline{\text{CS1}}$ is multiplexed with $\overline{\text{ZWS}}$. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| $\overline{CTS1}$<br>$\overline{CTS2}$ | 72<br>64 | 70<br>62 | I<br>Group 1 | **UART Clear to Send signals 1 and 2.** When low, this signal indicates that the modem or data transfer device is ready to exchange data.<br>The $\overline{CTS}$ signal is a modem status input signal whose condition can be tested by reading bit 4 (CTS) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MSR indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MSR. $\overline{CTS}$ has no effect on the transmitter.<br>If modem status interrupts are enabled, an interrupt is generated whenever the DCTS bit of the MSR is set.<br>$\overline{CTS2}$ is multiplexed with A13. When $\overline{CTS2}$ is not selected, it is masked to 0. |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | 17<br>16<br>15<br>14<br>13<br>12<br>11<br>10 | 15<br>14<br>13<br>12<br>11<br>10<br>9<br>8 | I/O<br>Group 6 | **Data.** These signals are bi-directional data lines to the microprocessor. D0 is the LSB and D7 is the MSB. |
| $\overline{DACK0}$ | 55 | 53 | I<br>Group 1 | **DMA Acknowledge 0.** An active low input signal used to acknowledge DMA request 0 (DRQ0), and to enable the $\overline{RD}$ and $\overline{WR}$ input signals during a DMA transfer. It can be used by either the FDC, or the SCC2 or the parallel port. If none of them uses this input signal, it is ignored. If the device which uses this signal is disabled or configured with no DMA, the signal is also ignored. Upon reset, it is ignored. |
| $\overline{DACK1}$ | 54 | 52 | I<br>Group 1 | **DMA Acknowledge 1.** An active low input signal used to acknowledge DMA request 1 (DRQ1), and enable the $\overline{RD}$ and $\overline{WR}$ input signals during a DMA transfer. It can be used by one of the following: FDC, SCC2 or parallel port. If none of them uses this input signal, it is ignored. If the device which uses this signal is disabled or configured with no DMA, the signal is also ignored. Upon reset, it is ignored. |
| $\overline{DACK2}$ | 5 | 3 | I<br>Group 1 | **DMA Acknowledge 2.** An active low input signal used to acknowledge DMA request 2 (DRQ2), and enable the $\overline{RD}$ and $\overline{WR}$ input signals during a DMA transfer. It can be used by one of the following: FDC, SCC2 or parallel port. If none of them uses this input signal, it is ignored. If the device which uses this signal is disabled or configured with no DMA, the signal is also ignored. Upon reset, it is used by the FDC. |
| $\overline{DACK3}$ | 51 | 49 | I<br>Group 1 | **DMA Acknowledge 3.** An active low input signal used to acknowledge DMA request 3 (DRQ3), and enable the $\overline{RD}$ and $\overline{WR}$ inputs during a DMA transfer. It can be used by one of the following: FDC, SCC2 or parallel port. If none of them uses this input signal, it is ignored. If the device which uses this signal is disabled or configured with no DMA, the signal is also ignored. Upon reset, it is used by the FDC. $\overline{DACK3}$ is multiplexed with DRATE1, MSEN1, $\overline{CS0}$ and SIRQI2. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| $\overline{DCD1}$<br>$\overline{DCD2}$ | 77<br>69 | 75<br>67 | I<br>Group 1 | **UART Data Carrier Detect signals 1 and 2.** When low, this signal indicates that the modem or data transfer device has detected the data carrier.<br>The $\overline{DCD2,1}$ signals are modem status input signals whose condition can be tested by reading bit 7 (DCD) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MSR indicates whether the $\overline{DCD}$ input signal has changed state since the previous reading of the MSR.<br>If modem status interrupts are enabled, an interrupt is generated whenever the DDCD bit of the MSR is set to 1.<br>$\overline{DCD2}$ is multiplexed with A15. When $\overline{DCD2}$ is not selected, it is masked to 1. |
| DENSEL (Normal Mode) | 48 | 46 | O<br>Group 10 | **Density Select.** Indicates that a high density FDC data rate (500 Kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 Kbps or 300 Kbps) is selected. The polarity of DENSEL is controlled via bit 6 of the ASC register. The default is active high for high density.<br>DENSEL is also programmable via the MODE command.<br>DENSEL is multiplexed with ADRATE1. |
| (PPM Mode) | 78 | 76 | O<br>Group 10 | **Density Select.** This pin provides an additional Density Select signal in PPM mode when PNF = 0.<br>DENSEL is multiplexed with $\overline{AFD}$, $\overline{DSTRB}$. See Table 72 for more information. |
| $\overline{DIR}$ (Normal Mode) | 41 | 39 | O<br>Group 10 | **Direction.** This FDC output signal determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in, inactive = step out) during a seek operation. During read or write operations, $\overline{DIR}$ is inactive. |
| (PPM Mode) | 80 | 78 | O<br>Group 10 | **Direction.** This FDC pin provides an additional direction signal in PPM Mode when PNF = 0. $\overline{DIR}$ is multiplexed with $\overline{INIT}$. See Table 72 for more information. |
| $\overline{DR0}$<br>$\overline{DR1}$<br>(Normal Mode) | 44<br>45 | 42<br>43 | O<br>Group 10 | **FDC Drive Select signals 0 and 1.** These FDC signals are decoded drive select output signals controlled by Digital Output Register bits D0 and D1.<br>These signals are gated with DOR bits 7 through 4. These are active low output signals. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. $\overline{DR0,1}$ are exchanged only via the TDR register. (Bit 4 of the FCR register is reserved.)<br>$\overline{DR1}$ is multiplexed with PD. |
| $\overline{DR1}$ (PPM Mode) | 85 | 83 | O<br>Group 10 | **FDC Drive Select 1.** This signal provides an additional drive select signal in PPM mode when PNF = 0. It is drive select 1 when bit 4 of FCR is 0. It is drive select 0 when bit 4 of FCR is 1. This signal is active low. $\overline{DR1}$ is multiplexed with $\overline{ACK}$. See Table 72 for more information. |
| $\overline{DR23}$ | 49 | 47 | O<br>Group 10 | **Drive 2 or 3.** This FDC signal is asserted when either drive 2 or drive 3 is accessed (except during logical drive exchange, see bit 3 of TDR). This pin is configured when bits 7, 6 of SIRQ3 are 01.<br>$\overline{DR23}$ is multiplexed with IRSL0, $\overline{DRV2}$, SIRQI3 and PNF. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| DRATE0<br>DRATE1<br>(Normal Mode) | 52<br>51 | 50<br>49 | O<br>Group 8 | **Data Rates 0 and 1.** These FDC output signals reflect the currently selected FDC data rate, (bits 1 and 0 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last). The pins are totem-pole buffered output signals (6 mA sink, 6 mA source).<br>DRATE0 is multiplexed with MSEN0. DRATE1 is multiplexed with MSEN1, SIRQI2, $\overline{\text{CS0}}$ and $\overline{\text{DACK3}}$. |
| DRATE0<br>(PPM Mode) | 87 | 85 | O<br>Group 8 | **Data Rate 0.** This pin provides an additional FDC data rate signal, in PPM mode, when PNF = 0.<br>DRATE0 is multiplexed with PD6. See Table 72 for more information. |
| DRQ0<br>DRQ1<br>DRQ2<br>DRQ3 | 56<br>33<br>4<br>60 | 54<br>31<br>2<br>58 | O<br>Group 6 | **DMA Requests 0, 1, 2 and 3.** These active high outputs signal the DMA controller that a data transfer is required.<br>This DMA request can be sourced by one of the following: FDC, SCC2 or parallel port. When not sourced by any of them, it is in TRI-STATE. In Plug and Play mode, when the sourced device is disabled or when the sourced device is configured with no DMA, it is also in TRI-STATE. Upon reset, DRQ2 is used by the FDC; and DRQ0,1 and 3 are in TRI-STATE.<br>DRQ3 is multiplexed with IRQ15, and SIRQI1. |
| $\overline{\text{DRV2}}$ | 49 | 47 | I<br>Group 4 | **Drive2.** This FDC input signal indicates (low) when a second disk drive has been installed. The state of this signal is available from Status Register A in PS/2 mode. This pin is configured when bits 7 and 6 of SIRQ3 are 00.<br>$\overline{\text{DRV2}}$ is multiplexed with $\overline{\text{DR23}}$, PNF, SIRQI3 and IRSL2. |
| $\overline{\text{DSKCHG}}$<br>(Normal Mode) | 32 | 30 | I<br>Group 4 | **Disk Change.** This FDC input signal indicates if the drive door is open. The state of this signal is available from the Digital Input Register (DIR). This signal can also be configured as the RGATE data separator diagnostic input signal via the MODE command (see “The MODE Command” on page -101) |
| (PPM Mode) | 89 | 87 | I<br>Group 4 | **Disk Change.** This signal provides an additional FDC Disk Change signal in PPM Mode when PNF = 0.$\overline{\text{DSKCHG}}$ is multiplexed with PD4. See Table 36 for more information. |
| $\overline{\text{DSR1}}$<br>$\overline{\text{DSR2}}$ | 76<br>68 | 74<br>66 | I<br>Group 1 | **Data Set Ready signals 1 and 2.** When low, these UART signals indicates that the appropriate data transfer device or modem is ready to establish a communications link. The $\overline{\text{DSR}}$ signal is a modem status input whose condition can be tested by reading bit 5 (DSR) of the Modem Status Register (MSR) for the appropriate channel. Bit 5 is the complement of the $\overline{\text{DSR}}$ signal. Bit 1 (DDSR) of the MSR indicates whether the $\overline{\text{DSR}}$ input signal has changed state since the previous reading of the MSR.<br>If modem status interrupts are enabled an interrupt is generated whenever the DDSR bit of the MSR is set.<br>When $\overline{\text{DSR2}}$ is not selected, it is masked to 0**.**<br>$\overline{\text{DSR2}}$ is multiplexed with IRRX2, IRQ12 and IRSL0. |
| $\overline{\text{DSTRB}}$ | 78 | 76 | O<br>Group 11 | **Data Strobe.** This signal is used in EPP mode as a data strobe. It is active low.<br>$\overline{\text{DSTRB}}$ is multiplexed with $\overline{\text{AFD}}$, DENSEL. See Table 72 for more information. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| $\overline{DTR1}$<br>$\overline{DTR2}$ | 71<br>63 | 69<br>61 | O<br>Group 7 | **Data Terminal Ready signals 1 and 2.** When low, these UART output signals indicate to the appropriate modem or data transfer device that the UART is ready to establish a communications link.<br>The $\overline{DTR}$ signal can be set to active low by programming bit 0 (DTR) of the Modem Control Register (MCR) to a high level. A Master Reset (MR) operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.<br>$\overline{DTR2}$ is multiplexed with A12 *(and BOUT2 in PC97338 only)*. |
| $\overline{ERR}$ | 79 | 77 | I<br>Group 3 | **Error.** This parallel port input signal is set low by the external printer when it has detected an error.<br>This pin is internally connected to a nominal 25 KΩ pull-up resistor.<br>$\overline{ERR}$ is multiplexed with $\overline{HDSEL}$. See Table 72 for more information. |
| $\overline{HDSEL}$ (Normal Mode) | 34 | 32 | O<br>Group 10 | **Head Select.** This FDC output signal determines which side of the FDD is accessed. Active (low) selects side 1, inactive (high) selects side 0. |
| (PPM Mode) | 79 | 77 | O<br>Group 10 | **Head Select.** This signal provides an additional head select signal in PPM mode when PNF = 0. $\overline{HDSEL}$ is multiplexed with $\overline{ERR}$. See Table 72 for more information. |
| *ID2*<br><br><br>*ID1*<br>*ID0* | *43 or 49*<br><br><br>*8*<br>*68* | *41 or 47*<br><br><br>*6*<br>*66* | *I*<br>*Group 1* | ***Identification –*** *These ID signals identify the infrared transceiver for Plug and Play support. These pins are read after reset. These pins are available only in PC97338.*<br>*ID2 is multiplexed with $\overline{MTR1}$, IDLE and IRSL2 or with $\overline{DRV2}$, PNF, $\overline{DR23}$, SIRQI3 and IRSL2.*<br>*ID1 is multiplexed with IRSL1.*<br>*ID0 is multiplexed with $\overline{DSR2}$, IRQ12, IRRX2 and IRSL0.* |
| IDLE | 43 | 41 | O<br>Group 10 | **Idle.** This FDC output pin is used for an IDLE output signal when bit 4 of PMC is 1. It is used for $\overline{MTR1}$ when bit 4 of PMC is 0. IDLE indicates that the FDC is in the Idle state and can be powered down. Whenever the FDC is in the Idle state, or whenever the FDC is in a power-down state, the pin is active high.<br>IDLE is multiplexed with $\overline{MTR1}$ and IRSL2. |
| $\overline{INDEX}$ (Normal Mode) | 47 | 45 | I<br>Group 4 | **Index.** This input signal indicates the beginning of an FDD track. |
| (PPM Mode) | 94 | 92 | I<br>Group 4 | **FDC Index.** This signal provides an additional index signal in PPM mode when PNF = 0.$\overline{INDEX}$ is multiplexed with PD0. See Table 72 for more information. |
| $\overline{INIT}$ | 80 | 78 | O<br>Group 11 | **Parallel Port Initialize.** When this signal is low, it causes the printer to be initialized. This signal is in a TRI-STATE condition 10 nsec after a 1 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 KΩ resistor.<br>$\overline{INIT}$ is multiplexed with $\overline{DIR}$. |
| IOCHRDY | 53 | 51 | O<br>Group 13 | **I/O Channel Ready.** This is the I/O Channel Ready open-drain output signal. When IOCHRDY is driven low, the EPP extends the host cycle. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| IRQ3<br>IRQ4<br>IRQ5<br>IRQ6<br>IRQ7<br>IRQ9<br>IRQ10<br>IRQ11<br>IRQ12<br>IRQ15<br>(Plug and Play mode) | 1<br>100<br>98<br>97<br>96<br>57<br>58<br>59<br>68<br>60 | 99<br>98<br>96<br>95<br>94<br>55<br>56<br>57<br>66<br>58 | I/O<br>Group 6 | **Interrupts Requests 3, 4, 5, 6, 7, 9, 10, 11, 12 and 15.** These signals are used to request an interrupt from the host processor, when appropriate. These output pins can be configured as totem-pole or open-drain outputs (see below).<br>Any of these interrupt request lines may be assigned to any one of the following: SCC1, SCC2, parallel port, FDC, SIRQI1 signal, SIRQI2 signal, or SIRQI3 signal. For more details, refer to Sections 2 and 6.<br>When the parallel port's interrupt is routed to one of these pins, bit 6 of the PCR determines whether the output signal is totem pole or open drain. Otherwise, they are totem-pole outputs.<br>This pin is I/O only when the parallel port's interrupt is routed to this pin, ECP is enabled and bit 6 of PCR is 1.The Plug and Play mode is determined by bit 3 of PNP0.<br>IRQ5 is multiplexed with ADRATE0.<br>IRQ12 is multiplexed with $\overline{\text{DSR2}}$, IRRX2 and IRSL0.<br>IRQ15 is multiplexed with SIRQI1 and DRQ3. |
| IRQ3<br>IRQ4<br>(Legacy mode) | 1<br>100 | 99<br>98 | O<br>Group 6 | **Interrupts 3 and 4.** These are active high interrupts associated with the serial ports. IRQ3 presents the device interrupt request if the serial channel has been designated as COM2 or COM4. IRQ4 presents the device interrupt request if the serial port is designated as COM1 or COM3.<br>The appropriate interrupt is enabled via IER, the associated Interrupt Enable bit (Modem Control Register (MCR) bit 3), and the interrupt request is actually triggered when one of the following events occur: Receiver Error, Receive Data available, Transmitter Holding Register Empty, or a Modem Status Flag is set.<br>The interrupt request signal becomes inactive (low) after the appropriate interrupt service routine is executed, after being disabled via the IER, or after a Master Reset. Either interrupt can be disabled and put in TRI-STATE by setting bit 3 of the MCR low. |
| IRQ5<br>(Legacy mode) | 98 | 96 | I/O<br>Group 6 | **Interrupt 5.** This active high output signal indicates a parallel port interrupt request. When enabled, this signal follows the $\overline{\text{ACK}}$ signal input. When bit 4 in the parallel port Control Register is set and the parallel port address is designated as shown in Table 11, this interrupt is enabled. When not enabled this signal is TRI-STATE. This pin is I/O only when ECP is enabled, and IRQ5 is configured. |
| IRQ6<br>(Legacy mode) | 97 | 95 | O<br>Group 6 | **Interrupt 6.** This active high output signal indicates an interrupt request upon completion of the execution phase for certain FDC commands. It also signals when a data transfer is ready during a non-DMA operation. In PC-AT or Model 30 mode, this signal is enabled by bit D3 of the DOR. In PS/2 mode, IRQ6 is always enabled, and bit D3 of the DOR is reserved. |
| IRQ7<br>(Legacy mode) | 96 | 94 | I/O<br>Group 6 | **Interrupt 7.** This active high output signal indicates a parallel port interrupt request. When enabled, this signal follows the $\overline{\text{ACK}}$ signal input. When bit 4 in the parallel port Control Register is set and the parallel port address is designated as shown in Table 11, this interrupt is enabled. When not enabled, this signal is in TRI-STATE.<br>This pin is I/O only when ECP is enabled, and IRQ7 is configured. For ECP operation, refer to the interrupt ECP in Section 4.5.5. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| IRRX1<br>IRRX2 | 67<br>68 | 65<br>66 | I<br>Group 1 | **Infrared Received data signals 1 and 2.** Infrared serial data input signals. The infrared Analog Front End (AFE) is expected to send 1 to IRRX if there is no transmission. If it sends 0, the input signal should be inverted by RXINV (bit 4 of register 7, in bank 7 of SCC2 - See Figure 88).<br>IRRX1 is multiplexed with SIN2.<br>IRRX2 is multiplexed with $\overline{\text{DSR2}}$, IRQ12 and IRSL0. |
| IRSL0<br>IRSL1<br>IRSL2 | 68<br>8<br>43 or 49 | 66<br>6<br>41 or 47 | O<br>Group 12 | **Infrared Control signals 0, 1 and 2.** These signals control the infrared Analog Front End (AFE).<br>IRSL0 is multiplexed with $\overline{\text{DSR2}}$, IRQ12, IRRX2 *(and ID0 in PC97338)*.<br>*IRSL1 is multiplexed with ID1 in PC97338.*<br>IRSL2 is multiplexed with either $\overline{\text{DRV2}}$, PNF, $\overline{\text{DR23}}$, SIRQI3 *(and ID2 in PC97338)*, or with $\overline{\text{MTR1}}$, IDLE *(and ID2 in PC97338)*. |
| IRTX | 65 | 63 | O<br>Group 12 | **Infrared Transmitted data.** Infrared serial data output.<br>IRTX is multiplexed with SOUT2, CFG0 (and BOUT2 in PC87338). |
| MR | 2 | 100 | I<br>Group 1 | **Master Reset.** Active high input signal that resets the controller to the idle state. The configuration registers are set to their selected default values. See the reset status for each functional unit. |
| MSEN0<br>MSEN1<br>(Normal Mode) | 52<br>51 | 50<br>49 | I<br>Group 4 | **Media Sense signals 0 and 1.** MSEN0 is selected as a media sense input signal when bit 1 of the FCR register is 0. MSEN1 is selected as a media sense input signal when bits 7 and 6 of the SIRQ2 register are 00.<br>Each pin is internally connected to a 10 KΩ pull-up resistor. When bit 1 of FCR is 1, pin 52 is used as a Data Rate 0 output pin, and the pull-up resistor is disabled.<br>When $\overline{\text{DACK3}}$, DRATE1, $\overline{\text{CS0}}$ or SIRQI2 is selected on the pin, MSEN1 is masked to 1.<br>MSEN0 is multiplexed with DRATE0.<br>MSEN1 is multiplexed with $\overline{\text{DACK3}}$, $\overline{\text{CS0}}$, SIRQI2 and DRATE1. |
| MSEN0<br>MSEN1<br>(PPM Mode) | 88<br>86 | 86<br>84 | I<br>Group 4 | **Media Sense signals 0 and 1.** These signals provide additional media sense signals in PPM mode when PNF = 0.<br>MSEN0 and MSEN1 are multiplexed with PD5 and PD7, respectively. See Table 72 for more information. |
| $\overline{\text{MTR0}}$<br>$\overline{\text{MTR1}}$<br>(Normal Mode) | 46<br>43 | 44<br>41 | O<br>Group 10 | **FDC Motor Select signals 0 and 1.** These motor enable lines for drives 0 and 1 are controlled by bits 7 through 4 of the Digital Output register. They are active low output signals. They are encoded with information to control four FDDs ($\overline{\text{MTR0}}$ exchanges logical motor values with $\overline{\text{MTR1}}$) according to the TDR register settings.<br>Bit 4 of the FCR register is reserved.<br>$\overline{\text{MTR1}}$ is multiplexed with IDLE and IRSL2. |
| $\overline{\text{MTR1}}$<br>(PPM Mode) | 84 | 82 | O<br>Group 10 | **FDC Motor Select 1.** This signal provides an additional motor select 1 signal in PPM mode when PNF = 0. It is active low. This pin is the motor enable line for drive 1 or drive 0, according to the TDR register. Bit 4 of the FCR register is reserved.<br>$\overline{\text{MTR1}}$ is multiplexed with BUSY and $\overline{\text{WAIT}}$. See Table 72 for more information. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| PD | 45 | 43 | O<br>Group 10 | **Power Down.** This pin is used for the FDC Power-Down (PD) output signal when bit 4 of PMC is 1. It is used for $\overline{DR1}$ when bit 4 of PMC is 0. PD is active high whenever the FDC is put into a power-down state by bit 6 of DSR (or bit 3 of FER, or bit 0 of PTR), or by the MODE command.<br>PD is multiplexed with $\overline{DR1}$. |
| PD0<br>PD1<br>PD2<br>PD3<br>PD4<br>PD5<br>PD6<br>PD7 | 94<br>93<br>92<br>91<br>89<br>88<br>87<br>86 | 92<br>91<br>90<br>89<br>87<br>86<br>85<br>84 | I/O<br>Group 1<br>and<br>Group 11 | **Parallel- Port Data signals 0 through 7.** These bidirectional pins transfer data to and from the peripheral data bus and the parallel port Data Register. These pins have high current drive capability. See “Device Description” on page -197.<br>PD7-0 are multiplexed with $\overline{INDEX}$, $\overline{TRK0}$, $\overline{WP}$, $\overline{RDATA}$, $\overline{DSKCHG}$, MSEN0, DRATE0 and MSEN1, respectively. See Table 72 for more information. |
| PE | 83 | 81 | I<br>Group 2 | **Paper End.** This parallel port input signal is set high by the external printer when it is out of paper.<br>This pin is internally grounded by a nominal 25 KΩ pull-down resistor.<br>PE is multiplexed with $\overline{WDATA}$. See Table 72 for more information. |
| PNF | 49 | 47 | I<br>Group 1 | **Printer Not Floppy.** PNF is the Printer Not Floppy signal. It selects the device which is connected to the PPM pins.<br>When a parallel printer is connected, PNF must be set to 1, and when a floppy disk drive is connected, PNF must be set to 0. This pin is configured as PNF when bits 7 and 6 of SIRQ3 are 10.<br>PNF is multiplexed with $\overline{DRV2}$, $\overline{DR23}$, SIRQI3 and IRSL2. |
| $\overline{RD}$ | 19 | 17 | I<br>Group 1 | **Read.** Active low input signal to indicate a data read by the microprocessor. |
| $\overline{RDATA}$<br>(Normal Mode) | 35 | 33 | I<br>Group 4 | **Read Data.** This input signal is the raw serial data read from the floppy disk drive. |
| (PPM Mode) | 91 | 89 | I<br>Group 4 | **Read Data.** This pin provides an additional read data signal in PPM mode when PNF = 0.<br>$\overline{RDATA}$ is multiplexed with PD3. See Table 72 for more information. |
| $\overline{RI1}$<br>$\overline{RI2}$ | 70<br>62 | 68<br>60 | I<br>Group 1 | **Ring Indicators 1 and 2.** When low, these UART signals indicates that a telephone ring signal has been received by the appropriate modem.<br>The $\overline{RI}$ signal is a modem status input signal whose condition can be tested by reading bit 6 (RI) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MSR indicates whether the $\overline{RI}$ input signal has changed from low to high since the previous reading of the MSR.<br>When the TERI bit of MSR is set to 1, an interrupt is generated if modem status interrupts are enabled.<br>$\overline{RI2}$ is multiplexed with A11. When $\overline{RI2}$ is not selected, it is masked to 1. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| $\overline{RTS1}$<br>$\overline{RTS2}$ | 74<br>66 | 72<br>64 | O<br>Group 7 | **Requests to Send 1 and 2.** When low, this output signal indicates to the modem or data transfer device that the appropriate UART is ready to exchange data.<br>The $\overline{RTS}$ signal can be set to active low by programming bit 1 (RTS) of the Modem Control Register (MCR) to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.<br>$\overline{RTS1}$ is multiplexed with BADDR0.<br>$\overline{RTS2}$ is multiplexed with A14. |
| SIN1<br>SIN2 | 75<br>67 | 73<br>65 | I<br>Group 1 | **Serial Input data 1 and 2.** These UART input signals receive composite serial data from the communications link (peripheral device, modem, or data transfer device).<br>SIN2 is multiplexed with IRRX1. |
| SIRQI1<br>SIRQI2<br>SIRQI3 | 60<br>51<br>49 | 58<br>49<br>47 | I<br>Group 1 | **System IRQ Input signals 1, 2 and 3.** These input signals can be routed to one of the following output pins: IRQ7-3 or IRQ12-9. SIRQI2 and SIRQI3 can also be routed to IRQ15. Software configuration determines to which output pin the input signal is routed.<br>SIRQI1 is multiplexed with IRQ15 and DRQ3.<br>SIRQI2 is multiplexed with DRATE1, MSEN1, $\overline{CS0}$ and $\overline{DACK3}$.<br>SIRQI3 is multiplexed with $\overline{DRV2}$, PNF, $\overline{DR23}$ and IRSL2. |
| SLCT | 82 | 80 | I<br>Group 2 | **Select.** This parallel port input signal is set high by the printer when it is selected.<br>This pin is grounded by an internal nominal 25 KΩ pull-down resistor.<br>SLCT is multiplexed with $\overline{WGATE}$. |
| $\overline{SLIN}$ | 81 | 79 | I/O<br>Group 11 | **Select Input.** When this parallel port signal is low, it selects the external printer. This signal enters TRI-STATE within 10 nsec after a 0 is loaded into the corresponding Control Register bit.<br>An external 4.7 KΩ pull-up resistor to $V_{CC}$ must be connected to this pin.<br>$\overline{SLIN}$ is multiplexed with $\overline{ASTRB}$, $\overline{STEP}$. See Table 72 for more information. |
| SOUT1<br>SOUT2 | 73<br>65 | 71<br>63 | O<br>Group 7 | **Serial Output signals 1 and 2** These UART output signals send composite serial data to the communications link (peripheral device, modem, or data transfer device). The SOUT signal is set to a marking state (logic 1) after a Master Reset operation.<br>SOUT1 is multiplexed with BADDR1 (and BOUT1 in PC87338).<br>SOUT2 is multiplexed with IRTX, CFG0 (and BOUT2 in PC87338). |
| $\overline{STB}$ | 95 | 93 | I/O<br>Group 11 | **Strobe.** This output signal indicates to the printer that valid data is available at the parallel port. This pin enters TRI-STATE within 10 nsec after a 0 is loaded into the corresponding Control Register bit.<br>An external 4.7 KΩ pull-up resistor to $V_{CC}$ must be connected to this pin.<br>$\overline{STB}$ is multiplexed with $\overline{WRITE}$. See Table 72 for more information. |
| $\overline{STEP}$<br>(Normal Mode) | 40 | 38 | O<br>Group 10 | **Step.** This FDC output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| (PPM Mode) | 81 | 79 | O Group 10 | **Step.** This pin provides an additional step signal in PPM mode when PNF = 0. $\overline{STEP}$ is multiplexed with $\overline{SLIN}$ and $\overline{ASTRB}$. See Table 72 for more information. |
| TC | 6 | 4 | I Group 1 | **Terminal Count.** This control signal from the DMA controller indicates the termination of a DMA block transfer. TC is accepted by the module (FDC, parallel port or SCC2) only when the corresponding DMA acknowledge signal ($\overline{DACK0}$, $\overline{DACK1}$, $\overline{DACK2}$ or $\overline{DACK3}$, according to software configuration) is active. TC is active high in PC-AT mode, and active low in PS/2 mode. |
| $\overline{TRK0}$ (Normal Mode) | 37 | 35 | I Group 4 | **Track 0.** This FDC input indicates to the controller that the head of the selected floppy disk drive is at track zero. |
| (PPM Mode) | 93 | 91 | I Group 4 | **Track 0.** This pin provides an additional Track 0 signal in PPM Mode when PNF = 0. $\overline{TRK0}$ is multiplexed with PD1 (See Table 72 for more information). |
| VDD | 50<br>99 | 48,<br>97 | I | **Power Supply signals.** These pins input the 3.3 V or 5 V supply voltage to the ChipVLJ and ChipVJG device. |
| VSS | 42<br>9<br>90<br>61 | 40<br>7<br>88<br>59 | O | **Ground signals.** These pins ground the ChipVLJ and ChipVJG circuitry. |
| $\overline{WAIT}$ | 84 | 82 | I Group 1 | **Wait.** This signal is used in EPP mode, by the parallel port device, to extend its access cycle. It is active low. $\overline{WAIT}$ is multiplexed with BUSY and $\overline{MTR1}$. See Table 72 for more information. |
| $\overline{WDATA}$ (Normal Mode) | 39 | 37 | O Group 10 | **FDC Write Data.** This FDC output signal is the write precompensated serial data that is written to the selected floppy disk drive. Precompensation is software selectable. |
| (PPM Mode) | 83 | 81 | O Group 10 | **FDC Write Data.** This pin provides an additional $\overline{WDATA}$ signal in PPM mode when PNF = 0. $\overline{WDATA}$ is multiplexed with PE. See Table 72 for more information. |
| $\overline{WGATE}$ (Normal Mode) | 38 | 36 | O Group 10 | **FDC Write Gate.** This FDC output signal enables the write circuitry of the selected disk drive. $\overline{WGATE}$ is designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled. |
| (PPM Mode) | 82 | 80 | O Group 10 | **FDC Write Gate.** This pin provides an additional $\overline{WGATE}$ signal in PPM mode, when PNF = 0. $\overline{WGATE}$ is multiplexed with SLCT. See Table 72 for more information. |
| $\overline{WP}$ (Normal Mode) | 36 | 34 | I Group 4 | **Write Protect.** This FDC input indicates that the disk in the selected drive is write protected. |
| (PPM Mode) | 92 | 90 | I Group 4 | **Write Protect.** This pin provides an additional $\overline{WP}$ signal in PPM mode, when PNF = 0. $\overline{WP}$ is multiplexed with PD2. See Table 72 for more information. |

| Symbol | PQFP Pin | TQFP Pin | I/O and Group # | Function |
|---|---|---|---|---|
| $\overline{WR}$ | 18 | 16 | I<br>Group 1 | **Write.** This active low input signal indicates a write from the microprocessor to the Chip. |
| $\overline{WRITE}$ | 95 | 93 | O<br>Group 11 | **Write Strobe.** This signal is used in EPP mode as write strobe. It is active low. $\overline{WRITE}$ is multiplexed with $\overline{STB}$. See Table 72 for more information. |
| X1 | 7 | 5 | I<br>Group 5 | **Clock.** Active clock input signal of 14.318 MHz, 24 MHz or 48 MHz. |
| $\overline{ZWS}$ | 3 | 1 | O<br>Group 13 | **Zero Wait State.** This pin is used for the Zero Wait State open-drain output signal, when bit 6 of FCR is 0. $\overline{ZWS}$ is driven low when the EPP or ECP is written to, and the access time can be shortened. This pin is $\overline{CS1}$ when bit 6 of FCR is 1.<br>$\overline{ZWS}$ is multiplexed with the $\overline{CS1}$. |

**TABLE 2. Multi-Function Pins (Excluding Strap Pins)**

| PQFP Pin | TQFP Pin | Symbols |
|---|---|---|
| 3 | 1 | $\overline{CS1}$/$\overline{ZWS}$ |
| *8* | *6* | *IRSL1/ID1 (in PC97338)* |
| 43 | 41 | $\overline{MTR1}$/IDLE/IRSL2 *(and ID2 in PC97338)* |
| 45 | 43 | $\overline{DR1}$/PD |
| 48 | 46 | DENSEL/ADRATE1 |
| 49 | 47 | $\overline{DRV2}$/PNF/$\overline{DR23}$/SIRQI3/IRSL2 *(and ID2 in PC97338)* |
| 51 | 49 | DRATE1/MSEN1/$\overline{CS0}$/SIRQI2/$\overline{DACK3}$ |
| 52 | 50 | DRATE0/MSEN0 |
| 60 | 58 | IRQ15/SIRQI1/DRQ3 |
| 62 | 60 | $\overline{RI2}$/A11 |
| 63 | 61 | $\overline{DTR2}$/A12 *(and BOUT2 in PC97338)* |
| 64 | 62 | $\overline{CTS2}$/A13 |
| 65 | 63 | SOUT2/IRTX |
| 66 | 64 | $\overline{RTS2}$/A14 |
| 67 | 65 | SIN2/IRRX1 |
| 68 | 66 | $\overline{DSR2}$/IRQ12/IRRX2/IRSL0 *(and ID0 in PC97338)* |
| 69 | 67 | $\overline{DCD2}$/A15 |
| *71* | *69* | *$\overline{DTR1}$/BOUT1 (Only in PC97338)* |
| 73 | 71 | SOUT1/BOUT1 (Only in PC87338) |
| 78 | 76 | $\overline{AFD}$/$\overline{DSTRB}$/DENSEL(PPM) |
| 79 | 77 | $\overline{ERR}$/$\overline{HDSEL}$(PPM) |
| 80 | 78 | $\overline{INIT}$/$\overline{DIR}$(PPM) |
| 81 | 79 | $\overline{SLIN}$/$\overline{STEP}$(PPM)/$\overline{ASTRB}$ |
| 82 | 80 | SLCT/$\overline{WGATE}$(PPM) |
| 83 | 81 | PE/$\overline{WDATA}$(PPM) |
| 84 | 82 | BUSY/$\overline{WAIT}$/$\overline{MTR1}$(PPM) |
| 85 | 83 | $\overline{ACK}$/$\overline{DR1}$(PPM) |
| 86 | 84 | PD7/MSEN1(PPM) |
| 87 | 85 | PD6/DRATE0(PPM) |
| 88 | 86 | PD5/MSEN0(PPM) |
| 89 | 87 | PD4/$\overline{DSKCHG}$(PPM) |
| 91 | 89 | PD3/$\overline{RDATA}$(PPM) |
| 92 | 90 | PD2/$\overline{WP}$(PPM) |
| 93 | 91 | PD1/$\overline{TRK0}$(PPM) |
| 94 | 92 | PD0/$\overline{INDEX}$(PPM) |
| 95 | 93 | $\overline{STB}$/$\overline{WRITE}$ |
| 98 | 96 | IRQ5/ADRATE0 |

**TABLE 3. IRQ12, A15-11 / SCC2 / Infrared Pin Allocation**

| PQFP Pin | TQFP Pin | Reset Value of CFG0 is 0 | Reset Value of CFG0 is 1 |
|---|---|---|---|
| 62 | 60 | Function: A11<br>others: $\overline{RI2}$ = 1 | Function: $\overline{RI2}$<br>Others: A11 = 0 |
| 63 | 61 | Function: A12 | Function: $\overline{DTR2}$/*BOUT2*[a]<br>Others: A12 = 0 |
| 64 | 62 | Function: A13<br>Others: $\overline{CTS2}$ = 0 | Function: $\overline{CTS2}$<br>Others: A13 = 0 |
| 66 | 64 | Function: A14 | Function: $\overline{RTS2}$<br>Others: A14 = 0 |
| 69 | 67 | Function: A15<br>Others: $\overline{DCD2}$ = 1 | Function: $\overline{DCD2}$<br>Others: A15 = 0 |

*a. $\overline{DTR2}$ or BOUT2 is selected on the pin via the SCC2 registers in PC97338 only. See Section 5.*

**TABLE 4. SCC2 Mode Configurations 1**

| Pin | | Wake Up | | Run-Time Selection[a] | |
|---|---|---|---|---|---|
| PQFP | TQFP | Reset Value of CFG0 is 0 | Reset Value of CFG0 is 1 | InfraRed Mode Selected | UART Mode Selected |
| 65 | 63 | Function: IRTX | Function: SOUT2/BOUT2[b] | Function: IRTX | Function: SOUT2/BOUT2[b] |
| 67 | 65 | Function: IRRX1 | Function: SIN2 | Function: IRRX1 | Function: SIN2 |

a. Run time selection is via the SCC2 registers (see Section 5). If the reset value of CFG0 is 0, run time selection is disabled after reset. To enable run time selection, configure the SCC2 to any infra-red mode. Once this is done, run time selection is enabled. If the reset value of CFG0 is 1, run time selection is enabled immediately after reset.

b. SOUT2 or BOUT2 is selected on the pin via SCC2 registers in PC87338 only. See Section 5.

**TABLE 5. SCC2 Mode Configurations 2**

| Pin | | Wake Up | | Run-Time Selection | | | |
|---|---|---|---|---|---|---|---|
| | | | | Reset Value of CFG0 is 0 | | Reset Value of CFG0 is 1 | |
| PQFP | TQFP | Reset Value of CFG0 = 0 | Reset Value of CFG0 = 1 | Bit 3 of SCF3 = 0 | Bit 3 of SCF3 = 1 | InfraRed Mode Selected | UART Mode Selected |
| 68 | 66 | Function: IRQ12<br>Others: $\overline{DSR2}$ = 0 | Function: $\overline{DSR2}$ | Function: IRQ12<br>Others: $\overline{DSR2}$ = 0 | Function: IRRX2/IRSL0/*ID0*[a]<br>Others: $\overline{DSR2}$ = 0 | Function: IRRX2/IRSL0/*ID0*[a]<br>Others: $\overline{DSR2}$ = 0 | Function: $\overline{DSR2}$ |

a. IRRX2 or IRSL0/*ID0* is selected on the pin via the SCC2 registers. *ID0 is available only in PC97338*. See Section 5.

# 2.0 Configuration

## 2.1 OVERVIEW

The configuration register set consists of 37 registers, which control the Chip set-up. Setup values stored in these registers enable or disable major functions, such as FDC, SCCs and the parallel port, and set functional parameters such as functional mode selection, pin functionality, interrupt configuration, hardware-controlled power down options and I/O address assignment.

Table 7 lists these registers, their mnemonic abbreviations and index number (which serves as an address offset). Bitmaps of these registers, in order of increasing index numbers, appear in Section 2.3.1 on page 41.

## 2.2 CONFIGURATION REGISTER SETUP

Certain configuration registers are setup by hardware pin strapping schemes. All others are setup by software. The hardware-configured registers may be updated by software after power-up.

### 2.2.1 Hardware Device Configuration

Three configuration registers in the Chip are setup by hardware pin strapping options. The FER, FAR and PTR register default contents are setup by CFG0 during reset.

CFG0 is set to 0 level by default, and may be changed to logical 1 by attaching an external pull-up resistor. The values set by this method are loaded into the device registers during reset. The setting of this pin selects one of two sets of default values for loading. This enables automatic configuration without software intervention.

Table 6 shows the hardware-controlled default configurations.

CFG0 controls selection of 11 address bits with fully standard interface of SCC2, or 16 address bits and SCC2 with SIN and SOUT signals only.

- 11-bit address mode - The chip is in this mode, if during reset CFG0 = 1. SCC2 wakes up with the full standard interface.
- 16-bit address mode - The chip is in this mode, if during reset CFG0 = 0. SCC2 wakes up in 16550 UART/SIR mode.

The default configuration can be modified by software at any time after reset by using the access procedure described in the Section 2.2.

**TABLE 6. Default Configurations Controlled by Hardware**

| CFG0 | Reset Value of FAR, FER, PTR | Reset Configuration |
|---|---|---|
| 0(Default) | FER = $xx000000_B$<br>PTR = $00x000x0_B$<br>FAR = $00010000_B$ | • All modules disabled (power down)<br>• 16 address bits.<br>• SCC2 in Legacy SIR mode, with SIN and SOUT signals only. |
| 1 | | • All modules disabled (power down).<br>• 11 address bits.<br>• SCC2 in Legacy mode, with the full standard interface. |

**TABLE 7. Configuration Registers**

| Symbol | Description | Index | HW Cfg | Modules Affected | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | FDC | PP | S1 | S2 | IR | CS | CFG |
| ASC | Advanced SuperI/O Chip Configuration | 09h | | x | x | | | | | |
| CLK | Clock Control | 51h | | | | | | | | x |
| CS0CF | Chip Select 0 Configuration | 0Bh | | | | | | | x | |
| CS0HA | Chip Select 0 Base Address, High | 10h | | | | | | | x | |
| CS0LA | Chip Select 0 Base Address, Low | 0Ah | | | | | | | x | |
| CS1CF | Chip Select 1 Configuration | 0Dh | | | | | | | x | |
| CS1HA | Chip Select 1 Base Address, High | 11h | | | | | | | x | |
| CS1LA | Chip Select 1 Base Address, Low | 0Ch | | | | | | | x | |
| FAR | Function Address Register | 01h | x | | x | x | x | | | |
| FBAH | FDC Base Address, High | 49h | | x | | | | | | |
| FBAL | FDC Base Address, Low | 48h | | x | | | | | | |
| FCR | Function Control Register | 03h | | x | x | | | | x | x |
| FER | Function Enable Register | 00h | x | x | x | x | x | | | |
| PBAH | Parallel port Base Address, High | 43h | | | x | | | | | |
| PBAL | Parallel port Base Address, Low | 42h | | | x | | | | | |
| PCR | Parallel port Control Register | 04h | | | x | | | | | |
| PMC | Power Management Control | 06h | | x | x | x | | | | x |
| PNP0 | Plug and Play Configuration 0 | 1Bh | | x | x | x | x | | | x |
| PNP1 | Plug and Play Configuration 1 | 1Ch | | | | x | x | | | |
| PNP2 | Plug and Play Configuration 2 | 41h | | x | | | | | | |
| PNP3 | Plug and Play Configuration 3 | 4Fh | | | | | x | x | | |
| PTR | Power and Test Register | 02h | x | | x | x | x | | | |
| SBAH | SuperI/O chip Base Address, High | 4Bh | | | | | | | | x |
| SBAL | SuperI/O chip Base Address, Low | 4Ah | | | | | | | | x |
| SCF0 | SuperI/O chip Configuration 0 | 12h | | | | | x | | | |
| SCF1 | SuperI/O chip Configuration 1 | 18h | | | x | | | | | |
| SCF2 | SuperI/O chip Configuration 2 | 40h | | x | | | x | x | | |
| SCF3 | SuperI/O chip Configuration 3 | 50h | | x | x | | x | x | | x |
| SID | SuperI/O chip Identification | 08h | | | | | | | | x |
| SIRQ1 | System IRQ Input 1 Configuration | 4Ch | | | | | | | | x |
| SIRQ2 | System IRQ Input 2 Configuration | 4Dh | | x | | | | | x | x |
| SIRQ3 | System IRQ input 3 configuration | 4Eh | | x | x | | | | | x |
| TUP | Tape, UART and Parallel Port Configuration | 07h | | x | x | x | | | | x |
| S1BAH | SCC1 Base Address, High | 45h | | | | x | | | | |
| S1BAL | SCC1 Base Address, Low | 44h | | | | x | | | | |
| S2BAH | SCC2 Base Address, High | 47h | | | | | x | | | |
| S2BAL | SCC2 Base Address, Low | 46h | | | | | x | | | |

### 2.2.2 Software Device Configuration

Besides the three hardware-configured registers, all Legacy-mode access to the configuration registers is achieved by the use of an INDEX and DATA register pair. Each configuration register is indicated by the value loaded into the INDEX register. The data to be written into or read from the indicated configuration register is transferred via the DATA register.

Accessing the configuration registers in this way requires only two system I/O addresses. These two addresses are configured by strapping the values of pins BADDR0 and BADDR1 during reset, as described in Table 8. Since that I/O space is shared by other devices the INDEX and DATA registers may conflict with other system devices constrained to use this I/O address space. Such conflicts may be resolved by changing the INDEX and DATA register address assignments after reset, as described in Section 2.2.5.

**TABLE 8. INDEX and DATA Register Address Options and Configuration Register Accessibility**

| BADDR Pin | | INDEX Register Address | DATA Register Address | Accessible after Reset |
|---|---|---|---|---|
| 1 | 0 | | | |
| 0 | 0 | 398h | 399h | Yes |
| 0 | 1 | undefined | undefined | No[a] |
| 1 | 0 | 15Ch | 15Dh | Yes |
| 1 | 1 | 2Eh | 2Fh | Yes |

a. Apply Plug and Play protocol.

### 2.2.3 Updating Configuration Registers

The settings of the configuration registers are accessible via the INDEX and DATA registers. The location of these registers is set by hardware during reset, and the software is not informed of the chosen hardware setting. The first step required to change configuration registers settings is, to locate the addresses of the INDEX and DATA registers.

To access the configuration registers after reset, use the following procedure.

1. Determine the location of the INDEX register.

   Check the possible locations (see Table 8) by reading them twice. At the correct location only, the first byte to return will be 88h, and the second will be 00h. This double read must be conducted before any writes have been made to the addresses being checked since the ID byte is only issued from the Index register during the first read after a reset. (The register is reset by read. Subsequent reads return the value loaded into the Index register (except bits 6-4 which are reserved and always read 0), or 00h if no write has been made).

2. Load the configuration registers.
   A. Disable CPU interrupts (only for the PC87338).
   B. Write the index of the configuration register (00h-0Eh) to the INDEX register.
   C. Write the correct data for the configuration register to the DATA register (*one write access in the PC97338* and two consecutive write accesses in the PC87338).
   D. Enable CPU interrupts (only for the PC87338).
3. Load the configuration registers (read-modify-write).
   A. Disable CPU interrupts (only for the PC87338).
   B. Write the index of the configuration register (00h-0Eh) to the INDEX register.
   C. Read the configuration data in that register via the DATA register.
   D. Modify the configuration data.
   E. Write the changed data for the configuration register to the DATA register (*one write access in the PC97338* and two consecutive write accesses in the PC87338).
   F. Enable CPU interrupts (only for the PC87338).

A single read access to the INDEX and DATA registers can be done at any time without disabling CPU interrupts. Reading the INDEX register returns the last value loaded into the INDEX register. Reading the DATA register returns the configuration register data pointed to by the INDEX register.

If during reset BADDR1 = 0 and BADDR0 = 1, the INDEX and DATA register addresses are determined after reset via the Plug and Play protocol. As long as these addresses are undefined, the configuration registers are not accessible. See Table 8.

### 2.2.4 Reserved Bits in Configuration Registers

To maintain compatibility with future SuperI/O chips, do not modify reserved bits when the register is written, i.e., use read-modify-write to preserve the value of reserved bits.

### 2.2.5 INDEX and DATA Register Locations

During reset, the INDEX and DATA register pair can be located at one of three locations by a hardware strapping option on two pins (BADDR0 and BADDR1) (see Table 8). This enables resolution of conflicts with other devices in the I/O address space.

For all reset values of BADDR0,1, the INDEX and DATA register pair can always be relocated via configuration registers SBAL and SBAH. See “Relocating the INDEX and DATA Register Pair” on page 40.

The INDEX register address is always even. The DATA register is always at the next consecutive address. Bit 7 of the INDEX register is reserved, and is always read 0.

### 2.2.6 Plug and Play Protocol

The following protocol is based on the Plug and Play ISA Specification 1.0a. It should be applied on power-up, if during reset BADDR1 = 0 and BADDR0 = 1. It is not applicable otherwise. For any other reset values of BADDR0,1, the hardware does not respond.

This protocol is used to determine the addresses of the INDEX and DATA registers. When the protocol is applied, the CPU interrupts should be disabled.

Upon power up, an initiation key must be written to one of the following I/O ports: 279h, 3BDh or 3F0h. The initiation key consists of a predefined series of write operations. All of the write operations in the series must be to the same port. These ports are write only. The ports are chosen so as to avoid conflicts in the installed base of ISA functions. (These ports serve as read-only registers in legacy devices.) The write sequence is decoded by the Chip.

If the proper series of I/O writes is detected, the configuration of the Chip base address (address of the Index register) follows. The base address of the Chip is configured by two additional I/O writes to the chosen I/O port (the same I/O port to which the initiation key was written). The data in the first write holds the eight high address bits of the Chip base address. The data in the second write holds the eight low address bits of the Chip base address. Once these two I/O writes are accomplished, the INDEX and DATA registers are accessible and the Chip is configurable.

Since this protocol is based on the Plug and Play ISA Specification 1.0a, software should conclude this protocol with a sequence of two write cycles of 0x00 to the chosen I/O port. Once the Plug and Play protocol is concluded, it can not be applied again until a hardware reset is asserted. CPU interrupts can be enabled at this point. The addresses of the INDEX and DATA registers are still reconfigurable, via the SBAL and SBAH configuration registers, as explained in the Section “Relocating the INDEX and DATA Register Pair” on page 40.

The hardware check of the initiation key is implemented as a linear feedback shift register (LFSR). See “The Linear Feedback Shift Register (LFSR)” on page 40. Software generates the LFSR sequence and writes it to one of the three I/O ports defined above as a sequence of 8-bit write cycles (all writes are to the same I/O port). Hardware compares the byte of write data with the value in the shift register at each write. When the data does not match, the hardware resets to the initial value of the LFSR. Software should reset the LFSR to its initial value using a sequence of two write cycles of 0x00 to the chosen port (one of the three I/O ports) before the initiation key is sent.

Figure 1 shows the flowchart of the Plug and Play protocol.

**FIGURE 1. Plug and Play Protocol Flowchart**

## The Linear Feedback Shift Register (LFSR)

The LFSR is an 8-bit shift register that resets to the value of 0x6A. (See Figure 2.) The feedback taps for this shift register are taken from register bits 1 and 0 of LFSR.

The initiation key should be sent to the Chip upon power on. The software should ensure that the LFSR is in its initial state. Then 32 writes are performed. The first 30 writes must be exactly equal to the 30 values the LFSR will generate starting from 0x6A. The last two writes are of 0x00.

The exact sequence for the initiation key in hexadecimal notation is (reading left to right, top to bottom):

6A, B5, DA, ED, F6, FB, 7D, BE,
DF, 6F, 37, 1B, 0D, 86, C3, 61,
B0, 58, 2C, 16, 8B, 45, A2, D1,
E8, 74, 3A, 9D, CE, E7, 00, 00

**FIGURE 2. LFSR Circuit**

## Relocating the INDEX and DATA Register Pair

The INDEX and DATA registers are relocated via configuration registers SBAL and SBAH, as follows:

1. Write to the SBAH register.

   A temporary register (TEMP_SBAH) is updated with the written data (as in all configuration registers). SBAH register is not updated yet with the written data, i.e., a read from SBAH register will return the data prior to the write.

   The addresses of the INDEX and DATA registers are not modified.

2. Write to the SBAL register.

   The second consecutive write updates the SBAL register with the written data and updates the SBAH register with the data stored in the temporary register (TEMP_SBAH).

   The addresses of the INDEX and DATA registers are modified according to the data of SBAL and SBAH.

3. Return to (1) if addresses of the INDEX and DATA registers need to be changed again.

Upon reset, TEMP_SBAH is initialized to the initialization value of the SBAH register. When the SBAH register is updated by the Plug and Play protocol, TEMP_SBAH is updated too, with the same value.

This scheme maintains the coherence of the INDEX and DATA register addresses.

## 2.3 THE CONFIGURATION REGISTERS

The next section presents the bitmaps of the configuration registers in address order. The sections that follow describe the bits and fields of each register in detail, in the same order.

“Reset” specifies the value of a bit after reset. “Required” indicates that the bit must always have that value.

To maintain compatibility with other SuperI/O chips, the value of reserved bits may not be altered. Use read-modify-write to preserve their values.

### 2.3.1 Configuration Register Bitmaps

**Function Enable Register (FER) Index 00h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- Parallel Port Enable
- SCC1 Enable
- SCC2 Enable
- FDC Enable
- FDC Four-Drive Encoding
- Select FDC Secondary Address
- Reserved
- Reserved

**Function Address Register (FAR) Index 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | x | 0 | 0 | 0 | x | 0 | Reset |
| | | | | | | | | Required |

- Parallel Port Address
- SCC1 Address
- SCC2 Address
- Select COM3 or COM4

**Power and Test Register (PTR) Index 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- Power Down
- Reserved
- Reserved
- Select IRQ5 or IRQ7
- SCC1 Test Mode
- Reserved
- Lock Configuration
- Select Extended or Compatible Parallel Port

**Function Control Register (FCR) Index 03h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Reset |
| | | | 0 | | 0 | | | Required |

- TDR Mode Select
- Select MSEN0 or DRATE0
- Reserved
- Parallel Port Float Control
- Reserved
- Zero Wait State Enable
- Select $\overline{ZWS}$ or $\overline{CS1}$
- Clock Multiplier Test Bit

**Parallel Port Control Register (PCR) Index 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | 0 | | | | | Required |

- EPP Enable
- EPP Version Select
- ECP Enable
- ECP Clock Freeze
- Reserved
- Parallel Port Interrupt I/O Control
- Parallel Port Open-Drain Control
- Reserved

**Power Management Control Register (PMC) Index 06h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- Reserved
- FDC TRI-STATE Control
- SCC1 TRI-STATE Control
- Reserved
- PD and IDLE or IRSL2/*ID2* Enable
- Selective Lock
- PPM TRI-STATE Enable
- Reserved

**Tape, SCCs and Parallel Port Configuration Register (TUP) Index 07h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | | | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- Reserved
- FDC 2 Mbps Enable
- EPP Time-Out Interrupt Enable
- *Reserved*(PC97338) / MIDI(PC87338)
- Reserved
- PD Status
- IDLE Status
- IDLE Pin Mask

**SuperI/O Chip Identification Register (SID) Index 08h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | x | x | x | Reset |
| 1 | 0 | 1 | 1 | 0 | x | x | x | Required |

- D0
- D1
- D2
- D3
- D4
- D5
- D6
- D7

**Advanced SuperI/O Chip Configuration Register (ASC) Index 09h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | x | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- 0: Select IRQ5 or ADRATE0
- 1: Reserved
- 2: Enhanced TDR Support
- 3: PNF Status
- 4: Select DENSEL or ADRATE1
- 5: ECP CNFGA Bit
- 6: DENSEL Polarity Select
- 7: System Operation Mode

**Chip Select 0 Low Address Register (CS0LA) Index 0Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

- 0: A0
- 1: A1
- 2: A2
- 3: A3
- 4: A4
- 5: A5
- 6: A6
- 7: A7

**Chip Select 0 Configuration Register (CS0CF) Index 0Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- 0: Reserved
- 1: Reserved
- 2: Reserved
- 3: Number of Decoded Address Bits
- 4: $\overline{CS0}$ Assert Enable (Write)
- 5: $\overline{CS0}$ Assert Enable (Read)
- 6: Reserved
- 7: Reserved

**Chip Select 1 Low Address Register (CS1LA) Index 0Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

- 0: A0
- 1: A1
- 2: A2
- 3: A3
- 4: A4
- 5: A5
- 6: A6
- 7: A7

**Chip Select 1 Configuration Register (CS1CF) Index 0Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- 0: Reserved
- 1: Reserved
- 2: Reserved
- 3: Number of Decoded Address Bits
- 4: $\overline{CS1}$ Assert Enable (Write)
- 5: $\overline{CS1}$ Assert Enable (Read)
- 6: Reserved
- 7: Reserved

**Chip Select 0 High Address Register (CS0HA) Index 10h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

| Address Length | |
|---|---|
| **CFG0 = 1 11 Bits** | **CFG0 = 0 16 bits** |
| A8 | A8 |
| A9 | A9 |
| A10 | A10 |
| Reserved | A11 |
| Reserved | A12 |
| Reserved | A13 |
| Reserved | A14 |
| Reserved | A15 |

**Chip Select 1 High Address Register (CS1HA) Index 11h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

| Address Length | |
|---|---|
| **CFG0 = 1 11 Bits** | **CFG0 = 0 16 bits** |
| A8 | A8 |
| A9 | A9 |
| A10 | A10 |
| Reserved | A11 |
| Reserved | A12 |
| Reserved | A13 |
| Reserved | A14 |
| Reserved | A15 |

**SuperI/O Chip Configuration Register 0 (SCF0) Index 12h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | x | x | 0 | x | x | x | Reset |
| | | | | | | | | Required |

- 0: Reserved
- 1: Reserved
- 2: Reserved
- 3: UART TRI-STATE Control
- 4: Reserved
- 5: Reserved
- 6: Reserved
- 7: Reserved

**SuperI/O Chip Configuration Register 1 (SCF1) Index 18h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | 0 | 0 | 0 | 0 | 0 | x | Reset |
| | | | | | | | | Required |

- Reserved
- ECP DMA Number
- Parallel Port DMA Plug and Play Support
- Reserved
- Reserved

**Plug and Play Configuration Register 2 (PNP2) Index 41h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- FDC Interrupt Mapping
- FDC DMA Plug-and-Play Support
- Reserved

**Plug and Play Configuration Register 0 (PNP0) Index 1Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | x | x | x | Reset |
| | | | | | | | | Required |

- Parallel Port IRQ Select
- Legacy/Plug-and Play Mode
- Parallel Port Interrupt Mapping

**Parallel Port Base Address Low Byte Register (PBAL) Index 42h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

- A2
- A3
- A4
- A5
- A6
- A7
- A8
- A9

**Plug and Play Configuration Register 1 (PNP1) Index 1Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- SCC1 Interrupt Mapping
- SCC2 Interrupt Mapping

**Parallel Port Base Address High Byte Register (PBAH) Index 43h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

| Address Length | |
|---|---|
| **CFG0 = 1 11 Bits** | **CFG0 = 0 16 bits** |
| Reserved | Reserved |
| Reserved | Reserved |
| A10 | A10 |
| Reserved | A11 |
| Reserved | A12 |
| Reserved | A13 |
| Reserved | A14 |
| Reserved | A15 |

**SuperI/O Chip Configuration Register 2 (SCF2) Index 40h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

- VLD1,0
- Reserved
- Reserved
- SCC1 Bank Select Enable
- SCC2 Normal Power Mode
- SCC2 is Busy
- SCC2 Bank Select Enable

**SCC1 Base Address Low Byte Register (S1BAL) Index 44h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

- Reserved
- A3
- A4
- A5
- A6
- A7
- A8
- A9

**SCC1 Base Address High Byte Register (S1BAH) Index 45h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

| Address Length CFG0 = 1 11 Bits | CFG0 = 0 16 bits |
|---|---|
| Reserved | Reserved |
| Reserved | Reserved |
| A10 | A10 |
| Reserved | A11 |
| Reserved | A12 |
| Reserved | A13 |
| Reserved | A14 |
| Reserved | A15 |

**FDC Base Address High Byte Register (FBAH) Index 49h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

| Address Length CFG0 = 1 11 Bits | CFG0 = 0 16 bits |
|---|---|
| Reserved | Reserved |
| Reserved | Reserved |
| A10 | A10 |
| Reserved | A11 |
| Reserved | A12 |
| Reserved | A13 |
| Reserved | A14 |
| Reserved | A15 |

**SCC2 Base Address Low Byte Register (S2BAL) Index 46h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

Reserved
A3
A4
A5
A6
A7
A8
A9

**SuperI/O Chip Base Address Low Byte Register (SBAL) Index 4Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

Reserved
A1
A2
A3
A4
A5
A6
A7

**SCC2 Base Address High Byte Register (S2BAH) Index 47h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

| Address Length CFG0 = 1 11 Bits | CFG0 = 0 16 bits |
|---|---|
| Reserved | Reserved |
| Reserved | Reserved |
| A10 | A10 |
| Reserved | A11 |
| Reserved | A12 |
| Reserved | A13 |
| Reserved | A14 |
| Reserved | A15 |

**SuperI/O Chip Base Address High Byte Register (SBAH) Index 4Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

| Address Length CFG0 = 1 11 Bits | CFG0 = 0 16 bits |
|---|---|
| A8 | A8 |
| A9 | A9 |
| A10 | A10 |
| Reserved | A11 |
| Reserved | A12 |
| Reserved | A13 |
| Reserved | A14 |
| Reserved | A15 |

**FDC Base Address Low Byte Register (FBAL) Index 48h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

Reserved
A3
A4
A5
A6
A7
A8
A9

**System IRQ Input 1 Configuration Register (SIRQ1) Index 4Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | 0 | x | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

SIRQI1 Mapping
Invert SIRQI1
SIRQI1 Status
Select IRQ15, SIRQI1 or DRQ3

## 2.3.2 Function Enable Register (FER), Index 00h

This register enables and disables major chip functions. Disabled functions have their clocks automatically powered down, but the data in their registers remains intact. It also selects whether the FDC controller is located at the primary or secondary address.

**FIGURE 3. FER Register Bitmap**

**Bit 0 - Parallel Port Enable**

0 - The parallel port is disabled.

1 - The parallel port can be accessed at the address specified by: In Legacy mode: the FAR bits 1,0. In Plug and Play mode: by PBAL and PBAH registers.

**Bit 1- SCC1 Enable**

This bit enables or disables SCC1.

Any SCC1 interrupt that is enabled and active, or becomes active after SCC1 is disabled, asserts the associated IRQ pin when SCC1 is disabled. If disabling SCC1 via software, clear ISEN bit (see sec. 5.14.5 on page 159) to 0 before clearing FER bit 1. This is not an issue after reset because ISEN is 0 until it is written.

0 - Access to SCC1 is blocked and it is in power down mode. The SCC1 registers retain all data in power down mode.

1 - In Legacy mode, SCC1 can be accessed at the address specified by bits 3,2 of the FAR. In Plug and Play mode, the address is specified the by S1BAL and S1BAH registers.

**Bit 2 - SCC2 Enable**

This bit enables SCC2. Any SCC2 interrupt that is enabled and active or becomes active after SCC2 is disabled asserts the associated IRQ pin when SCC2 is disabled. If disabling SCC2 via software, clear ISEN bit (see sec. 5.14.5 on page 159) to 0 before clearing FER bit 2. This is not an issue after reset because ISEN is 0 until it is written.

0 - Access to SCC2 is blocked and it is in power down mode. The SCC2 registers retain all data in power down mode.

1 - In Legacy mode, SCC2 can be accessed at the address specified by bits 5,4 of the FAR. In Plug and Play mode, the address is specified by the S2BAL and S2BAH registers.

**Bit 3 - FDC Enable**

This bit enables the FDC

0 - Access to the FDC is blocked and it is in power down mode. The FDC registers retain all data in power down mode.

1 - FDC can be accessed at the address specified by bit 5 of FER in Legacy mode, and by the FBAL and FBAH registers in Plug and Play mode.

**Bit 4 - FDC Four-Drive Encoding**

0 - The Chip can control two floppy disk drives directly without an external decoder.

1 - The two drive select signals and two motor enable signals from the FDC are encoded so that four floppy disk drives can be controlled. See Table 10.

Controlling four FDDs requires an external decoder. The pin states shown in Table 10 are a direct result of the bit patterns shown. All other bit patterns produce pin states that should not be decoded to enable any drive or motor.

**Bit 5 - Primary or Secondary FDC Address**

In Legacy mode, this bit selects the primary or secondary FDC address. See Table 9.

In Plug and Play mode, this bit is ignored.

**TABLE 9. Primary and Secondary Drive Address Selection**

| Bit 5 of FER | PC-AT Mode |
|---|---|
| 0 | Primary: 3F0-7h |
| 1 | Secondary: 370-7h |

**Bits 7,6 - Reserved**

These bits are reserved.

**TABLE 10. Encoded Drive and Motor Pin Information (Bit 4 of FER = 1)**

| Digital Output Register | | | | | | | | Drive Control Pins | | | | Decoded Functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | $\overline{MTR1}$ | $\overline{MTR0}$ | $\overline{DR1}$ | $\overline{DR0}$ | |
| x | x | x | 1 | x | x | 0 | 0 | Note | 0 | 0 | 0 | Activate drive 0 and motor 0 |
| x | x | 1 | x | x | x | 0 | 1 | Note | 0 | 0 | 1 | Activate drive 1 and motor 1 |
| x | 1 | x | x | x | x | 1 | 0 | Note | 0 | 1 | 0 | Activate drive 2 and motor 2 |
| 1 | x | x | x | x | x | 1 | 1 | Note | 0 | 1 | 1 | Activate drive 3 and motor 3 |
| x | x | x | 0 | x | x | 0 | 0 | Note | 1 | 0 | 0 | Activate drive 0 and deactivate motor 0 |
| x | x | 0 | x | x | x | 0 | 1 | Note | 1 | 0 | 1 | Activate drive 1 and deactivate motor 1 |
| x | 0 | x | x | x | x | 1 | 0 | Note | 1 | 1 | 0 | Activate drive 2 and deactivate motor 2 |
| 0 | x | x | x | x | x | 1 | 1 | Note | 1 | 1 | 1 | Activate drive 3 and deactivate motor 3 |

**Note:**

When bit 4 of the FER register = 1, $\overline{MTR1}$ presents a pulse that is the inverted image of the IOW strobe. This inverted pulse is active whenever an I/O write to address 3F2h or 372h takes place. This pulse is delayed by 25 - 80 nsec after the leading edge of IOW and its leading edge can be used to clock data into an external

latch (e.g., 74LS175). Address 3F2h is used if the FDC is located at the primary address (bit 5 of FER = 0) and address 372h is used if the FDC is located at the secondary address (bit 5 of FER = 1).

### 2.3.3 Function Address Register (FAR), Index 01h

In Plug and Play mode, this register is ignored.

In Legacy mode, this register selects the ISA I/O address range to which each peripheral function responds.

**FIGURE 4. FAR Register Bitmap**

**Bits 1,0 - Parallel Port Address**

These bits select the parallel port address as shown in Table 11.

**TABLE 11. Parallel Port Addresses**

| FAR | | Parallel Port Address | AT Interrupt |
|---|---|---|---|
| Bit 1 | Bit 0 | | |
| 0 | 0 | LPT2 (378-37F) | IRQ5 [a] |
| 0 | 1 | LPT1 (3BC-3BE) | IRQ7 |
| 1 | 0 | LPT3 (278-27F) | IRQ5 |
| 1 | 1 | Reserved | TRI-STATE (CTR4=0) |

a. The interrupt assigned to this address can be changed to IRQ7 by setting bit 3 of the Power and Test Register (PTR)

**Bits 3,2 - SCC1 Address**

These bits determine which ISA I/O address range is associated with SCC1 as shown in Table 13.

**TABLE 12. COM Port Selection for SCC1**

| FAR | | SCC1 |
|---|---|---|
| Bit 3 | Bit 2 | COM Port # |
| 0(default) | 0(default) | COM1 (3F8-F) |
| 0 | 1 | COM2 (2F8-F) |
| 1 | 0 | COM3 (See Table 14.) |
| 1 | 1 | COM4 (See Table 14.) |

**Bits 5,4 - SCC2 Address**

These bits determine which ISA I/O address range is associated with SCC2 as shown in Table 12.

**TABLE 13. COM Port Selection for SCC2**

| FAR | | SCC2 |
|---|---|---|
| Bit 5 | Bit 4 | COM# |
| 0 | 0 | COM1 (3F8-F) |
| 0(default) | 1(default) | COM2 (2F8-F) |
| 1 | 0 | COM3 (See Table 14.) |
| 1 | 1 | COM4 (See Table 14.) |

**Bits 7,6 - Select COM3 or COM4**

These bits select the addresses that are used for COM3 and COM4 as shown in Table 14.

**TABLE 14. Address Selection for COM3 and COM4**

| Bit 7 | Bit 6 | COM3 IRQ4 | COM4 IRQ3 |
|---|---|---|---|
| 0 | 0 | 3E8-Fh | 2E8-Fh |
| 0 | 1 | 338-Fh | 238-Fh |
| 1 | 0 | 2E8-Fh | 2E0-7h |
| 1 | 1 | 220-7h | 228-Fh |

### 2.3.4 Power and Test Register (PTR), Index 02h

This register determines the power-down method used and whether hardware power-down is enabled, and provides a bit for software power down of all enabled functions. It selects whether IRQ7 or IRQ5 is associated with LPT2. It puts the enabled SCCs into their test mode. Independent of this register the floppy disk controller can enter low power mode via the MODE command or the Data Rate Select (DSR) register.

**FIGURE 5. PTR Register Bitmap**

**Bit 0 - Power Down**

Setting this bit causes all enabled functions to be powered down.

Bits 3 and 2 of PCR can affect this function.

0 - Functions not powered down.

1 - Setting this bit causes all enabled functions to be powered down. All register data is retained when the clocks are stopped. The FDC, SCCs and parallel port are affected by this bit when the relevant PMC register bits and SCF0 register bits are set.

**Bit 1 - Reserved**

This bit is reserved.

**Bit 2 - Reserved**

This bit is reserved and must be set to 0.

**Bit 3 - Select IRQ5 or IRQ7**

In Plug and Play mode, this bit is ignored.

In Legacy mode, setting this bit associates the parallel port with IRQ7 when the address for the parallel port is 378 - 37Fh (LPT2). This bit is ignored when the parallel port address is 3BC - 3BEh (LPT1) or 278 - 27Fh (LPT3).

0 - LPT2 not associated with IRQ7

1 - LPT2 associated with IRQ7

**Bit 4 - SCC1 Test Mode**

Setting this bit puts SCC1 into a test mode, which causes its BAUDOUT clock to be present on its SOUT1 pin if the bit 7 of the Line Control Register (LCR) is set to 1.

0 - No test mode

1 - Test mode.

**Bit 5 - Reserved**

This bit is reserved.

**Bit 6 - Lock Configuration**

Setting this bit to 1 prevents all further write accesses to the Configuration Registers. Once it is set by software it can only be cleared by a hardware reset. After the initial hardware reset it is 0.

0 - Configuration Registers accessible. (Default)

1 - Configuration Registers locked.

**Bit 7 - Select Extended or Compatible Parallel Port**

When not in EPP or ECP modes, this bit controls SPP (Standard Parallel Port) mode (Compatible or Extended mode), thus controlling Pulse/Level interrupt:

In EPP mode this bit should be 0. In ECP mode, this bit is ignored.

0 - Compatible mode, pulse interrupt.

1 - Extended mode, level interrupt.

### 2.3.5 Function Control Register (FCR), Index 03h

This register determines several pin options. It selects Data Rate output or automatic media sense input signals.

For Enhanced Parallel Port it enables the $\overline{ZWS}$ options and pin.

On reset, bits 7-1 of FCR are cleared to 0.

**FIGURE 6. FCR Register Bitmap**

**Bit 0 - TDR Mode Select**

This bit selects TDR mode when bit 2 of ASC is zero.

This bit is ignored when bit 2 of ASC is 1 (see bit 2 of ASC for complete TDR mode selection). This bit is initialized to 1 during reset, thus selecting AT Compatible TDR.

0 - TDR is in Automatic Media Sense Mode. Bits 7-5 of TDR are valid.

1 - TDR is in AT Compatible Mode. Bits 7-2 of TDR are in TRI-STATE during read. (Default)

**Bit 1 - Select MSEN0 or DRATE0**

This bit is initialized to 0 during reset, thus selecting MSEN0.

0 - MSEN0 is selected on the pin. (Default)

1 - DRATE0 is selected on the pin.

**Bit 2 - Reserved**

This bit is reserved.

**Bit 3 - Parallel Port Multiplexor (PPM) Float Control**

When this bit is zero, the PPM pins are driven. Otherwise, they are in TRI-STATE. Bit 3 is also functional when the PPM is not configured. (The PPM is configured when bits 7,6 of SIRQ3 are 10, and bit 1 of SCF3 is 0.)

When this bit is set the PPM output signals are in TRI-STATE and the input signals are blocked to reduce their leakage current. The values of the blocked input signals are: BUSY=1, PE=0, SLCT=0, $\overline{\text{ACK}}$=1 and $\overline{\text{ERR}}$=1.

To avoid undefined FDC input signals, the PPM can be disabled before this bit is set.

0 - The PPM pins are driven.

1 - The PPM pins are in TRI-STATE and the pullup resistors are disconnected.

**Bit 4 - Reserved**

This bit is reserved and is always 0.

**Bit 5 - Zero Wait State Enable**

0 - No $\overline{\text{ZWS}}$ enabled.

1 - If pin 3 is configured as $\overline{\text{ZWS}}$ (see bit 6), $\overline{\text{ZWS}}$ is driven low when the Enhanced Parallel Port (EPP) or the ECP can accept a short host read/write-cycle; otherwise the $\overline{\text{ZWS}}$ open drain output signal is not driven. EPP $\overline{\text{ZWS}}$ operation should be configured when the system's device is fast enough to support it.

**Bit 6 - Select $\overline{\text{ZWS}}$ or $\overline{\text{CS1}}$ on pin 3**

0 - $\overline{\text{ZWS}}$ function is selected on pin 3.

1 - $\overline{\text{CS1}}$ function is selected on pin 3

**Bit 7 - Reserved**

Reserved bit. Write 0.

### 2.3.6 Printer Control Register (PCR), Index 04h

This register enables the EPP, ECP, version modes, and interrupt options. See Table 15.

**TABLE 15. Parallel Port Mode**

| Operation Mode | Bit 0 of FER | Bit 7 of PTR | Bit 0 of PCR | Bit 2 of PCR |
|---|---|---|---|---|
| None | 0 | X | X | X |
| Compatible | 1 | 0 | 0 | 0 |
| Extended | 1 | 1 | 0 | 0 |
| EPP | 1 | 0 | 1 | 0 |
| ECP | 1 | X | 0 | 1 |

On reset all the bits of PCR are cleared to 0.

**FIGURE 7. PCR Register Bitmap**

**Bit 0 - EPP Enable**

0 - The EPP is disabled, and the EPP registers are not accessible (access ignored).

1 - If bit 2 of PCR is 0, the EPP is enabled. The EPP should not be configured with base address 3BCh.

**Bit 1 - EPP Version Select**

0 - Version 1.7 is supported.

1 - Version 1.9 is supported (IEEE 1284).

**Bit 2 - ECP Enable**

Enables or disables ECP mode. In Plug and Play mode, IRQ7-3, IRQ12-9 or IRQ15 are selected via the PNP0 register.

0 - The ECP is disabled and in power-down mode. The ECP registers are not accessible (access ignored), the ECP interrupt is inactive and DMA request pin is in TRI-STATE. The IRQ5,7 input signals are blocked to reduce their leakage currents.

1 - The ECP is enabled. The software should change this bit to 1 only when bits 2-0 of the existing CTR are 100.

**Bit 3 - ECP Clock Freeze Control**

When either this bit or the ECP enable bit is 0, there is no change in the Chip clock stopping mechanism.

0 - The ECP does not affect the stopping of the clock multiplier (power-down mode 3) and does not change the function of bit 0 of PTR.

1 - If the ECP is enabled (bit 2 of PCR is 1), the clock multiplier is not stopped (power mode 3 is not entered) and the ECP clock is not stopped (power down mode 2 excludes the ECP).

**Bit 4 - Reserved**

This bit is reserved and must be set to 0.

**Bit 5 - Parallel Port Interrupt Polarity Control**

This bit controls the polarity of the interrupt line allocated for the parallel port.

0 - The interrupt polarity is as defined in the existing Chip, and the ECP interrupt event is level high or negative pulse.

1 - The interrupt event polarity is inverted.

**Bit 6 - Parallel Port Open-Drain Control**

Parallel port interrupt (the parallel port-allocated interrupt line) open-drain control bit.

0 - The configured interrupt line (IRQ5 or IRQ7) has a totem-pole output with TRI-STATE ability.

1 - The configured interrupt line has an open drain output signal (drive low or TRI-STATE).

**Bit 7 - Reserved**

This bit is reserved. To maintain compatibility with future Super I/O chips, do not modify this bit when this register is written, i.e., use read-modify-write to preserve the value of this bit.

### 2.3.7 Power Management Control Register (PMC), Index 06h

This register controls the TRI-STATE and input signals. The PMC Register is accessed at index 06h. The PMC Register is cleared to 0 on reset.

**FIGURE 8. PMC Register Bitmap**

**Bit 0 - Reserved**

This bit is reserved.

**Bit 1 - FDC TRI-STATE Control**

0 - No TRI-STATE enabled.

1 - If the FDC is powered down, the FDC output signals are in TRI-STATE, except the FDC-allocated interrupt line, PD, IDLE and the PPM output signals, even if the PPM is used for FDC pins, i.e., this bit does not control the IRQ6 and PPM pins.

In addition, if the FDC is powered down, the FDC input signals (except $\overline{\text{DSKCHG}}$) are blocked to reduce their leakage current.

**Bit 2 - SCC1 TRI-STATE Control**

This bit controls the TRI-STATE status of the SCC1 output pins and blocked the input pins, to avoid leakage current. This bit does not control the TRI-STATE status of the SCC1 interrupt.

0 - TRI-STATE disabled on SCC1 signals.

1 - If SCC1 is disabled or the Chip is in power-down mode, SCC1 output signals are in TRI-STATE and the input signals are blocked to reduce their leakage current.

The values of the blocked input signals are: $\overline{\text{SIN1}}$=1, $\overline{\text{CTS1}}$=1, $\overline{\text{DSR1}}$=1, $\overline{\text{DCD1}}$=1 and $\overline{\text{RI1}}$=1.

**Bit 3 - Reserved**

This bit is reserved.

**Bit 4 - PD and IDLE or IRSL2/*ID2* Enable**

This is the PD and IDLE (FDC power management output signals) or IRSL2/*ID2* enable bit. When bit 2 of the SCF3 register is 1, IRSL2 controls pin 43 (PQFP) or 41 (TQFP) instead of $\overline{\text{MTR1}}$ or IDLE. See Tables 16 and 17. *ID2 is available only in PC97338.*

0 - $\overline{\text{MTR1}}$ or IRSL2/*ID2* controls pin 43 (PQFP) or 41 (TQFP), and $\overline{\text{DR1}}$ controls pin 45 (PQFP) or 43 (TQFP).

1 - IDLE or IRSL2/*ID2* controls pin 43 (PQFP) or 41 (TQFP), and PD controls pin 45 (PQFP) or 43 (TQFP).

**TABLE 16. Bit Settings to Enable $\overline{\text{MRT1}}$, IDLE or IRSL2**

| Bit 2 of SCF3 | Bit 4 of PMC | Function Selected on Pin #43 (PQFP) or Pin #41 (TQFP) |
|---|---|---|
| 0 | 0 | $\overline{\text{MTR1}}$ |
| 0 | 1 | IDLE |
| 1 | x | IRSL2 |

**TABLE 17. Bit Settings to Enable $\overline{\text{DR1}}$ or PD**

| Bit 4 of PMC | Function Selected on Pin #45 (PQFP) or Pin #43 (TQFP) |
|---|---|
| 0 | $\overline{\text{DR1}}$ |
| 1 | PD |

**Bit 5 - Selective Lock**

This bit enables locking of the following configuration bits: bit 5 of PMC (this bit), bit 4 of FER, bits 7 through 0 of FAR, bit 3 of PTR and bit 6 of FCR. Unlike bit 6 of PTR, it does not lock all the configuration bits.

Once this bit is set by software it can only be cleared by a hardware reset. This bit should be used instead of bit 6 of PTR if a configuration bit should be dynamically modified by software (like PMC bits).

0 - No lock, except via bit 6 of PTR.

1 - Any write to the above configuration bits is ignored, until a Master Reset clears this bit.

**Bit 6 - Parallel Port (PPM) TRI-STATE Enable**

This bit enables reduction in power consumption, when the SuperI/O chip is in power-down mode, or the parallel port is disabled, by placing the PPM output signals in TRI-STATE, and blocking the PPM input signals.

0 - The parallel port pins are enabled.

1 - If the parallel port is disabled, or the Super I/O chip is in power-down mode, the output signals of the parallel port, pins (except the Parallel Port-allocated interrupt line]) are in TRI-STATE, and the input signals are blocked to reduce their leakage currents.

The values of the blocked input signals are: $\overline{\text{BUSY}}$=1, PE=0, SLCT=0, $\overline{\text{ACK}}$=1 and $\overline{\text{ERR}}$=1.

**Bit 7 - Reserved**

This bit is reserved. To maintain compatibility with future SIO chips, do not modify this bit when this register is written, i.e., use read-modify-write to preserve the value of this bit.

### 2.3.8 Tape, SCCs and Parallel Port Configuration Register (TUP), Index 07h

The TUP Register is cleared to 0XX00000 on reset.

**FIGURE 9. TUP Register Bitmap**

**Bit 0 - Reserved**

This bit is reserved.

**Bit 1 - FDC 2 Mbps Enable**

Upon reset, this bit is cleared to 0.

0 - 2 Mbps is not supported by the FDC, and the FDC clock is 24 MHz. (Default)

1 - 2 Mbps is supported by the FDC, and the FDC clock is 48 MHz The operating voltage should be 5 V. See Section 3.1.

**Bit 2 - EPP Time-Out Interrupt Enable**

0 - The EPP time-out interrupt is masked.

1 - The EPP time-out interrupt is generated on the selected IRQ line (the Parallel Port-allocated interrupt line), according to bit 6 of PCR.

**Bit 3 - MIDI/*Reserved***

In the PC87338 version this is the MIDI baud rate configuration bit which function as follow:

0 - The SCC1 baud rate generator is fed by the master clock of the Chip, divided by 13.

1 - The SCC1 baud rate generator is fed by the master clock of the Chip divided by 12. This bit should be set to support a MIDI port.

*This bit is reserved in the PC97338 version.*

**Bit 4 - Reserved**

This bit is reserved.

**Bit 5 - PD Status**

This bit holds the FDC power-down state, as defined for the PD pin, even when pin 45 (or 43 for VJG package) is not configured as PD. This bit is read only.

**Bit 6 - IDLE Status**

This bit holds the FDC idle state, as defined for the IDLE pin, even when pin 43 (or pin 41 in the VJG package) is not configured as IDLE, and when IDLE is masked by bit 7 of TUP. This bit is read only.

**Bit 7 - IDLE Pin Mask**

This bit masks the IDLE output pin (but not the IDLE status bit). This bit is ignored when pin 43 is not configured as IDLE.

0 - The IDLE output pin is unmasked The IDLE pin drives the value of the FDC idle state.

1 - The IDLE output pin is masked. The IDLE pin is driven low.

## 2.3.9 SuperI/O Chip Identification Register (SID), Index 08h

The SID register is accessed, like the other configuration registers, through the INDEX register.

This read-only register identifies the chip. Bits 2-0 contain the revision code. SID holds the value B0h.

**FIGURE 10. SID Register Bitmap**

## 2.3.10 Advanced SuperI/O Chip Configuration Register (ASC), Index 09h

During reset, bits 2-0 and bits 5,4 are initialized to 0, and bits 7,6 are initialized to 1 (1100X000).

**FIGURE 11. ASC Register Bitmap**

**Bit 0 - Select IRQ5 or ADRATE0**

In Plug and Play mode, this bit does not affect the interrupt mapping of the parallel port (even when ADRATE0 is selected).

In Legacy mode, selection of parallel port interrupt pin (IRQ5 or IRQ7) via bits 1 and 0 of FAR, and via bit 3 of PTR, is ignored and IRQ7 is used as parallel port interrupt.

0 - Pin 98 (PQFP) or pin 96 (TQFP) is IRQ5. IRQ5 is controlled by bits 6 and 5 of PCR.

1 - Pin 98 (PQFP) or pin 96 (TQFP) is ADRATE0 open drain output. ADRATE0 has the same value as DRATE0.

**Bit 1 - Reserved**

This bit is reserved.

**Bit 2 - Enhanced TDR Support**

0 - TDR read is a function of bit 0 of the FCR configuration register.

1 - The Chip provides enhanced TDR support.

**Bit 3 - PNF Status**

This bit reflects the value of the PNF pin. It is a read only bit; data written to this bit is ignored. It is undefined when the pin is configured as $\overline{DRV2}$ or $\overline{DR23}$.

This bit is undefined when the pin is configured as $\overline{DRV2}$, $\overline{DR23}$, SIRQI3 or IRSL2/*ID2*.

**Bit 4 - Select DENSEL or ADRATE1**

Controls the behavior of pin 48 in the PQFP package or of pin 46 in the TQFP package.

0 - The pin is used for DENSEL.

1 - The pin is used for ADRATE1.

**Bit 5 - ECP CNFGA Bit**

The value of this pin is reflected on bit 3 of CNFGA ECP register.

**Bit 6 - DENSEL Polarity**

This bit controls the polarity of the DENSEL signal.

Upon reset this bit is initialized to 1, thus selecting active high DENSEL for 500 Kbps, 1 Mbps and 2 Mbps data rates

0 - DENSEL is active low for data transmission rates of 500 Kbps, 1 Mbps and 2 Mbps data rates and active high for rates 250 Kbps and 300 Kbps.

1 - DENSEL is active low for data transmission rates of 250 Kbps, 300 Kbps data rates and active high for rates of 500 Kbps, 1 Mbps and 2 Mbps. (Default)

**Bit 7 - System Operation Mode**

The Chip can be configured to either AT or PS/2 mode.

Upon reset this bit is initialized to 1, thus selecting AT mode.

0 - PS/2 mode.

1 - AT mode. (Default)

### 2.3.11 Chip Select 0 Low Address Register (CS0LA), Index 0Ah

This register holds the low address bits of the monitored I/O address. See CS0HA and CS0CF for complementary description. Bit 0 holds A0

**FIGURE 12. CS0LA Register Bitmap**

### 2.3.12 Chip Select 0 Configuration Register (CS0CF), Index 0Bh

This register controls the behavior of the $\overline{CS0}$ pin. $\overline{CS0}$ is asserted on non-DMA PIO cycles, when $\overline{RD}$ or $\overline{WR}$ is asserted. $\overline{CS0}$ can be asserted only on reads, or on writes or on all cycles. The register is initialized to 0 during reset.

**FIGURE 13. CS0CF Register Bitmap**

**Bits 2-0 - Reserved**

These bits are reserved.

**Bit 3 - Number of Decoded Address Bits**

0 - During reset, if CFG0 = 0, decode 16 address bits (A15-A0) and compare them to CS0HA and CS0LA bits.

During reset, if CFG0 = 1, decode 11 address bits (A10-A0) and compare them to bits 2-0 of CS0HA and bits 7-0 of CS0LA. Bits 7-3 of CS0HA are ignored.

1 - During reset, if CFG0 = 0, decode four address bits (A15-A12) and compare them to bits 7-4 of CS0HA. Bits 3-0 of CS0HA and bits 7-0 of CS0LA are ignored.

During reset, if CFG0 = 1, it is illegal to set this bit to 1.

**Bit 4 - $\overline{\text{CS0}}$ Assert Enable (Write)**

0 - Do not enable $\overline{\text{CS0}}$ assertion on write cycles.

1 - Enable $\overline{\text{CS0}}$ assertion on write cycles.

**Bit 5 - $\overline{\text{CS0}}$ Assert Enable (Read)**

0 - Do not enable $\overline{\text{CS0}}$ assertion on read cycles.

1 - Enable $\overline{\text{CS0}}$ assertion on read cycles.

**Bits 7,6 - Reserved**

These bits are reserved.

### 2.3.13 Chip Select 1 Low Address Register (CS1LA), Index 0Ch

This register holds the low address bits of the monitored I/O address. See CS1HA and CS1CF for complementary description. Bit 0 holds A0.

**FIGURE 14. CS1LA Register Bitmap**

### 2.3.14 Chip Select 1 Configuration Register (CS1CF), Index 0Dh

This register controls the behavior of the $\overline{\text{CS1}}$ pin. $\overline{\text{CS1}}$ is asserted on non-DMA PIO cycles, when $\overline{\text{RD}}$ or $\overline{\text{WR}}$ is asserted. $\overline{\text{CS1}}$ can be asserted only on reads or writes or on all cycles. The register is initialized to 0 during reset.

**FIGURE 15. CS1CF Register Bitmap**

**Bits 2-0 - Reserved**

These bits are reserved.

**Bit 3 - Number of Decoded Address Bits**

0 - If during reset CFG0 = 0, decode 16 address bits (A15-A0) and compare them to CS1HA and CS1LA bits.

If during reset CFG0 = 1, decode 11 address bits (A10-A0) and compare them to bits 2-0 of CS1HA and bits 7-0 of CS1LA. Bits 7-3 of CS1HA are ignored.

1 - If during reset CFG[0]=0, decode 14 address bits (A15-A2) and compare them to bits 7-0 of CS1HA and bits 7-2 of CS1LA. Bits 1,0 of CS1LA are ignored.

If during reset CFG0 = 1. decode nine address bits (A10-A2) and compare them to bits 2-0 of CS1HA and bits 7-2 of CS1LA. Bits 7-3 of CS1HA and bits 1-0 of CS1LA are ignored.

**Bit 4 - $\overline{\text{CS1}}$ Assert Enable (Write)**

0 - Do not enable $\overline{\text{CS1}}$ assertion on write cycles.

1 - Enable $\overline{\text{CS1}}$ assertion on write cycles.

**Bit 5 - $\overline{\text{CS1}}$ Assert Enable (Read)**

0 - Do not enable $\overline{\text{CS1}}$ assertion on read cycles.

1 - Enable $\overline{\text{CS1}}$ assertion on read cycles.

**Bits 7,6 - Reserved**

These bits are reserved.

### 2.3.15 Chip Select 0 High Address Register (CS0HA), Index 10h

This register holds the high address bits of the monitored I/O address. See CS0LA and CS0CF for complementary description. Bit 0 holds A8. If during reset CFG0 is1, A15-11 are not input signals of the chip. Therefore, bits 7-3 are reserved.

**FIGURE 16. CS0HA Register Bitmap**

### 2.3.16 Chip Select 1 High Address Register (CS1HA), Index 11h

This register holds the high address bits of the monitored I/O address. See CS1LA and CS1CF for complementary description. Bit 0 holds A8. If during reset CFG0 is 1, A15-11 are not input pins of the chip. Therefore, bits 7-3 are reserved.

**FIGURE 17. CS1HA Register Bitmap**

### 2.3.17 SuperI/O Chip Configuration Register 0 (SCF0), Index 12h

Upon reset, SCF0 is initialized to xxxx0xxx.

**FIGURE 18. SCF0 Register Bitmap**

**Bits 2-0 - Reserved**

These bits are reserved.

**Bit 3 - SCC2 TRI-STATE Control**

This bit controls the TRI-STATE status of the SCC2 output pins and blocked the input pins, to avoid leakage current. This bit does not control the TRI-STATE status of the SCC2 interrupt.

0 - No TRI-STATE enabled in SCC2 pins.

1 - If SCC2 is disabled or the Chip is in power-down mode, SCC2 and IR output signals are in TRI-STATE and the input signals are blocked to reduce their leakage current.

The values of the blocked input signals are: IRRX1=1, IRRX2=1, SIN2=1, $\overline{CTS2}$=1, $\overline{DSR2}$=1, $\overline{DCD2}$=1, ID0=1, ID1=1, ID2=1 and $\overline{RI2}$=1.

When IRSL2-0 control their respective pins they are all 0, under these conditions.

**Bits 7-4 - Reserved**

Reserved.

## 2.3.18 SuperI/O Chip Configuration Register 1 (SCF1), Index 18h

Upon reset, SCF1 is initialized to xx00000x.

**FIGURE 19. SCF1 Register Bitmap**

**Bit 0 - Reserved**

This bit is reserved.

**Bits 2,1 - ECP DMA Number**

Reported ECP DMA number, as reflected on bits 1,0 of the CNFGB ECP register. Bit 2 of SCF1 is reflected on bit 1 of CNFGB and bit 1 of SCF1 on bit 0 of CNFGB.

Microsoft's ECP Protocol and ISA Interface Standard defines these bits as shown in Table 18.

**TABLE 18. ECP DMA Option Selection**

| Bit 2 | Bit 1 | Selected DMA Option |
|---|---|---|
| 0 | 0 | Jumpered 8-bit DMA (Default) |
| 0 | 1 | DMA Channel 1 selected |
| 1 | 0 | DMA Channel 2 selected |
| 1 | 1 | DMA Channel 3 selected |

**Bits 5-3 - Parallel Port DMA Plug and Play Support**

Upon reset these bits are initialized to 000.

When a DMA request signal, i.e., DRQ0, DRQ1, DRQ2 or DRQ3, is not configured as an FDC DMA request signal, a parallel port DMA request signal or a SCC2 DMA request signal, it is in TRI-STATE.

When a DMA acknowledge signal, i.e., $\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$, $\overline{\text{DACK2}}$ or $\overline{\text{DACK3}}$, is not configured as an FDC DMA acknowledge signal, a parallel port DMA acknowledge signal or a SCC2 DMA acknowledge signal, it is ignored.

**TABLE 19. Parallel Port Plug and Play DMA Settings**

| Bit 5 | Bit 4 | Bit 3 | Parallel Port DMA Plug and Play Setting |
|---|---|---|---|
| 0 | 0 | 0 | Disabled. Parallel port's DMA is not connected to any ISA DMA channel, i.e., it is not connected to any of the chip's DMA pins.<br>It is the software's responsibility to route all DMA sources onto the ISA DMA channels correctly. |
| 0 | 0 | 1 | Parallel port's DMA request and acknowledge signals are connected to DRQ0 and $\overline{\text{DACK0}}$ pins. |
| 0 | 1 | 0 | Parallel port's DMA request and acknowledge signals are connected to DRQ1 and $\overline{\text{DACK1}}$ pins. |
| 0 | 1 | 1 | Parallel port's DMA request and acknowledge signals are connected to DRQ2 and $\overline{\text{DACK2}}$ pins. |
| 1 | 0 | 0 | Parallel port's DMA request and acknowledge signals are connected to DRQ3 and $\overline{\text{DACK3}}$ pins. |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Bits 7-6 - Reserved**

These bits are reserved.

### 2.3.19 Plug and Play Configuration 0 Register (PNP0), Index 1Bh

This register allows configurable mapping of the parallel port's interrupt onto the ISA interrupts. Upon reset, PNP0 is initialized to 00000xxx.

**FIGURE 20. PNP0 Register Bitmap**

**Bits 2-0 - Parallel Port IRQ Select**

These bits are reflected on bits 5-3 of the CNFGB ECP register. Bit 0 of PNP0 is reflected on bit 3 of CNFGB.

Upon reset, these bits are undefined.

Microsoft's ECP Protocol and ISA Interface Standard defines these bits as shown in Table 20.

**TABLE 20. Parallel Port Plug and Play Interrupt Assignment**

| Bit 2 | Bit 1 | Bit 0 | Interrupt Assignment |
|---|---|---|---|
| 0 | 0 | 0 | Parallel port's interrupt is selected by jumpers |
| 0 | 0 | 1 | IRQ7 is parallel port's interrupt |
| 0 | 1 | 0 | IRQ9 is parallel port's interrupt |
| 0 | 1 | 1 | IRQ10 is parallel port's interrupt |
| 1 | 0 | 0 | IRQ11 is parallel port's interrupt |
| 1 | 0 | 1 | IRQ14 is parallel port's interrupt |
| 1 | 1 | 0 | IRQ15 is parallel port's interrupt |
| 1 | 1 | 1 | IRQ5 is parallel port's interrupt |

**Bit 3 - Select Legacy or Plug and Play Mode**

Upon reset this bit is initialized to 0. This bit may be modified only when all modules are disabled. In both modes, the Chip can decode 11-bit addresses or 16-bit addresses, according to the strap pin CFG0. Decoding of 10-bit addresses is not supported.

0 - Legacy mode. (Default)

The interrupts and the base addresses of the FDC, SCC1, SCC2 and the parallel port are configured as in legacy devices, i.e., as in previous SuperI/O chips. DMA channels are configurable under this mode.

1 - Plug and Play mode.

The interrupts, the DMA channels and the base addresses of the FDC, SCC1, SCC2 and the parallel port are fully Plug and Play.

**Bits 7-4 - Parallel Port Interrupt Mapping**

Parallel port interrupt mapping in Plug and Play mode. Upon reset these bits are initialized to 0000.

When enabled it can be routed onto one of the following ISA interrupts: IRQ7-3, IRQ12-9 and IRQ15, as shown in Table 21.

**TABLE 21. Parallel Port Plug and Play Interrupt Mapping**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Interrupt |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | Invalid |
| 0 | 0 | 1 | 0 | Invalid |
| 0 | 0 | 1 | 1 | IRQ3 |
| 0 | 1 | 0 | 0 | IRQ4 |
| 0 | 1 | 0 | 1 | IRQ5 |
| 0 | 1 | 1 | 0 | IRQ6 |
| 0 | 1 | 1 | 1 | IRQ7 |
| 1 | 0 | 0 | 0 | Invalid |
| 1 | 0 | 0 | 1 | IRQ9 |
| 1 | 0 | 1 | 0 | IRQ10 |
| 1 | 0 | 1 | 1 | IRQ11 |
| 1 | 1 | 0 | 0 | IRQ12 |
| 1 | 1 | 0 | 1 | Invalid |
| 1 | 1 | 1 | 0 | Invalid |
| 1 | 1 | 1 | 1 | IRQ15 |

Disable means the interrupt of the parallel port is not routed to any ISA interrupt. Unpredictable results when invalid values are written. IRQ5, IRQ12 and IRQ15 can not always be configured. For more details, see Section 6 on page 190.

It is the software's responsibility to route all interrupt sources onto the ISA interrupts correctly. These bits work with bits 2-0, to select the interrupt destination for the parallel port. However, the ac-

tual hardware selection is determined by bits 7-4 and it is software's responsibility to keep bits 2-0 and 7-4 in synchronization (if desired).

In Legacy mode, these bits are ignored and parallel port interrupt mapping is controlled by bits 1,0 of the FAR register, bit 3 of the PTR register and bit 0 of the ASC register.

### 2.3.20 Plug and Play Configuration 1 Register (PNP1), Index 1Ch

This register allows configurable mapping of the SCC's interrupt onto the ISA interrupts. Upon reset, PNP1 is initialized to 00000000.

In Legacy mode, this register is ignored and the UART interrupt mapping is controlled via bits 7-2 of the FAR register.

**FIGURE 21. PNP1 Register Bitmap**

**Bits 3-0 - SCC1 Interrupt Mapping**

SCC1 interrupt mapping in Plug and Play mode. Upon reset these bits are initialized to 0000.

These bits are defined and handled identically to bits 4,5,6 and 7 of the parallel port in the Plug and Play Configuration 0 Register (PNP0), Index 1Bh.

**Bits 7-4 - SCC2 Interrupt Mapping**

SCC2 interrupt mapping in Plug and Play mode. Upon reset these bits are initialized to 0000.

These bits are defined and handled identically to bits 4,5,6 and 7 of the parallel port in the Plug and Play Configuration 0 Register (PNP0), Index 1Bh.

### 2.3.21 SuperI/O Chip Configuration Register 2 (SCF2), Index 40h

Undefined value when out of reset. This register controls the following.

**FIGURE 22. SCF2 Register Bitmap**

**Bits 1,0 - VLD0,1**

These bits determine the state of bit 5 in the FDC Tape Drive Register (TDR), when either Automatic Media Sense TDR or Enhanced TDR is configured (bit 0 of FCR = 0 or bit 2 of ASC = 1).

Bit 5 of TDR holds $\overline{VLD0}$ bit value when two floppy disk drives mode is configured (bit 4 of FER is 0) and drive 0 is accessed. Bit 5 of TDR holds $\overline{VLD1}$ bit value when two floppy disk drives mode is configured (bit 4 of FER is 0) and drive 1 is accessed. Otherwise, bit 5 of TDR holds 1.

Upon reset, these bits are undefined.

**TABLE 22. TDR Bit 5 Values**

| Drive Accessed | SCF2 | | TDR |
|---|---|---|---|
| | Bit 1 | Bit 0 | Bit 5 |
| 0 | x | 0 | 0 |
| 0 | x | 1 | 1 |
| 1 | 0 | x | 0 |
| 1 | 1 | x | 1 |
| None | x | x | 1 |

**Bits 3-2 - Reserved**

These bits are reserved.

**Bit 4 - SCC1 Bank Select Enable**

Enables bank switching. Upon reset, this bit is initialized to 0.

0 - All attempts to access the extended registers of SCC1 are ignored. (Default)

1 - SCC1 extended registers accessible.

**Bits 5 - SCC2 Normal Power Mode**

Upon reset, this bit is initialized to 1.

0 - Low power mode. SCC2's clock is disabled. IRSL2, 1 and 0 output signals are set to 0. The $\overline{RI2}$ input signal can be set to generate an interrupt. Registers are maintained.

1 - Normal power mode - SCC2's clock is enabled. SCC2 is functional, when bit 2 of the FER register is set to 1.

**Bit 6 - SCC2 is Busy**

Read only. This bit can be used by power management software to decide when to power down SCC2.

This bit is initialized to 0.

0 - No transfer is in progress. (Default)

1 - A transfer is in progress.

UART and SIR mode: t = one character + 48*(bit time)
one character time =
(bit time) * (word size + start bit + number of stop bits + parity bit)
Bit time = 1/baudrate
TV Remote: t = 75 µs
MIR, FIR: t = 32 µs

**FIGURE 23. Busy Flag Timing**

**Bit 7 - SCC2 Bank Select Enable**

Enables bank switching. Upon reset, this bit is initialized to 0.

0 - All attempts to access the extended registers of SCC2 are ignored. (Default)

1 - SCC2 extended registers accessible.

## 2.3.22 Plug and Play Configuration 2 Register (PNP2), Index 41h

This register allows configurable mapping of the FDC's interrupt and DMA signals onto the ISA interrupts and DMA channels. It allows also configurable mapping of the parallel port's DMA signals onto the ISA DMA channels. Upon reset, PNP2 is initialized to 00110000.

**FIGURE 24. PNP2 Register Bitmap**

**Bits 3-0 - FDC Interrupt Mapping**

FDC interrupt mapping in Plug and Play mode. Upon reset these bits are initialized to 0000.

When enabled it can be routed onto one of the following ISA interrupts: IRQ3-IRQ7, IRQ9-IRQ12 and IRQ15. See Table 23.

Disable means FDC's interrupt is not routed to any ISA interrupt. Unpredictable results when invalid values are written. IRQ5, IRQ12 and IRQ15 can not always be configured. For more details, refer to Section 6 on page 190.

It is the software's responsibility to route all interrupt sources onto the ISA interrupts correctly.

In Legacy mode, these bits are ignored and the interrupt of the FDC is connected to IRQ6.

**TABLE 23. FDC Plug and Play Interrupt Mapping**

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | Invalid |
| 0 | 0 | 1 | 0 | Invalid |
| 0 | 0 | 1 | 1 | IRQ3 |
| 0 | 1 | 0 | 0 | IRQ4 |
| 0 | 1 | 0 | 1 | IRQ5 |
| 0 | 1 | 1 | 0 | IRQ6 |
| 0 | 1 | 1 | 1 | IRQ7 |

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | Invalid |
| 1 | 0 | 0 | 1 | IRQ9 |
| 1 | 0 | 1 | 0 | IRQ10 |
| 1 | 0 | 1 | 1 | IRQ11 |
| 1 | 1 | 0 | 0 | IRQ12 |
| 1 | 1 | 0 | 1 | Invalid |
| 1 | 1 | 1 | 0 | Invalid |
| 1 | 1 | 1 | 1 | IRQ15 |

**Bits 6-4 - FDC DMA Plug and Play Support**

Upon reset these bits are initialized to 011. It is the software's responsibility to route all DMA sources onto the ISA DMA channels correctly. See Table 24.

When a DMA request pin, i.e., DRQ0, DRQ1, DRQ2 or DRQ3 is not configured as an FDC DMA request signal or a Parallel Port DMA request signal, it is in TRI-STATE.

When a DMA acknowledge pin, i.e., $\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$ or $\overline{\text{DACK3}}$ is not configured as an FDC DMA acknowledge signal or a parallel port DMA acknowledge signal, it is ignored.

**TABLE 24. FDC Plug and Play DMA Settings**

| Bit 5 | Bit 4 | Bit 3 | FDC DMA Plug and Play Setting |
|---|---|---|---|
| 0 | 0 | 0 | Disabled. FDC DMA is not connected to any ISA DMA channel, i.e., it is not connected to any of the chip's DMA pins. |
| 0 | 0 | 1 | FDC DMA request and acknowledge signals are connected to DRQ0 and $\overline{\text{DACK0}}$ pins. |
| 0 | 1 | 0 | FDC DMA request and acknowledge signals are connected to DRQ1 and $\overline{\text{DACK1}}$ pins. |
| 0 | 1 | 1 | FDC DMA request and acknowledge signals are connected to DRQ2 and $\overline{\text{DACK2}}$ pins. |
| 1 | 0 | 0 | FDC DMA request and acknowledge signals are connected to DRQ3 and $\overline{\text{DACK3}}$ pins. |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Bit 7 - Reserved**

This bit is reserved.

### 2.3.23 Parallel Port Base Address Low Byte Register (PBAL), Index 42h

This register holds the low address bits of the parallel port's base address.

In Legacy mode, this register is ignored and the base address of the parallel port is determined by bits 1 and 0 of the FAR register.

In Plug and Play mode when EPP is enabled, bit 0 (A2) must be 0.

This register may be modified only when the parallel port is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so there will be no conflicts.

**FIGURE 25. PBAL Register Bitmap**

### 2.3.24 Parallel Port Base Address High Byte Register (PBAH), Index 43h

This register holds the high address bits of the parallel port's base address.

In Plug and Play mode, when ECP is enabled, bit 2 (A10) must be 0.

In Legacy mode, this register is ignored and the base address of the Parallel Port is determined by bits 1 and 0 of the FAR register.

This register may be modified only when the parallel port is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so there will be no conflicts.

**FIGURE 26. PBAH Register Bitmap**

## 2.3.25 SCC1 Base Address Low Byte Register (S1BAL), Index 44h

This register holds the low address bits of SCC1's base address.

In Legacy mode, this register is ignored and the base address of SCC1 is determined by bits 3 and 2, and bits 7 and 6 of the FAR register.

This register may be modified only when SCC1 is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so there will be no conflicts.

**FIGURE 27. S1BAL Register Bitmap**

## 2.3.26 SCC1 Base Address High Byte Register (S1BAH), Index 45h

This register holds the high address bits of SCC1's base address.

In Legacy mode, this register is ignored and the base address of SCC1 is determined by bits 3 and 2, and bits 7 and 6 of the FAR register.

This register may be modified only when SCC1 is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so as to avoid conflicts.

**FIGURE 28. S1BAH Register Bitmap**

## 2.3.27 SCC2 Base Address Low Byte Register (S2BAL), Index 46h

This register holds the low address bits of SCC2's base address.

In Legacy mode, this register is ignored and the base address of SCC2 is determined by bits 7 through 4 of the FAR register.

This register may be modified only when SCC2 is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so as to avoid conflicts.

**FIGURE 29. S2BAL Register Bitmap**

### 2.3.28 SCC2 Base Address High Byte Register (S2BAH), Index 47h

This register holds the high address bits of SCC2's base address.

In Legacy mode, this register is ignored and the base address of SCC2 is determined by bits 4-7 of FAR register.

This register may be modified only when SCC2 is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so as to avoid conflicts.

**FIGURE 30. S2BAH Register Bitmap**

### 2.3.29 FDC Base Address Low Byte Register (FBAL), Index 48h

This register holds the low address bits of the FDC's base address.

In Legacy mode, this register is ignored and the base address of the FDC is determined by bit 5 of the FER register.

This register may be modified only when the FDC is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so as to avoid conflicts.

**FIGURE 31. FBAL Register Bitmap**

### 2.3.30 FDC Base Address High Byte Register (FBAH,) Index 49h

This register holds the high address bits of the FDC's base address.

In Legacy mode, this register is ignored and the base address of the FDC is determined by bit 5 of the FER register.

This register may be modified only when the FDC is disabled. Undefined value when out of reset.

It is the software's responsibility to configure all devices so as to avoid conflicts.

**FIGURE 32. FBAH Register Bitmap**

### 2.3.31 SIO Base Address Low Byte Register (SBAL), Index 4Ah

This register holds the low address bits of the base address of the SuperI/O chip, i.e., the Chip. These bits are also the low address bits of the INDEX register.

The address of the DATA register is the next consecutive address after the address of the INDEX register.

The reset value of SBAL depends on the values of BADDR0 and BADDR1 during reset. See Table 25.

For more details about programming the Chip's base address, see Section 2.2.5 on page 38.

It is the software's responsibility to configure all devices so as to avoid conflicts.

**TABLE 25. SBAL Reset Values**

| BADDR1 | BADDR0 | SBAL Reset Value |
|---|---|---|
| 0 | 0 | 98h |
| 0 | 1 | Undefined |
| 1 | 0 | 5Ch |
| 1 | 1 | 2Eh |

**FIGURE 33. SBAL Register Bitmap**

### 2.3.32 SIO Base Address High Byte Register (SBAH), Index 4Bh

This register holds the high address bits of the base address of the SuperI/O chip, i.e., the Chip. These bits are also the high address bits of the INDEX register.

The address of the DATA register is the next consecutive address after the address of the INDEX register.

The reset value of SBAH depends on the values of BADDR0 and BADDR1 during reset. See Table 26.

For more details about programming the Chip's base address see Section 2.2.5 on page 38.

It is the software's responsibility to configure all devices so as to avoid conflicts.

**TABLE 26. SBAH Reset Values**

| BADDR1 | BADDR0 | SBAH Reset Values |
|---|---|---|
| 0 | 0 | 03h |
| 0 | 1 | Undefined |
| 1 | 0 | 01h |
| 1 | 1 | 00h |

**FIGURE 34. SBAH Register Bitmap**

### 2.3.33 System IRQ Input 1 Configuration Register (SIRQ1), Index 4Ch

This register allows configuration of the SIRQI1 signal. It is initialized to x0x00000 during reset.

**FIGURE 35. SIRQ1 Register Bitmap**

**Bits 3-0 - SIRQI1 Mapping**

When it controls its pin, SIRQI1 can be routed onto one of the following ISA interrupts: IRQ7-3, IRQ12-9. See Table 27.

Unpredictable results when invalid values are written. IRQ5 and IRQ12 can not always be configured. For more details, refer to Section 6.

It is the software's responsibility to route all interrupt sources onto the ISA interrupts correctly.

**TABLE 27. SIRQI1 Plug and Play Interrupt Mapping**

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | Invalid |
| 0 | 0 | 1 | 0 | Invalid |
| 0 | 0 | 1 | 1 | IRQ3 |
| 0 | 1 | 0 | 0 | IRQ4 |
| 0 | 1 | 0 | 1 | IRQ5 |
| 0 | 1 | 1 | 0 | IRQ6 |
| 0 | 1 | 1 | 1 | IRQ7 |
| 1 | 0 | 0 | 0 | Invalid |
| 1 | 0 | 0 | 1 | IRQ9 |
| 1 | 0 | 1 | 0 | IRQ10 |
| 1 | 0 | 1 | 1 | IRQ11 |
| 1 | 1 | 0 | 0 | IRQ12 |
| 1 | 1 | 0 | 1 | Invalid |
| 1 | 1 | 1 | 0 | Invalid |
| 1 | 1 | 1 | 1 | Invalid |

**Bit 4 - Invert SIRQI1**

This bit inverts the interrupt selected by bits 3-0.

0 - SIRQI1 not inverted. IRQx = SIRQI1.

1 - SIRQI1 inverted. IRQx = $\overline{\text{SIRQI1}}$.

**Bit 5 - SIRQI1 Status**

This bit is read-only. It holds the value of SIRQI1, when SIRQI1 controls its pin.

**Bits 7, 6 - Select IRQ15, SIRQI1 or DRQ3**

Upon reset, these bits are initialized to 00.

**TABLE 28. SIRQ1 Interrupt Settings**

| Bit 7 | Bit 6 | Selected Interrupt Connected to Pin |
|---|---|---|
| 0 | 0 | IRQ15 |
| 0 | 1 | SIRQI1 |
| 1 | 0 | DRQ3 |
| 1 | 1 | Reserved |

## 2.3.34 System IRQ Input 2 Configuration Register (SIRQ2), Index 4Dh

This register allows configuration of the SIRQI2 signal. See Table 30. It is initialized to 00x00000 during reset.

**FIGURE 36. SIRQ2 Register Bitmap**

**Bits 3-0 - SIRQI2 Mapping**

When it controls its pin, SIRQI2 can be routed onto one of the following ISA interrupts: IRQ7-3, IRQ12-9 and IRQ15. See Table 29.

Unpredictable results when invalid values are written. IRQ5, IRQ12 and IRQ15 can not always be configured. For more details, refer to Section 6.

It is the software's responsibility to route all interrupt sources onto the ISA interrupts correctly.

**TABLE 29. SIRQI2 Plug and Play Interrupt Mapping**

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | Invalid |
| 0 | 0 | 1 | 0 | Invalid |
| 0 | 0 | 1 | 1 | IRQ3 |
| 0 | 1 | 0 | 0 | IRQ4 |
| 0 | 1 | 0 | 1 | IRQ5 |
| 0 | 1 | 1 | 0 | IRQ6 |
| 0 | 1 | 1 | 1 | IRQ7 |
| 1 | 0 | 0 | 0 | Invalid |
| 1 | 0 | 0 | 1 | IRQ9 |
| 1 | 0 | 1 | 0 | IRQ10 |
| 1 | 0 | 1 | 1 | IRQ11 |
| 1 | 1 | 0 | 0 | IRQ12 |
| 1 | 1 | 0 | 1 | Invalid |
| 1 | 1 | 1 | 0 | Invalid |
| 1 | 1 | 1 | 1 | IRQ15 |

**Bit 4 - Invert SIRQI2**

In the following, x may equal 3, 4, 5, 6, 7, 9, 10, 11, 12 or 15, according to bits 3-0 of this register.

0 - SIRQI2 is not inverted. IRQx = SIRQI2.

1 - SIRQI2 is inverted. IRQx = inverted SIRQI2.

**Bit 5 - SIRQI2 Status**

This bit is read-only. It holds the value of SIRQI2, when SIRQI2 controls its pin.

**Bits 7,6 - Select MSEN1, DRATE1, $\overline{\text{CS0}}$ or SIRQI2**

These bits are ignored when bit 0 of the SCF3 register is 1. Setting bit 0 of the SCF3 register to 1 gives $\overline{\text{DACK3}}$ control of the pin it shares with MSEN1, DRATE1, $\overline{\text{CS0}}$ and SIRQI2.

Table 30 shows how the values of these bits control which signal uses the pin they share.

**TABLE 30. Selecting MSEN1, DRATE1, $\overline{\text{CS0}}$ or SIRQI2**

| Bit 0 of SCF3 | Bit 7 of SIRQ2 | Bit 6 of SIRQ2 | Signal that Uses the Pin |
|---|---|---|---|
| 0 | 0 | 0 | MSEN1 |
| 0 | 0 | 1 | DRATE1 |
| 0 | 1 | 0 | $\overline{\text{CS0}}$ |
| 0 | 1 | 1 | SIRQI2 |
| 1 | x | x | $\overline{\text{DACK3}}$ |

## 2.3.35 System IRQ Input 3 Configuration Register (SIRQ3), Index 4Eh

This register allows configuration of the SIRQI3 signal. See Table 32.

SIRQ3 is initialized to 00x00000 during reset.

**FIGURE 37. SIRQ3 Register Bitmap**

**Bits 3-0 - SIRQI3 Mapping**

When SIRQI3 controls its pin, it can be routed onto one of the following ISA interrupts: IRQ3-IRQ7, IRQ9-IRQ12 and IRQ15. See Table 31.

Unpredictable results when invalid values are written. IRQ5, IRQ12 and IRQ15 can not always be configured. For more details, refer to Section 6.

It is the software's responsibility to route all interrupt sources onto the ISA interrupts correctly.

**TABLE 31. SIRQI3 Plug and Play Interrupt Mapping**

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | Invalid |
| 0 | 0 | 1 | 0 | Invalid |
| 0 | 0 | 1 | 1 | IRQ3 |
| 0 | 1 | 0 | 0 | IRQ4 |
| 0 | 1 | 0 | 1 | IRQ5 |
| 0 | 1 | 1 | 0 | IRQ6 |
| 0 | 1 | 1 | 1 | IRQ7 |
| 1 | 0 | 0 | 0 | Invalid |
| 1 | 0 | 0 | 1 | IRQ9 |
| 1 | 0 | 1 | 0 | IRQ10 |
| 1 | 0 | 1 | 1 | IRQ11 |
| 1 | 1 | 0 | 0 | IRQ12 |
| 1 | 1 | 0 | 1 | Invalid |
| 1 | 1 | 1 | 0 | Invalid |
| 1 | 1 | 1 | 1 | IRQ15 |

**Bit 4 - Invert SIRQI3**

In the following, x = 3, 4, 5, 6, 7, 9, 10, 11, 12 or 15, according to bits 0-3 of this register.

0 - SIRQI3 not inverted. IRQx = SIRQI3.

1 - SIRQI3 inverted. IRQx = $\overline{\text{SIRQI3}}$.

**Bit 5 - SIRQI3 Status**

This bit is read-only. It holds the value of SIRQI3, when selected on the pin.

**Bits 7,6 - Select $\overline{\text{DRV2}}$, $\overline{\text{DR23}}$, PNF or SIRQI3**

When $\overline{\text{DR23}}$ controls the pin, it is asserted when either drive 2 or drive 3 is accessed (except during logical drive exchange - see bit 3 of TDR). Its value is undefined in four drive encoded mode, i.e., when bit 4 of the FER register is 1.

$\overline{\text{DRV2}}$ is masked to 1, when $\overline{\text{DR23}}$ controls the pin on the pin. When $\overline{\text{DRV2}}$, PNF or SIRQI3 control the pin, the pin is read via the $\overline{\text{DRV2}}$ bit (in the FDC registers).

When PNF does not control the pin, it is masked to 1.

These bits are ignored when bit 1 of the SCF3 register is 1. Bit 1 of the SCF3 register allows selection of IRSL2/*ID0 (ID0 in PC97338 only)* to control the pin.

Table 32 shows how the values of these bits control which signal uses the pin they share.

**TABLE 32. Selecting $\overline{\text{DRV2}}$, $\overline{\text{DR23}}$, PNF or SIRQI3**

| Bit 1 of SCF3 | Bit 7 of SIRQ3 | Bit 6 of SIRQ3 | Signal that Uses the Pin |
|---|---|---|---|
| 0 | 0 | 0 | $\overline{\text{DRV2}}$ |
| 0 | 0 | 1 | $\overline{\text{DR23}}$ |
| 0 | 1 | 0 | PNF |
| 0 | 1 | 1 | SIRQI3 |
| 1 | x | x | IRSL2 |

## 2.3.36 Plug-and-Play Configuration 3 Register (PNP3), Index 4Fh

This register allows configurable mapping of the SCC2 DMA signals onto the ISA DMA channels, as shown in Tables 33 and 34, for reception and transmission, respectively.

When a DMA request pin, i.e., DRQ0, DRQ1, DRQ2 or DRQ3, is not configured as an FDC DMA request signal, a parallel port DMA request signal or a SCC2 DMA request signal, it is in TRI-STATE.

When a DMA acknowledge pin, i.e., $\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$, $\overline{\text{DACK2}}$ or $\overline{\text{DACK3}}$, is not configured as an FDC DMA acknowledge signal, a parallel port DMA acknowledge signal or a SCC2 DMA acknowledge signal, it is ignored.

**FIGURE 38. PNP3 Register Bitmap**

**Bits 2-0 - SCC2 Receiver Channel Selection**

Upon reset these bits are initialized to 000. It is the software's responsibility to route all DMA sources onto the ISA DMA channels correctly. Table 33 shows the encoding options for these bits.

**TABLE 33. SCC2 Receiver Channel Selection**

| Bit 2 | Bit 1 | Bit 0 | SCC2 Receiver Channel Selection Settings |
|---|---|---|---|
| 0 | 0 | 0 | Disabled. SCC2 DMA is not connected to any ISA DMA channel, i.e., it is not connected to any of the chip's DMA pins. |
| 0 | 0 | 1 | SCC2 receiver DMA request and acknowledge signals are connected to DRQ0 and $\overline{\text{DACK0}}$ pins. |
| 0 | 1 | 0 | SCC2 receiver DMA request and acknowledge signals are connected to DRQ1 and $\overline{\text{DACK1}}$ pins. |
| 0 | 1 | 1 | SCC2 receiver DMA request and acknowledge signals are connected to DRQ2 and $\overline{\text{DACK2}}$ pins. |
| 1 | 0 | 0 | SCC2 receiver DMA request and acknowledge signals are connected to DRQ3 and $\overline{\text{DACK3}}$ pins. |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Bits 5-3 - SCC2 Transmission Channel Selection**

Upon reset these bits are initialized to 000. It is the software's responsibility to route all DMA sources onto the ISA DMA channels correctly. Table 34 shows the encoding options for these bits.

**TABLE 34. SCC2 Transmission Channel Selection**

| Bit 5 | Bit 4 | Bit 3 | SCC2 Transmission Channel Selection Setting |
|---|---|---|---|
| 0 | 0 | 0 | Disabled. SCC2 DMA is not connected to any ISA DMA channel, i.e., it is not connected to any of the chip's DMA pins. |
| 0 | 0 | 1 | SCC2 transmitter DMA request and acknowledge signals are connected to DRQ0 and $\overline{\text{DACK0}}$ pins. |
| 0 | 1 | 0 | SCC2 transmitter DMA request and acknowledge signals are connected to DRQ1 and $\overline{\text{DACK1}}$ pins. |
| 0 | 1 | 1 | SCC2 transmitter DMA request and acknowledge signals are connected to DRQ2 and $\overline{\text{DACK2}}$ pins. |
| 1 | 0 | 0 | SCC2 transmitter DMA request and acknowledge signals are connected to DRQ3 and $\overline{\text{DACK3}}$ pins. |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

## 2.3.37 SuperI/O Configuration 3 Register (SCF3), Index 50h

This register controls the following. Upon reset, all implemented bits are initialized to 0.

**FIGURE 39. SCF3 Register Bitmap**

**Bit 0 - Select DRATE1, MSEN1, $\overline{\text{CS0}}$, SIRQI2 or $\overline{\text{DACK3}}$**

When the pin is assigned for $\overline{\text{DACK3}}$, MSEN1 is masked to 1.

0 - DRATE1, MSEN1, $\overline{\text{CS0}}$ or SIRQI2 may use the pin, according to bits 7 and 6 of the SIRQ2 register. (Default)

1 - $\overline{\text{DACK3}}$ may use the pin.

**Bit 1 - Select $\overline{\text{DRV2}}$, PNF, $\overline{\text{DR23}}$, SIRQI3 or IRSL2/*ID2***

$\overline{\text{DRV2}}$ and PNF are masked to 1, when the pin is assigned for IRSL2.

0 - $\overline{\text{DRV2}}$, PNF, $\overline{\text{DR23}}$ or SIRQI3 may use the pin, according to bits 7 and 6 of SIRQ3 register.

1 - IRSL2/*ID2* may use the pin (*ID2 is only in PC97338)*.

**Bit 2 - Select $\overline{\text{MTR1}}$, IDLE or IRSL2/*ID2***

0 - $\overline{\text{MTR1}}$ or IDLE may use the pin, according to bit 4 of PMC register.

1 - IRSL2/*ID2* uses the pin (*ID2 is only in PC97338)*.

**Bit 3 - Select IRQ12, IRRX2, IRSL0/*ID0***

This bit is ignored in 11-bit address mode.

0 - IRQ12 may use the pin.

1 - IRRX2 or IRSL0/*ID0* may use the pin, according to SCC2 extended registers (*ID0 is only in PC97338)*.

**Bit 7-4 - Reserved**

These bits are reserved.

## 2.3.38 Clock Control Register (CLK), Index 51h

Upon power on (when $V_{DD}$ is applied), all bits of this register are initialized to 0.

This register is not reset by the MR pin.

**FIGURE 40. CLK Register Bitmap**

**Bits 1,0 - SuperI/O Chip Clock Source**

These bits define the clock source for the SuperI/O chip that is fed via the X1 pin.

Upon power on, these bits are read or write. Once they are written, they become read-only bits.

00 - The clock source is the on-chip clock multiplier fed by 14.318 MHz.

01 - The clock source is the on-chip clock multiplier fed by 24 MHz.

10 - The clock source is 48 MHz.

11 - Reserved.

**Bit 2 - Clock Multiplier Enable**

Bits 2 and 3 of the PCR register may affect this bit.

0 - On chip clock multiplier is disabled.

1 - On chip clock multiplier is enabled.

**Bit 3 - Valid Multiplier Clock Status**

Read only.

0 - On-chip clock (clock multiplier output) is frozen.

1 - On-chip clock (clock multiplier output) is stable and toggling.

**Bits 7-4 - Reserved**

These bits are reserved.

## 2.3.39 Manufacturing Test Register (MTEST), Index 52h

*This register controls manufacturing tests. It exist only in the PC97338 version.*

# 3.0 The Digital Floppy Disk Controller (FDC)

The Floppy Disk Controller (FDC) is suitable for all PC-AT, EISA, PS/2, and general purpose applications. DP8473 and N82077 software compatibility is provided. Key features include a 16-byte FIFO, PS/2 diagnostic register support, perpendicular recording mode, CMOS disk input and output logic, and a high performance Digital Data Separator (DDS).

Figure 41shows a functional block diagram of the FDC. The rest of this Section describes the FDC functions, data transfer, the FDC registers, the phases of FDC commands, the result phase status registers and the FDC commands, in that order.

## 3.1 FDC FUNCTIONS

The Chip is software compatible with the DP8473 and 82077 Floppy Disk Controllers (FDCs). Upon a power-on reset, the 16-byte FIFO is disabled. Also, the disk interface output signals are configured as active push-pull output signals, which are compatible with both CMOS input signals and open-collector resistor terminated disk drive input signals. The FIFO can be enabled with the CONFIGURE command. The FIFO can be very useful at high data rates, with systems that have a long DMA bus latency, or with multi-tasking systems such as the EISA or MCA bus structures.

The FDC supports all the DP8473 MODE command features as well as some additional features. These include control over the enabling of the FIFO for read and write operations, disabling burst mode for the FIFO, a bit that will configure the disk interface outputs as open-drain output signals, and programmability of the DENSEL output signal.

### 3.1.1 Microprocessor Interface

The FDC interface to the microprocessor consists of the A9-3, AEN, $\overline{RD}$, and $\overline{WR}$ signals, which access the chip for read and write operations; the data signals D7-0; the address lines A2-0, which select the appropriate register (see Table 35); the IRQ6 signal, and the DMA interface signals DRQ, $\overline{DACK}$, and TC. It is through this microprocessor interface that the Floppy Disk Controller (FDC) receives commands, transfers data, and returns status information.

**FIGURE 41. FDC Functional Block Diagram**

### 3.1.2 System Operation Modes

The FDC operates in PC-AT mode or PS/2 mode. The active mode is determined by bit 7 of the ASC register.

#### PC-AT Mode

The PC-AT register set is enabled. The DMA enable bit in the Digital Output Register (DOR) becomes valid (IRQ6 and DRQ can be put in TRI-STATE). TC and DENSEL become active high signals (defaults to a 5.25" floppy disk drive).

#### PS/2 Mode

This mode supports the PS/2 models 50/60/80 configuration and register set. The value of the DMA enable bit in the Digital Output Register (DOR) becomes unimportant (IRQ6 and DRQ signals are always valid). TC and DENSEL become active low signals (default to 3.5" floppy drive).

## 3.2 DATA TRANSFER

### 3.2.1 Data Rates

The FDC supports the standard PC data rates of 250, 300 and 500 Kbps, as well as1 Mbps and 2 Mbps. High performance tape and floppy disk drives that are currently emerging in the PC world, transfer data at 1 Mbps. Very high performance tape drives transfer data at 2 Mbps. The FDC also supports the perpendicular recording mode, a new format used for some high capacity disk drives at 1 Mbps.

The internal digital data separator needs no external components. It improves the window margin performance standards of the DP8473, and is compatible with the strict data separator requirements of floppy disk drives and tape drives.

The FDC contains write precompensation circuitry that defaults to 125 nsec for 250, 300, and 500 Kbps (41.67 nsec at 1 Mbps). These values can be overridden in software to disable write precompensation or to provide levels of precompensation up to 250 nsec.

The FDC has internal 24 mA data bus buffers which allow direct connection to the system bus. The internal 40 mA totem-pole disk interface buffers are compatible with both CMOS drive input signals and 150 ¾ resistor terminated disk drive input signals.

### 3.2.2 The Data Separator

The internal data separator is a fully digital PLL. The fully digital PLL synchronizes the raw data signal read from the disk drive. The synchronized signal is used to separate the encoded clock and data pulses. The data pulses are broken down into bytes, and then sent to the microprocessor by the controller.

The FDC supports five data transfer rates: 250, 300, 500 Kbps and 1, 2 Mbps in Modified Frequency Modulation (MFM) format. *In the PC97338 the FDC supports also the FM encoded data mode.*

The FDC has a dynamic window margin and lock range performance capable of handling a wide range of floppy disk drives. In addition, the data separator operates under a variety of conditions, including high fluctuations in the motor speed of tape drives that are compatible with floppy disk drives.

The dynamic window margin is the primary indicator of the quality and performance level of the data separator. It indicates the toleration of the data separator for Motor Speed Variation (MSV) of the drive spindle motor and bit jitter (or window margin).

Figure 42 shows the dynamic window margin in the performance of the FDC at different data rates, generated using a FlexStar FS-540 floppy disk simulator and a proprietary dynamic window margin test program written by National Semiconductor.

**FIGURE 42. PC87338/PC97338 Dynamic Window Margin Performance**

The x axis measures MSV. MSV is translated directly to the actual rate at which the data separator reads data from the disk. In other words, a faster than nominal motor results in a higher data rate.

The dynamic window margin performance curve also indicates how much bit jitter (or window margin) can be tolerated by the data separator. This parameter is shown on the y-axis of the graph. Bit jitter is caused by the magnetic interaction of adjacent data pulses on the disk, which effectively shifts the bits away from their nominal positions in the middle of the bit window. Window margin is commonly measured as a percentage. This percentage indicates how far a data bit can be shifted early or late with respect to its nominal bit position, and still be read correctly by the data separator. If the data separator cannot correctly decode a shifted bit, then the data is misread and a CRC error results.

The dynamic window margin performance curve supplies two pieces of information:

- The maximum range of MSV (also called “lock range”) that the data separator can handle with no read errors.
- The maximum percentage of window margin (or bit jitter) that the data separator can handle with no read errors.

Thus, the area under the dynamic window margin curves in Figure 42 is the range of MSV and bit jitter that the FDC can handle with no read errors. The internal digital data separator of the FDC performs much better than comparable digital data separator designs, and does not require any external components.

The controller maximizes the internal digital data separator by implementing a read algorithm that enhances the lock characteristics of the fully digital Phase-Locked Loop (PLL). The algorithm minimizes the effect of bad data on the synchronization between the PLL and the data.

It does this by forcing the fully digital PLL to re-lock to the clock reference frequency any time the data separator attempts to lock to a non-preamble pattern. See the state diagram of this read algorithm in Figure 43.

**FIGURE 43. Read Algorithm State Diagram**

### 3.2.3 Perpendicular Recording Mode Support

The FDC is fully compatible with perpendicular recording mode disk drives at all data transfer rates. These perpendicular drives are also called 4 Mbyte (unformatted) or 2.88 Mbyte (formatted) drives. This refers to their maximum storage capacity.

Perpendicular recording orients the magnetic flux changes (which represent bits) vertically on the disk surface, allowing for a higher recording density than conventional longitudinal recording methods. This increased recording density increases data rate by up to 1 Mbps, thereby doubling the storage capacity. In addition, the perpendicular 2.88 MB drive is read/write compatible with 1.44 MB and 720 KB diskettes (500 Kbps and 250 Kbps respectively).

The 2.88 MB drive has unique format and write data timing requirements due to its read/write head and pre-erase head design. This is illustrated in Figure 44.

**FIGURE 44. Perpendicular Recording Drive Read/Write Head and Pre-Erase Head**

Unlike conventional disk drives which have only a read/write head, the 2.88 MB drive has both a pre-erase head and read/write head. With conventional disk drives, the read/write head, itself, can rewrite the disk without problems. 2.88 MB drives need a pre-erase head to erase the magnetic flux on the disk surface before the read/write head can write to the disk surface. The pre-erase head is activated during disk write operations only, i.e. FORMAT and WRITE DATA commands.

In 2.88 MB drives, the pre-erase head leads the read/write head by 200 µm, which translates to 38 bytes at 1 Mbps (19 bytes at 500 Kbps).

For both conventional and perpendicular drives, $\overline{\text{WGATE}}$ is asserted with respect to the position of the read/write head. With conventional drives, this means that $\overline{\text{WGATE}}$ is asserted when the read/write head is located at the beginning of the preamble to the data field.

With 2.88 MB drives, since the preamble must be erased before it is rewritten, $\overline{\text{WGATE}}$ should be asserted when the pre-erase head is located at the beginning of the preamble to the data field. This means that $\overline{\text{WGATE}}$ should be asserted when the read/write head is at least 38 bytes (at 1 Mbps) before the preamble. Tables 49 and 50 on page 104 show how the perpendicular format affects gap 2 and, consequently, $\overline{\text{WGATE}}$ timing, for different data rates.

Because of the 38-byte spacing between the read/write head and the pre-erase head at 1 Mbps, the gap 2 length of 22 bytes used in the standard IBM disk format is not long enough. The format standard for 2.88 MB drives at 1 Mbps called the Perpendicular Format, increases the length of gap 2 to 41 bytes. See Figure 58 on page 99.

The PERPENDICULAR MODE command puts the Floppy Disk Controller (FDC) into perpendicular recording mode, which allows it to read and write perpendicular media. Once this command is invoked, the read, write and format commands can be executed in the normal manner. The perpendicular mode of the FDC will work at all data rates, adjusting the format and write data parameters accordingly. See “The PERPENDICULAR MODE Command” on page 104 for more details.

### 3.2.4 Data Rate Selection

The FDC sets the data rate in two ways. For PC compatible software, the Configuration Control Register (CCR) at address 3F7h programs the data rate for the FDC. The lower bits D1 and D0 in the CCR set the data rate. The other bits should be set to zero. See Table 40 on page 82 to see how to encode the desired data rate.

The lower two bits of the Data rate Select Register (DSR) at address 4 can also set the data rate. These bits are encoded like the corresponding bits in the CCR. The remainder of the bits in the DSR have other functions. See the description of the DSR in Section 3.3.7 on page 82 for more details.

The data rate is determined by the last value written to either the CCR or the DSR. Either the CCR or the DSR can override the data rate selection of the other register. When the data rate is selected, the micro-engine and data separator clocks are scaled appropriately. Also, the DRATE0 and DRATE1 output signals will reflect the state of the data selection bits that were last written to either the CCR or the DSR.

### 3.2.5 Write Precompensation

Write precompensation is a way of preconditioning the $\overline{\text{WDATA}}$ output signal to adjust for the effects of bit shift on the data as it is written to the disk surface. Data that is subject to bit shift is much harder to read by a data separator, and can cause soft read errors.

Bit shift is caused by the magnetic interaction of data bits as they are written to the disk surface. It shifts these data bits away from their nominal position in the serial MFM (*MFM or FM in the PC98338*) data pattern.

Write precompensation predicts where bit shift could occur within a data pattern. It then shifts the individual data bits early, late, or not at all so that when they are written to the disk, the shifted data bits will be back in their nominal position.

The FDC supports software programmable write precompensation. Upon power up, the default write precompensation values shown in Table 42 on page 82, will be used. In addition, the default starting track number for write precompensation is track zero

You can use the DSR to change the write precompensation using any of the values in Table 41 on page 82. Also, the starting track number for write precompensation can be changed with the CONFIGURE command.

### 3.2.6 FDC Low-Power Mode Logic

The FDC of the Chip supports two low-power modes, manual and automatic. Other low-power modes (also referred to as power down) of the Chip are described in Section 7.1.

In low-power mode, the microcode is driven from the clock, so it will be disabled while the clock is off. If bit 1 of the Power and Test configuration Register (PTR) is 1, the FDC clock is disabled upon entering this mode. Upon entering the power-down state, bit 7, the RQM (Request For Master) bit, in the Main Status Register (MSR) of the FDC will be cleared to 0.

For details concerning entering and exiting low-power mode by setting bit 6 of the Data rate Select Register (DSR) or by executing the LOW PWR option of the FDC MODE command, see "Recovery from Low-Power Mode" later in this section, the "Data Rate Select Register (DSR), Offset 100" on page 82 and Section "The MODE Command" on page 101.

The Data rate Select Register (DSR), Digital Output Register (DOR), and the Configuration Control Register (CCR) are unaffected and remain active in power-down mode. Therefore, you should make sure that the motor and drive select signals are turned off.

If the power to an external clock driving the Chip will be independently removed while the FDC is in power-down mode, it must not be done until 2 msec after the LOW PWR option of the FDC MODE command is issued.

#### Manual Low-Power Mode

Manual low power is enabled by writing a 1 to bit 6 of the DSR. The chip will power down immediately. This bit will be cleared to 0 after power up.

Manual low power can also be triggered by the MODE command. Manual low power mode functions as a logical OR function between the DSR low power bit and the LOW PWR option of the MODE command.

#### Automatic Low-Power Mode

Automatic low power mode switches the controller into low power 500 msec (at the 500 Kbps MFM data rate) after it has entered the Idle state. Once automatic low-power mode is set, it does not have to be set again, and the controller automatically goes into low power mode after entering the Idle state.

Automatic low-power mode can only be set with the LOW PWR option of the MODE command.

#### Recovery from Low-Power Mode

There are two ways the FDC section can recover from the power-down state.

Power up is triggered by a software reset via the DOR or DSR. Since a software reset requires initialization of the controller, this method might be undesirable.

Power up is also triggered by a read or write to either the Data Register (FIFO) or Main Status Register (MSR). This is the preferred way to power up since all internal register values are retained. It may take a few milliseconds for the clock to stabilize, and the microprocessor will be prevented from issuing commands during this time through the normal MSR protocol. That means that bit 7, the Request for Master (RQM) bit, in the MSR will be a 0 until the clock has stabilized. When the controller has completely stabilized after power up, the RQM bit in the MSR is set to 1 and the controller can continue where it left off.

### 3.2.7 Reset

The FDC can be reset by hardware or software. A hardware reset consists of pulsing the Master Reset (MR) input signal. A hardware reset sets all of the user addressable registers and internal registers to their default values. The SPECIFY command values are unaffected by reset, so they must be initialized again.

The major default conditions affected by reset are:

- FIFO disabled
- DMA disabled
- Implied seeks disabled
- Drive polling enabled

A software reset can be triggered by bit 2 of the Digital Output Register (DOR) or bit 7 of the Data rate Select Register (DSR). Bit 7 of DSR clears itself, while bit 2 of DOR does not clear itself.

If the LOCK bit in the LOCK command was set to 1 before the software reset, the FIFO, THRESH, and PRETRK parameters in the CONFIGURE command will be retained. In addition, the FWR, FRD, and BST parameters in the MODE command will be retained if LOCK is set to 1. This function eliminates the need for total initialization of the controller after a software reset.

After a hardware (assuming the FDC is enabled in the FER) or software reset, the Main Status Register (MSR) is immediately available for read access by the microprocessor. It will return a 00h value until all the internal registers have been updated and the data separator is stabilized.

When the controller is ready to receive a command byte, the MSR returns a value of 80h (Request for Master (RQM, bit 7) bit is set). The MSR is guaranteed to return the 80h value within 2.5 µsec after a hardware or software reset. All other user addressable registers other than the Main Status Register (MSR) and Data Register (FIFO) can be accessed at any time, even during software reset.

## 3.3 THE REGISTERS OF THE FDC

### Legacy Mode

In Legacy mode, the FDC registers are mapped to the offset address shown in Table 35, with the base address range provided by the on-chip address decoder. For PC-AT or PS/2 applications, the primary address range of the diskette controller is 3F0 to 3F7h, and the secondary address range is 370 to 377h.

**TABLE 35. The FDC Registers and Their Addresses**

| Symbol | Description | Offset | | | R/W |
|---|---|---|---|---|---|
| | | A2 | A1 | A0 | |
| SRA | Status Register A | 0 | 0 | 0 | R |
| SRB | Status Register B | 0 | 0 | 1 | R |
| DOR | Digital Output Register | 0 | 1 | 0 | R/W |
| TDR | Tape Drive Register | 0 | 1 | 1 | R/W |
| MSR | Main Status Register | 1 | 0 | 0 | R |
| DSR | Data Rate Select Register | 1 | 0 | 0 | W |
| FIFO | Data Register (FIFO) | 1 | 0 | 1 | R/W |
| - | (Bus in TRI-STATE) | 1 | 1 | 0 | X |
| DIR | Digital Input Register | 1 | 1 | 1 | R |
| CCR | CCR Configuration Control Register | 1 | 1 | 1 | W |

The FDC supports two system operation modes: PC-AT mode and PS/2 mode (micro-channel systems). Section 3.1.2 on page 70 describes each mode and “Bit 7 - System Operation Mode” on page 53 describes how each is enabled.

Unless specifically indicated otherwise, all fields in all registers are valid in both modes.

### Plug and Play Mode

In Plug and Play mode, the FDC has plug and play support, as follows:

- The FDC interrupt can be routed on one of the following ISA interrupts: IRQ3-IRQ7, IRQ9-IRQ12 and IRQ15 (see PNP2 register).
- The FDC DMA signals can be routed to one of three 8-bit ISA DMA channels (see PNP2 register); and its base address is software configurable (see FBAL and FBAH registers).
- Upon reset, the DMA of the FDC is routed to the DRQ2 and $\overline{\text{DACK2}}$ pins.

### 3.3.1 FDC Register Bitmaps

### 3.3.2 Status Register A (SRA), Offset 000

Status Register A (SRA) monitors the state of the IRQ6 signal and some of the disk interface signals. SRA is a read-only register that is valid only in PS/2 mode.

SRA can be read at any time while PS/2 mode is active. In PC-AT mode, all bits are in TRI-STATE during a microprocessor read.

**FIGURE 45. SRA Register Bitmap**

**Bit 0 - Head Direction**

This bit indicates the direction of the head of the Floppy Disk Drive (FDD). Its value is the inverse of the value of the $\overline{DIR}$ interface output signal.

0 - $\overline{DIR}$ is not active, i.e., the head of the FDD steps outward. (Default)

1 - $\overline{DIR}$ is active, i.e., the head of the FDD steps inward.

**Bit 1 - Write Protect ($\overline{WP}$)**

This bit indicates whether or not the selected Floppy Disk Drive (FDD) is write protected. Its value reflects the status of the $\overline{WP}$ disk interface input signal.

0 - $\overline{WP}$ is active, i.e., the FDD in the selected drive is write protected.

1 - $\overline{WP}$ is not active, i.e., the FDD in the selected drive is not write protected.

**Bit 2 - Beginning of Track ($\overline{INDEX}$)**

This bit indicates the beginning of a track. Its value reflects the status of the $\overline{INDEX}$ disk interface input signal.

0 - $\overline{INDEX}$ is active, i.e., it is the beginning of a track.

1 - $\overline{INDEX}$ is not active, i.e., it is not the beginning of a track.

**Bit 3 - Head Select**

This bit indicates which side of the Floppy Disk Drive (FDD) is selected by the head. Its value is the inverse of the $\overline{HDSEL}$ disk interface output signal.

0 - $\overline{HDSEL}$ is not active, i.e., the head of the FDD selects side 0. (Default)

1 - $\overline{HDSEL}$ is active, i.e., the head of the FDD selects side 1.

**Bit 4 - At Track 0 ($\overline{TRK0}$)**

This bit indicates whether or not the head of the Floppy Disk Drive (FDD) is at track 0. Its value reflects the status of the $\overline{TRK0}$ disk interface input signal.

0 - $\overline{TRK0}$ is active, i.e., the head of the FDD is at track 0.

1 - $\overline{TRK0}$ is not active, i.e., the head of the FDD is not at track 0.

**Bit 5 - Step**

This bit indicates whether or not the head of the Floppy Disk Drive (FDD) should move during a seek operation. Its value is the inverse of the $\overline{STEP}$ disk interface output signal.

0 - $\overline{STEP}$ is not active, i.e., the head of the FDD moves. (Default)

1 - $\overline{STEP}$ is active (low), i.e., the head of the FDD does not move.

**Bit 6 - Second Drive Installed ($\overline{DRV2}$)**

This bit indicates whether or not a second Floppy Disk Drive (FDD) has been installed. Its value reflects the status of the $\overline{TRK0}$ disk interface input signal.

0 - $\overline{DRV2}$ is active, i.e., a second FDD has been installed.

1 - $\overline{DRV2}$ is not active, i.e., a second FDD has not been installed.

**Bit 7 - IRQ6 Pending**

This bit signals the completion of the execution phase of certain FDC commands. Its value reflects the status of the IRQ6 pin.

0 - IRQ6 is not active.

1 - IRQ6 is active, i.e., the FDD has completed execution of certain FDC commands.

### 3.3.3 Status Register B (SRB), Offset 001

Status Register B (SRB) is a read-only diagnostic register that is valid only in PS/2 mode.

SRB can be read at any time while PS/2 mode is active. In PC-AT mode, all bits are in TRI-STATE during a microprocessor read.

**FIGURE 46. SRB Register Bitmap**

**Bit 0 - Motor 0 Status ($\overline{MTR0}$)**

This bit indicates whether motor 0 is on or off. It reflects the status of the $\overline{MTR0}$ disk interface output signal.

This bit is cleared to 0 by a hardware reset and unaffected by a software reset.

0 - $\overline{MTR0}$ is not active. Motor 0 is off.

1 - $\overline{MTR0}$ is active. Motor 0 is on. (Default)

**Bit 1 - Motor 1 Status ($\overline{MTR1}$)**

This bit indicates whether motor 1 is on or off. It reflects the status of the $\overline{MTR1}$ disk interface output signal.

This bit is cleared to 0 by a hardware reset and unaffected by a software reset.

0 - $\overline{MTR0}$ is not active. Motor 1 is off.

1 - $\overline{MTR0}$ is active. Motor 1 is on. (Default)

**Bit 2 - Write Circuitry Status ($\overline{WGATE}$)**

This bit indicates whether the write circuitry of the selected Floppy Disk Drive (FDD) is enabled or not. It reflects the status of the $\overline{WGATE}$ disk interface output signal.

0 - $\overline{\text{WGATE}}$ is not active. The write circuitry of the selected FDD is disabled.

1 - $\overline{\text{WGATE}}$ is active. The write circuitry of the selected FDD is enabled. (Default)

**Bit 3 - Read Data Status ($\overline{\text{RDATA}}$)**

If read data was sent, this bit indicates whether an odd or even number of bits was sent.

Every inactive edge transition of the $\overline{\text{RDATA}}$ disk interface output signal causes this bit to change state.

0 - Either no read data was sent or an even number of bits of read data was sent. (Default)

1 - An odd number of bits of read data was sent.

**Bit 4 - Write Data (WDATA)**

If write data was sent, this bit indicates whether an odd or even number of bits was sent.

Every inactive edge transition of the $\overline{\text{WDATA}}$ disk interface output signal causes this bit to change state.

0 - Either no write data was sent or an even number of bits of write data was sent. (Default)

1 - An odd number of bits of write data was sent.

**Bit 5 - Drive Select 0 Status**

This bit reflects the status of drive select bit 0 in the Digital Output Register (DOR). See Section 3.3.4.

It is cleared after a hardware reset and unaffected by a software reset.

0 - Either drive 0 or 2 is selected. (Default)

1 - Either drive 1 or 3 is selected.

**Bits 7,6 - Reserved**

These bits are reserved and are always 1.

### 3.3.4 Digital Output Register (DOR), Offset 010

DOR is a read/write register that can be written at any time. It controls the drive select and motor enable disk interface output signals, enables the DMA logic and contains a software reset bit.

The contents of the DOR is set to 00h after a hardware reset, and is unaffected by a software reset.

Table 36 shows how the bits of DOR select a drive and enable a motor when bit 4 of the Function Enable Register (FER) is 1. Bit patterns not shown produce states that should not be decoded to enable any drive or motor.

When bit 4 of the Function Enable Register (FER) is 1, $\overline{\text{MTR1}}$ presents a pulse that is the inverse of $\overline{\text{WR}}$. This pulse is active whenever an I/O write to address 3F2h or 372h occurs. This pulse is delayed for between 25 and 80 nsec after the leading edge of $\overline{\text{WR}}$. The leading edge of this pulse can be used to clock data into an external latch (e.g., 74LS175).

Address 3F2h is used if the FDC is located at the primary address (bit 5 of FER is 0) and address 372h is used if the FDC is located at the secondary address (bit 5 of FER is 1). See Table 9 on page 46.

**TABLE 36. Drive and Motor Pin Encoding When FER 4 = 1**

| Digital Output Register Bits | | | | | | | | Control Signals | | | | Decoded Functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MTR | | DR | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 1 | 0 | 1 | 0 | |
| x | x | x | 1 | x | x | 0 | 0 | - | 0 | 0 | 0 | Activate Drive 0 and Motor 0 |
| x | x | 1 | x | x | x | 0 | 1 | - | 0 | 0 | 1 | Activate Drive 1 and Motor 1 |
| x | 1 | x | x | x | x | 1 | 0 | - | 0 | 1 | 0 | Activate Drive 2 and Motor 2 |
| 1 | x | x | x | x | x | 1 | 1 | - | 0 | 1 | 1 | Activate Drive 3 and Motor 3 |
| x | x | x | 0 | x | x | 0 | 0 | - | 1 | 0 | 0 | Activate Drive 0 and Deactivate Motor 0 |
| x | x | 0 | x | x | x | 0 | 1 | - | 1 | 0 | 1 | Activate Drive 1 and deactivate Motor 1 |
| x | 0 | x | x | x | x | 1 | 0 | - | 1 | 1 | 0 | Activate Drive 2 and Deactivate Motor 2 |
| 0 | x | x | x | x | x | 1 | 1 | - | 1 | 1 | 1 | Activate Drive 3 and Deactivate Motor 3 |

Usually, the motor enable and drive select output signals for a particular drive are enabled together. Table 37 shows the DOR hexadecimal values that enable each of the four drives.

**TABLE 37. Drive Enable Hexadecimal Values**

| Drive | DOR Hexadecimal Value |
|---|---|
| 0 | 1C |
| 1 | 2D |
| 2 | 4E |
| 3 | 8F |

The motor enable and drive select signals for drives 2 and 3 are only available when four drives are supported, i.e., when bit 4 of FER is 1, or when drives 2 and 0 are exchanged. These signals require external logic.

**FIGURE 47. DOR Register Bitmap**

**Bits 1,0 - Drive Select**

These bits select a drive, so that only one drive select output signal is active at a time.

See four-drive encoding bit 4 of FER on page 46 and logical drive exchange bits 3,2 of TDR on page 80 for more information.

00 - Drive 0 is selected. (Default)

01 - Drive 1 is selected.

10 - If four drives are supported, or drives 2 and 0 are exchanged, drive 2 is selected.

11 - If four drives are supported, drive 3 is selected.

**Bit 2 - Reset Controller**

This bit can cause a software reset. The controller remains in a reset state until this bit is set to 1.

A software reset affects the CONFIGURE and MODE commands. See Section 3.6.2 on page 94 and 3.6.7 on page 101, respectively. A software reset does not affect the Data rate Select Register (DSR), Configuration Control Register (CCR) and other bits of this register (DOR).

This bit must be low for at least 100 nsec. There is enough time during consecutive writes to the DOR to reset software by toggling this bit.

0 - Reset controller. (Default)

1 - No reset.

**Bit 3 - DMA Enable (DMAEN)**

In PC-AT mode, this bit enables DMA operations by controlling the DRQ, $\overline{\text{DACK}}$, TC and IRQ6 DMA signals. In PC-AT mode, this bit is set to 0 after reset.

In PS/2 mode, this bit is reserved, and DRQ, $\overline{\text{DACK}}$, TC and IRQ6 are enabled. During reset, DRQ, $\overline{\text{DACK}}$, TC, and IRQ6 remain enabled.

0 - In PC-AT mode, DMA operations are disabled. $\overline{\text{DACK}}$ and TC are disabled, and DRQ and IRQ6 are put in TRI-STATE. (Default)

1 - In PC-AT mode, DMA operations are enabled, i.e., DRQ, $\overline{\text{DACK}}$, TC and IRQ6 signals are enabled.

**Bit 4- Motor Enable 0**

If four drives are supported (bit 4 of the Function Enable Register (FER) is 1), this bit may control the motor output signal for drive 0, depending on the remaining bits of this register. See Table 36.

If two drives are supported (bit 4 of the Function Enable Register (FER) is 0), this bit controls the motor output signal for drive 0.

0 - The motor signal for drive 0 is not active.

1 - The motor signal for drive 0 is active.

**Bit 5 - Motor Enable 1**

If four drives are supported (bit 4 of the Function Enable Register (FER) is 1), this bit may control the motor output signal for drive 0, depending on the remaining bits of this register. See Table 36.

If two drives are supported (bit 4 of the Function Enable Register (FER) is 0), this bit controls the motor output signal for drive 1.

0 - The motor signal for drive 1 is not active.

1 - The motor signal for drive 1 is active.

**Bit 6 - Motor Enable 2**

If drives 2 and 0 are exchanged (see logical drive exchange bits 3,2 of TDR on page 80), or if four drives are supported (bit 4 of the Function Enable Register (FER) is 1), this bit controls the motor output signal for drive 2. See Table 36.

0 - The motor signal for drive 2 is not active.

1 - The motor signal for drive 2 is active.

**Bit 7 - Motor Enable 3**

If four drives are supported (bit 4 of the Function Enable Register (FER) is 1), this bit may control the motor output signal for drive 3, depending on the remaining bits of this register. See Table 36.

0 - The motor signal for drive 3 is not active.

1 - The motor signal for drive 3 is active.

### 3.3.5 Tape Drive Register (TDR), Offset 011

The TDR register is a read/write register that acts as the Floppy Disk Controller's (FDC) media and drive type register.

The bits of the TDR register function differently, depending on the drive mode configured by bit 0 of the Function Control configuration Register (FCR) (page 48), bit 2 of the Advanced SuperI/O Chip (ASC) configuration register (page 52) and bits 1 and 0 of SuperI/O Chip configuration register 2 (SCF2) (page 58). See Table 38.

The TDR drive modes are:

- PC-AT Compatible
- Automatic Media Sense
- Enhanced

## PC-AT Compatible TDR Drive Mode

When bit 0 of FCR is 1, and bit 2 of ASC is 0, the TDR assigns a drive number to the tape drive support mode of the data separator. All other logical drives can be assigned as floppy drive support. Bits 7-2 are in TRI-STATE during read operations.

## Automatic Media Sense TDR Drive Mode

When bit 0 of FCR is 0, and bit 2 of ASC is 0, bits 7-5 of TDR are implemented, in addition to the bits that support Compatible AT TDR mode. Bits 4-2 are reserved.

## Enhanced TDR Drive Mode

When bit 0 of FCR is 0, and bit 2 of ASC is 0, the TDR uses all its bits for operation with PS/2 floppy disk drives, except for bit 4 which is reserved.

**FIGURE 48. TDR Register Bitmap**

**Bits 1,0 - Tape Drive Select 1,0**

These bits assign a logical drive number to a tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

00 - No drive selected.

01 - Drive 1 selected.

10 - Drive 2 selected.

11 - Drive 3 selected.

**TABLE 38. TDR Bit Utilization and Reset Values in Different Drive Modes**

| TDR Drive Mode | Bit 0 of FCR | Bit 2 of ASC | Bits of TDR | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Extra Density | High Density | Valid Data | Reserved | Logical Drive Control | | Drive Select | |
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PC-AT Compatible | 1 | 0 | Not used. In TRI-STATE during read operations. | | | | | | 0 | 0 |
| Automatic Media Sense | 0 | 0 | Not Reset | Not Reset | Not Reset | Reserved | | | 0 | 0 |
| Enhanced | 0 or 1 | 1 | Not Reset | Not Reset | Not Reset | 1 | 0 | 0 | 0 | 0 |

**Bits 3,2 - Logical Drive Control 1,0 (Enhanced Mode Only)**

These read/write bits control logical drive exchange between drives 0 and 2. Drive 3 is never exchanged for drive 2.

When four drives are configured, i.e., bit 4 of FER is 1, logical drives are not exchanged.

00 - No logical drive exchange.

01 - Logical drives 0 and 1 are exchanged.

10 - Logical drives 0 and 2 are exchanged.

Software exchanges the physical floppy disk control signals assigned to drives 0 and 2, i.e., $\overline{DR0}$, $\overline{DR23}$ and $\overline{MTR0}$, as follows:

The internal signal that selects drive 2 uses $\overline{DR0}$; the internal signal that selects the motor of drive 2 uses $\overline{MTR0}$; and the $\overline{DR0}$ internal signal uses $\overline{DR23}$.

11 - Reserved. Unpredictable results when 11 is configured.

**Bit 4 - Reserved**

This bit is reserved.

**Bit 5 - Valid Data (Automatic Media Sense and Enhanced Modes)**

This bit, together with bits 7,6, indicate what type of media is currently in the active floppy disk drive, as shown in Table 39.

**TABLE 39. Media Type Bit Settings**

| Bit 7 | Bit 6 | Bit 5 | Media Type |
|---|---|---|---|
| X | X | 1 | Invalid Data |
| 0 | 0 | 0 | 1.2 MB (5.25") |
| 0 | 1 | 0 | 2.88 MB |
| 1 | 0 | 0 | 1.44 MB |
| 1 | 1 | 0 | 720 KB |

The state of this bit reflects the value of either bit 1 or bit 0 of SCF2, i.e., the VLD1,0 bits. See bits 1,0 of SCF2 on page 58.

When two floppy disk drives are configured (bit 4 of FER is 0), this bit is the inverse of VLD0 (bit 0 of SCF2) when drive 0 is accessed, and the inverse of VLD1 (bit 1 of SCF2) when drive 1 is accessed. Otherwise, bit 5 of TDR is 1.

0 - Automatic media sensing is enabled and there is valid media ID sense data in bits 7 and 6 of this register.

1 - Automatic media sensing is disabled.

**Bit 6 - High Density (Automatic Media Sense and Enhanced Modes)**

When bit 5 is 0, this bit is used with bit 7 to indicate the type of media currently in the active floppy disk drive. If bit 5 is 1, it is invalid. See Table 39.

This bit reflects the value of the MSEN0 signal.

0 - If this bit is valid (bit 5 is 0), the floppy disk is 5.25 inch or 1.44 MB, depending on bit 7.

1 - If this bit is valid (bit 5 is 0), the floppy disk is 2.88 MB or 720 MB, depending on bit 7.

**Bit 7 - Extra Density (Automatic Media Sense and Enhanced Modes)**

When bit 5 is 0, this bit is used with bit 6 to indicate the type of media currently in the active floppy drive. If bit 5 is 1, it is invalid. See Table 39.

This bit reflects the value of the MSEN1 signal.

0 - If this bit is valid (bit 5 is 0), the floppy disk is 5.25 inch or 2.88 MB, depending on bit 6.

1 - If this bit is valid (bit 5 is 0), the floppy disk is 1.44 MB or 720 MB, depending on bit 6.

### 3.3.6 Main Status Register (MSR), Offset 100

This read-only register indicates the current status of the Floppy Disk Controller (FDC), indicates when the disk controller is ready to send or receive data through the Data Register (FIFO) and controls the flow of data to and from the Data Register (FIFO).

The MSR can be read at any time. It should be read before each byte is transferred to or from the Data Register (FIFO) except during a DMA transfer. No delay is required when reading this register after a data transfer.

The microprocessor can read the MSR immediately after a hardware or software reset, or recovery from a power down. The MSR contains a value of 00h, until the FDC clock has stabilized and the internal registers have been initialized.

When the FDC is ready to receive a new command, it reports a value of 80h for the MSR to the microprocessor. System software can poll the MSR until the MSR is ready. The MSR must report an 80h value (RQM set to 1) within 2.5 msec after reset or power up.

**FIGURE 49. MSR Register Bitmap**

**Bit 0 - Drive 0 Busy**

This bit indicates whether or not drive 0 is busy.

It is set to 1 after the last byte of the command phase of a SEEK or RECALIBRATE command is issued for drive 0.

This bit is cleared to 0 after the first byte in the result phase of the SENSE INTERRUPT command is read for drive 0.

0 - Not busy.

1 - Busy.

**Bit 1 - Drive 1 Busy**

This bit indicates whether or not drive 1 is busy.

It is set to 1 after the last byte of the command phase of a SEEK or RECALIBRATE command is issued for drive 1.

This bit is cleared to 0 after the first byte in the result phase of the SENSE INTERRUPT command is read for drive 1.

0 - Not busy.

1 - Busy.

**Bit 2 - Drive 2 Busy**

This bit indicates whether or not drive 2 is busy.

It is set to 1 after the last byte of the command phase of a SEEK or RECALIBRATE command is issued for drive 2.

This bit is cleared to 0 after the first byte in the result phase of the SENSE INTERRUPT command is read for drive 2.

0 - Not busy.

1 - Busy.

**Bit 3 - Drive 3 Busy**

This bit indicates whether or not drive 3 is busy.

It is set to 1 after the last byte of the command phase of a SEEK or RECALIBRATE command is issued for drive 3.

This bit is cleared to 0 after the first byte in the result phase of the SENSE INTERRUPT command is read for drive 3.

0 - Not busy.

1 - Busy.

**Bit 4 - Command in Progress**

This bit indicates whether or not a command is in progress. It is set after the first byte of the command phase is written. This bit is cleared after the last byte of the result phase is read.

If there is no result phase in a command, the bit is cleared after the last byte of the command phase is written.

0 - No command is in progress.

1 - A command is in progress.

**Bit 5 - Non-DMA Execution**

This bit indicates whether or not the controller is in the execution phase of a byte transfer operation in non-DMA mode.

This bit is used for multiple byte transfers by the microprocessor in the execution phase through interrupts or software polling.

0 - The FDC is not in the execution phase.

1 - The FDC is in the execution phase.

**Bit 6 - Data I/O (Direction)**

Indicates whether the controller is expecting a byte to be written or read, to or from the Data Register (FIFO).

0 - Data will be written to the FIFO.

1 - Data will be read from the FIFO.

**Bit 7 - Request for Master (RQM)**

This bit indicates whether or not the controller is ready to send or receive data from the microprocessor through the Data Register (FIFO). It is cleared to 0 immediately after a byte transfer and is set to 1 again as soon as the disk controller is ready for the next byte.

During a Non-DMA execution phase, this bit indicates the status of the interrupt.

0 - Not ready. (Default)

1 - Ready to transfer data.

### 3.3.7 Data Rate Select Register (DSR), Offset 100

This write-only register is used to program the data transfer rate, amount of write precompensation, power down mode, and software reset.

The data transfer rate is programmed via the CCR, not the DSR, for PC-AT, PS/2 and Micro Channel applications. Other applications can set the data transfer rate in the DSR.

The data rate of the floppy controller is determined by the most recent write to either the DSR or CCR.

The DSR is unaffected by a software reset. A hardware reset sets the DSR to 02h, which corresponds to the default precompensation setting and a data transfer rate of 250 Kbps.

**FIGURE 50. DSR Register Bitmap**

**Bits 1,0 - Data Transfer Rate Select 1,0 (DRATE 1,0)**

These bits determine the data transfer rate for the Floppy Disk Controller (FDC), depending on the supported speeds. See “Tape, SCCs and Parallel Port Configuration Register (TUP), Index 07h” on page 51. Table 40 shows the data transfer rate selected by each value of this field.

These bits are unaffected by a software reset, and are set to 10 (250 Kbps) after a hardware reset.

**TABLE 40. Data Transfer Rate Encoding**

| DSR Bits (DRATE) | | Value of Bit 1 of TUP | |
|---|---|---|---|
| **1** | **0** | **0 (24 MHz)** | **1 (48 MHz)** |
| 0 | 0 | 500 Kbps | Invalid |
| 0 | 1 | 300 Kbps | Invalid |
| 1 | 0 | 250 Kbps | Invalid |
| 1 | 1 | 1 Mbps | 2 Mbps[a] |

a. Not 100% tested.

**Bits 4-2 - Precompensation Delay Select**

This field sets the write precompensation delay that the Floppy Disk Controller (FDC) imposes on the $\overline{\text{WDATA}}$ disk interface output signal, depending on the supported speeds. See “Tape, SCCs and Parallel Port Configuration Register (TUP), Index 07h” on page 51. Table 3-6 shows the delay for each value of this field.

In most cases, the default delays shown in Table 42 are adequate. However, alternate values may be used for specific drive and media types.

Track 0 is the default starting track number for precompensation. The starting track number can be changed using the CONFIGURE command.

**TABLE 41. Write Precompensation Delays**

| DSR Bits | | | Value of Bit 1 of TUP | |
|---|---|---|---|---|
| **4** | **3** | **2** | **0 (24 MHz)** | **1 (48 MHz)** |
| 0 | 0 | 0 | Default (Table 42) | Default (Table 42) |
| 0 | 0 | 1 | 41.7 nsec | 20.8 nsec |
| 0 | 1 | 0 | 83.3 nsec | 41.7 nsec |
| 0 | 1 | 1 | 125.0 nsec | 62.5 nsec |
| 1 | 0 | 0 | 166.7 nsec | 83.3 nsec |
| 1 | 0 | 1 | 208.3 nsec | 104.2 nsec |
| 1 | 1 | 0 | 250.0 nsec | 125.0 nsec |
| 1 | 1 | 1 | 0.0 nsec | 0.0 nsec |

**TABLE 42. Default Precompensation Delays**

| Data Rate | Precompensation Delay |
|---|---|
| 2 Mbps | 20.8 nsec |
| 1 Mbps | 41.7 nsec |
| 500 Kbps | 125.0 nsec |
| 300 Kbps | 125.0 nsec |
| 250 Kbps | 125.0 nsec |

**Bit 5 - Undefined**

Should be set to 0.

**Bit 6 - Low Power**

This bit triggers a manual power down of the FDC in which the clock and data separator circuits are turned off. A manual power down can also be triggered by the MODE command.

After a manual power down, the FDC returns to normal power after a software reset, or an access to the Data Register (FIFO) or the Main Status Register (MSR).

0 - Normal power.

1 - Trigger power down.

**Bit 7 - Software Reset**

This bit controls the same kind of software reset of the FDC as bit 2 of the Digital Output Register (DOR). The difference is that this bit is automatically cleared to 0 (no reset) 100 nsec after it was set to 1.

See also “Bit 2 - Reset Controller” on page 78.

0 - No reset. (Default)

1 - Reset.

## 3.3.8 Data Register (FIFO), Offset 101

The Data Register of the FDC is a read/write register that is used to transfer all commands, data and status information between the microprocessor and the FDC.

During the command phase, the microprocessor writes command bytes into the Data Register after polling the RQM (bit 7) and DIO (bit 6) bits in the MSR. During the result phase, the microprocessor reads result bytes from the Data Register after polling the RQM and DIO bits in the MSR.

Use of the FIFO buffer lengthens the interrupt latency period and, thereby, reduces the chance of a disk overrun or underrun error occurring. Typically, the FIFO buffer is used at a 1 Mbps data transfer rate or with multi-tasking operating systems.

### Enabling and Disabling the FIFO Buffer

The 16-byte FIFO buffer can be used for DMA, interrupt, or software polling type transfers during the execution of a read, write, format or scan command.

The FIFO buffer is enabled and its threshold is set by the CONFIGURE command.

When the FIFO buffer is enabled, only execution phase byte transfers use it. If the FIFO buffer is enabled, it is not disabled after a software reset if the LOCK bit is set in the LOCK command.

The FIFO buffer is always disabled during the command and result phases of a controller operation. A hardware reset disables the FIFO buffer and sets its threshold to zero. The MODE command can also disable the FIFO for read or write operations separately.

After a hardware reset, the FIFO buffer is disabled to maintain compatibility with PC-AT systems.

### Burst Mode Enabled and Disabled

The FIFO buffer can be used with burst mode enabled or disabled by the MODE command.

In burst mode, DRQ or IRQ6 remains active until all of the bytes have been transferred to or from the FIFO buffer.

When burst mode is disabled, DRQ or IRQ6 is deactivated for 350 nsec to allow higher priority transfer requests to be processed.

### FIFO Buffer Response Time

During the execution phase of a command involving data transfer to or from the FIFO buffer, the maximum time the system has to respond to a data transfer service request is calculated by the following formula:

$$Max_Time = (THRESH + 1) \times 8 \times t_{DRP} - (16 \times t_{ICP})$$

This formula applies for all data transfer rates, whether the FIFO buffer is enabled or disabled. THRESH is a 4-bit value programmed by the CONFIGURE command, which sets the threshold of the FIFO buffer. If the FIFO buffer is disabled, THRESH is zero in the above formula. The last term in the formula, $(16 \times t_{ICP})$ is an inherent delay due to the microcode overhead required by the FDC. This delay is also data rate dependent. Section 8.4.1 on page 203 specifies minimum and maximum values for $t_{DRP}$ and $t_{ICP}$.

The programmable FIFO threshold (THRESH) is useful in adjusting the FDC to the speed of the system. A slow system with a sluggish DMA transfer capability requires a high value for THRESH. this gives the system more time to respond to a data transfer service request (DRQ for DMA mode or IRQ6 for interrupt mode). Conversely, a fast system with quick response to a data transfer service request can use a low value for THRESH.

**FIGURE 51. FDC Data Register Bitmap**

## 3.3.9 Digital Input Register (DIR), Offset 111

This read-only diagnostic register is used to detect the state of the $\overline{DSKCHG}$ disk interface input signal and some diagnostic signals. DIR is unaffected by a software reset.

The bits of the DIR register function differently depending on whether the FDC is operating in PC-AT mode or in PS/2 mode.

Section 3.1.2 on page 70 describes each mode and "Bit 7 - System Operation Mode" on page 53 describes how each is enabled.

In PC-AT mode, bits 6 through 0 are in TRI-STATE to prevent conflict with the status register of the hard disk at the same address as the DIR.

**FIGURE 52. DIR Register Bitmap**

**Bit 0 - High Density (PS/2 Mode Only)**

In PC-AT mode, this bit is reserved, in TRI-STATE and used by the status register of the hard disk.

In PS/2 mode, this bit indicates whether the data transfer rate is high or low.

0 - The data transfer rate is high, i.e., 1 Mbps, 2 Mbps or 500 Kbps.

1 - The data transfer rate is low, i.e., 300 Kbps or 250 Kbps.

**Bits 2,1 - Data Rata Select 1,0 (DRATE1,0) (PS/2 Mode Only)**

In PC-AT mode, these bits are reserved, in TRI-STATE and used by the status register of the hard disk.

In PS/2 mode, these bits indicate the status of the DRATE1,0 bits programmed in DSR or CCR, whichever is written last.

The significance of each value for these bits depends on the supported speeds. See "Tape, SCCs and Parallel Port Configuration Register (TUP), Index 07h" on page 51. See also Table 40.

00 - Data transfer rate is 500 Kbps or invalid.

01 - Data transfer rate is 300 Kbps or invalid.

10 - Data transfer rate is 250 Kbps or invalid.

11 - Data transfer rate is 1 or 2 Mbps.

**Bits 6-3 - Reserved**

These bits are reserved and are always 1. In PC-AT mode these bits are reserved and in TRI-STATE. They are used by the status register of the fixed hard disk.

**Bit 7 - Disk Changed ($\overline{\text{DSKCHG}}$)**

This bit reflects the status of the $\overline{\text{DSKCHG}}$ disk interface input signal.

During power down this bit is invalid, if it is read by the software.

0 - $\overline{\text{DSKCHG}}$ is not active.

1 - $\overline{\text{DSKCHG}}$ is active.

## 3.3.10 Configuration Control Register (CCR), Offset 111

This write-only register can be used to set the data transfer rate.

The data transfer rate is programmed via the CCR, not the DSR, for PC-AT, PS/2 and Micro Channel applications. Other applications can set the data transfer rate in the DSR. See Section 3.3.7.

This register is not affected by a software reset.

The data rate of the floppy controller is determined by the last write to either the CCR register or to the DSR register.

**FIGURE 53. CCR Register Bitmap**

**Bits 1,0 - Data Transfer Rate Select 1,0 (DRATE 1,0)**

These bits determine the data transfer rate for the Floppy Disk Controller (FDC), depending on the supported speeds. See "Tape, SCCs and Parallel Port Configuration Register (TUP), Index 07h" on page 51. Table 40 shows the data transfer rate selected by each value of this field.

These bits are unaffected by a software reset, and are set to 10 (250 Kbps) after a hardware reset.

**Bits 7-2 - Reserved**

These bits are reserved and should be set to 0.

## 3.4 THE PHASES OF FDC COMMANDS

FDC commands may be in the command phase, the execution phase or the result phase. The active phase determines how data is transferred between the Floppy Disk Controller (FDC) and the host microprocessor. When no command is in progress, the FDC may be either idle or polling a drive.

### 3.4.1 Command Phase

During the command phase, the microprocessor writes a series of bytes to the Data Register (FIFO). The first command byte contains the opcode for the command, which the controller can interpret to determine how many more command bytes to expect. The remaining command bytes contain the parameters required for the command.

The number of command bytes varies for each command. All command bytes must be written in the order specified in the Command Description Table in Section 3.6 on page 91. The execution phase starts immediately after the last byte in the command phase is written. Prior to performing the command phase, the Digital Output Register (DOR) should be set and the data rate should be set with the Data rate Select Register (DSR) or the Configuration Control Register (CCR).

The Main Status Register (MSR) controls the flow of command bytes, and must be polled by the software before writing each command phase byte to the Data Register (FIFO). Prior to writing a command byte, bit 7 of MSR (RQM, Request for Master) must be set and bit 6 of MSR (DIO, Data I/O direction) must be cleared.

After the first command byte is written to the Data Register (FIFO), bit 4 of MSR (CMD PROG, Command in Progress) is also set and remains set until the last result phase byte is read. If there is no result phase, the CMD PROG bit is cleared after the last command byte is written.

A new command may be initiated after reading all the result bytes from the previous command. If the next command requires selection of a different drive or a change in the data rate, the DOR and DSR or CCR should be updated, accordingly. If the command is the last command, the software should deselect the drive.

Normally, command processing by the controller core and updating of the DOR, DSR, and CCR registers by the microprocessor are operations that can occur independently of one another. Software must ensure that the these registers are not updated while the controller is processing a command.

### 3.4.2 Execution Phase

During the execution phase, the Floppy Disk Controller (FDC) performs the desired command.

Commands that involve data transfers (e.g., read, write and format operations) require the microprocessor to write or read data to or from the Data Register (FIFO) at this time. Some commands, such as SEEK or RECALIBRATE, control the read/write head movement on the disk drive during the execution phase via the disk interface signals. Execution of other commands does not involve any action by the microprocessor or disk drive, and consists of an internal operation by the controller.

Data can be transferred between the microprocessor and the controller during execution in DMA mode, interrupt transfer mode or software polling mode. The last two modes are non-DMA modes. All data transfer modes work with the FIFO enabled or disabled.

DMA mode is used if the system has a DMA controller. This allows the microprocessor to do other tasks while data transfer takes place during the execution phase.

If a non-DMA mode is used, an interrupt is issued for each byte transferred during the execution phase. Also, instead of using the interrupt during a non-DMA mode transfer, the Main Status Register (MSR) can be polled by software to indicate when a byte transfer is required.

#### DMA Mode - FIFO Disabled

DMA mode is selected by writing a 0 to the DMA bit in the SPECIFY command and by setting bit 3 of the DOR (DMA enabled) to 1.

In the execution phase when the FIFO is disabled, each time a byte is ready to be transferred, a DMA request (DRQ) is generated in the execution phase. The DMA controller should respond to the DRQ with a DMA acknowledge ($\overline{DACK}$) and a read or write pulse. The $\overline{DRQ}$ is cleared by the leading edge of the active low $\overline{DACK}$ input signal. After the last byte is transferred, an interrupt is generated, indicating the beginning of the result phase.

During DMA operations, FDC address signals are ignored since AEN input signal is 1. The DACK signal acts as the chip select signal for the FIFO, in this case, and the state of the address lines A2-0 is ignored. The Terminal Count (TC) signal can be asserted by the DMA controller to terminate the data transfer at any time. Due to internal gating, TC is only recognized when $\overline{DACK}$ is low.

### PC-AT Mode

In PC-AT interface mode when the FIFO is disabled, the controller is in single byte transfer mode. That is, the system has the time it takes to transfer one byte, to service a DMA request (DRQ) from the controller. DRQ is deactivated between bytes.

### PS/2 Mode

In PS/2 mode, for DMA transfers with the FIFO disabled, instead of single byte transfer mode, the FIFO is enabled with THRESH = 0Fh. Thus, DRQ is asserted when one byte enters the FIFO during a read, and when one byte can be written to the FIFO during a write. DRQ is deactivated by the leading edge of the $\overline{\text{DACK}}$ input signal, and is asserted again when $\overline{\text{DACK}}$ becomes inactive high. This operation is very similar to burst mode transfer with the FIFO enabled except that DRQ is deactivated between bytes.

## DMA Mode - FIFO Enabled

### Read Data Transfers

Whenever the number of bytes in the FIFO is greater than or equal to (16 – THRESH), a DRQ is generated. This is the trigger condition for the FIFO read data transfers from the floppy controller to the microprocessor.

When the last byte in the FIFO has been read, DRQ becomes inactive. DRQ is asserted again when the FIFO trigger condition is satisfied. After the last byte of a sector is read from the disk, DRQ is again generated even if the FIFO has not yet reached its threshold trigger condition. This guarantees that all current sector bytes are read from the FIFO before the next sector byte transfer begins.

**Burst Mode Enabled -** DRQ remains active until enough bytes have been read from the controller to empty the FIFO.

**Burst Mode Disabled -** DRQ is deactivated after each read transfer. If the FIFO is not completely empty, DRQ is asserted again after a 350 nsec delay. This allows other higher priority DMA transfers to take place between floppy disk transfers.

In addition, this mode allows the controller to work correctly in systems where the DMA controller is put into a read verify mode, where only $\overline{\text{DACK}}$ signals are sent to the FDC, with no $\overline{\text{RD}}$ pulses. This read verify mode of the DMA controller is used in some PC software. When burst mode is disabled, a pulse from the $\overline{\text{DACK}}$ input signal may be issued by the DMA controller, to correctly clocks data from the FIFO.

### Write Data Transfers

Whenever the number of bytes in the FIFO is less than or equal to THRESH, a DRQ is generated. This is the trigger condition for the FIFO write data transfers from the microprocessor to the FDC.

**Burst Mode Enabled -** DRQ remains active until enough bytes have been written to the controller to completely fill the FIFO.

**Burst Mode Disabled -** DRQ is deactivated after each write transfer. If the FIFO is not full, DRQ is asserted again after a 350 nsec delay. Deactivation of DRQ allows other higher priority DMA transfers to take place between floppy disk transfers.

The FIFO has a byte counter which monitors the number of bytes being transferred to the FIFO during write operations whether burst mode is enabled or disabled. When the last byte of a sector is transferred to the FIFO, DRQ is deactivated even if the FIFO has not been completely filled. Thus, the FIFO is cleared after each sector is written. Only after the FDC has determined that another sector is to be written, is DRQ asserted again. Also, since DRQ is deactivated immediately after the last byte of a sector is written to the FIFO, the system will not be delayed by deactivation of DRQ and is free to do other operations.

### Read and Write Data Transfers

The $\overline{\text{DACK}}$ input signal from the DMA controller may be held active during an entire burst, or a pulse may be issued for each byte transferred during a read or write operation. In burst mode, the FDC deactivates DRQ as soon as it recognizes that the last byte of a burst was transferred.

If a $\overline{\text{DACK}}$ pulse is issued for each byte, the leading edge of this pulse is used to deactivate DRQ. If a $\overline{\text{DACK}}$ pulse is issued, $\overline{\text{RD}}$ or $\overline{\text{WR}}$ is not required. This is the case during the read-verify mode of the DMA controller.

If $\overline{\text{DACK}}$ is held active during the entire burst, the trailing edge of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ pulse is used to deactivate DRQ. DRQ is deactivated within 50 nsec of the leading edge of $\overline{\text{DACK}}$, $\overline{\text{RD}}$, or $\overline{\text{WR}}$. This quick response should prevent the DMA controller from transferring extra bytes in most applications.

### Overrun Errors

An overrun or underrun error terminates the execution of a command, if the system does not transfer data within the allotted data transfer time. (See Section 3.3.8 on page 83), This puts the controller in the result phase.

During a read overrun, the microprocessor is required to read the remaining bytes of the sector before the controller asserts IRQ6, signifying the end of execution.

During a write operation, an underrun error terminates the execution phase after the controller has written the remaining bytes of the sector with the last correctly written byte to the FIFO. Whether there is an error or not, an interrupt is generated at the end of the execution phase, and is cleared by reading the first result phase byte.

$\overline{DACK}$ asserted alone, without a $\overline{RD}$ or $\overline{WR}$ pulse, is also counted as a transfer. If pulses of $\overline{RD}$ or $\overline{WR}$ are not being issued for each byte, a $\overline{DACK}$ pulse must be issued for each byte so that the Floppy Disk Controller(FDC) can count the number of bytes correctly.

The VERIFY command, allows easy verification of data written to the disk without actually transferring the data on the data bus.

## Interrupt Transfer Mode - FIFO Disabled

If interrupt transfer (non-DMA) mode is selected, IRQ6 is asserted instead of DRQ, when each byte is ready to be transferred.

The Main Status Register (MSR) should be read to verify that the interrupt is for a data transfer. The RQM and NON DMA bits (bits 7 and 5, respectively) in the MSR are set to 1. The interrupt is cleared when the byte is transferred to or from the Data Register (FIFO). To transfer the data in or out of the Data register, you must use the address bits of the FDC together and $\overline{RD}$ or $\overline{WR}$ must be active, i.e., A2-0 must be valid. It is not enough to just assert the address bits of the FDC. $\overline{RD}$ or $\overline{WR}$ must also be active for a read or write transfer to be recognized.

The microprocessor should transfer the byte within the data transfer service time (see Section 3.3.8 on page 83). If the byte is not transferred within the time allotted, an overrun error is indicated in the result phase when the command terminates at the end of the current sector.

An interrupt is also generated after the last byte is transferred. This indicates the beginning of the result phase. The RQM and DIO bits (bits 7 and 6, respectively) in the MSR are set to 1, and the NON DMA bit (bit 5) is cleared to 0. This interrupt is cleared by reading the first result byte.

## Interrupt Transfer Mode - FIFO Enabled

Interrupt transfer (non-DMA) mode with the FIFO enabled is very similar to interrupt transfer mode with the FIFO disabled. In this case, IRQ6 is asserted instead of DRQ, under the same FIFO threshold trigger conditions. The MSR should be read to verify that the interrupt is for a data transfer. The RQM and non-DMA bits (bits 7 and 5, respectively) in the MSR are set. To transfer the data in or out of the Data register, you must use the address bits of the FDC together and $\overline{RD}$ or $\overline{WR}$ must be active, i.e., A2-0 must be valid. It is not enough to just assert the address bits of the FDC. $\overline{RD}$ or $\overline{WR}$ must also be active for a read or write transfer to be recognized.

Burst mode may be used to hold the IRQ6 pin active during a burst, or burst mode may be disabled to toggle the IRQ6 pin for each byte of a burst. The Main Status Register (MSR) is always valid to the microprocessor. For example, during a read command, after the last byte of data has been read from the disk and placed in the FIFO, the MSR still indicates that the execution phase is active, and that data needs to be read from the Data Register (FIFO). Only after the last byte of data has been read by the microprocessor from the FIFO does the result phase begin.

The overrun and underrun error procedures for non-DMA mode are the same as for DMA mode. Also, whether there is an error or not, an interrupt is generated at the end of the execution phase, and is cleared by reading the first result phase byte.

## Software Polling

If non-DMA mode is selected and interrupts are not suitable, the microprocessor can poll the MSR during the execution phase to determine when a byte is ready to be transferred. The RQM bit (bit 7) in the MSR reflects the state of the IRQ6 signal. Otherwise, the data transfer is similar to the interrupt mode described above, whether the FIFO is enabled or disabled.

## 3.4.3 Result Phase

During the result phase, the microprocessor reads a series of result bytes from the Data Register (FIFO). These bytes indicate the status of the command. They may indicate whether the command executed properly, or may contain some control information.

See the specific commands in “The FDC Command Set” on page 91 or “Data Register (FIFO), Offset 101” on page 83 for details.

These result bytes are read in the order specified for that particular command. Some commands do not have a result phase. Also, the number of result bytes varies with each command. All result bytes must be read from the Data Register (FIFO) before the next command can be issued.

As it does for command bytes, the Main Status Register (MSR) controls the flow of result bytes, and must be polled by the software before reading each result byte from the Data Register (FIFO). The RQM bit (bit 7) and DIO bit (bit 6) of the MSR must both be set before each result byte can be read.

After the last result byte is read, the Command in Progress bit (bit 4) of the MSR is cleared, and the controller is ready for the next command.

For more information, see “The Result Phase Status Registers” on page 88.

### 3.4.4 Idle Phase

After a hardware or software reset, after the chip has recovered from power-down mode or when there are no commands in progress the controller is in the idle phase. The controller waits for a command byte to be written to the Data Register (FIFO). The RQM bit is set, and the DIO bit is cleared in the MSR.

After receiving the first command (opcode) byte, the controller enters the command phase. When the command is completed the controller again enters the idle phase. The Digital Data Separator (DDS) remains synchronized to the reference frequency while the controller is idle. While in the idle phase, the controller periodically enters the drive polling phase.

### 3.4.5 Drive Polling Phase

National Semiconductor’s FDC supports the polling mode of old 8-inch drives, as a means of monitoring any change in status for each disk drive present in the system. This support provides backward compatibility with software that expects it.

In the idle phase, the controller enters a drive polling phase every 1 msec, based on a 500 Kbps data transfer rate. In the drive polling phase, the controller checks the status of each of the logical drives (bits 0 through 3 of the MSR). The internal ready line for each drive is toggled only after a hardware or software reset, and an interrupt is generated for drive 0.

At this point, the software must issue four SENSE INTERRUPT commands to clear the status bit for each drive, unless drive polling is disabled via the POLL bit in the CONFIGURE command. See “Bit 4 - Disable Drive Polling (POLL)” on page 94. The CONFIGURE command must be issued within 500 µsec (worst case) of the hardware or software reset to disable drive polling.

Even if drive polling is disabled, drive stepping and delayed power-down occur in the drive polling phase. The controller checks the status of each drive and, if necessary, it issues a pulse on the $\overline{\text{STEP}}$ output signal with the $\overline{\text{DIR}}$ signal at the appropriate logic level.

The controller also uses the drive polling phase to automatically trigger power down. When the specified time that the motor may be off has expired, the controller waits 512 msec, based on data transfer rates of 500 Kbps and 1 Mbps, before powering down, if this function is enabled via the MODE command.

If a new command is issued while the FDC is in the drive polling phase, the MSR does not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This can cause a delay between the first and second bytes of up to 500 µsec at 250 Kbps.

## 3.5 THE RESULT PHASE STATUS REGISTERS

In the result phase of a command, result bytes that hold status information are read from the Data Register (FIFO). These bytes are the result phase status registers.

The result phase status registers may only be read from the Data Register (FIFO) during the result phase of certain commands, unlike the Main Status Register (MSR), which is a read only register that is always valid.

### 3.5.1 Result Phase Status Register 0 (ST0)

**FIGURE 54. ST0 Result Phase Register Bitmap**

**Bits 1,0 - Logical Drive Selected**

These two binary encoded bits indicate the logical drive selected at the end of the execution phase.

The value of these bits is reflected in bits 1,0 of the SR3 register, described on page 91.

00 - Drive 0 selected.

01 - Drive 1 selected.

10 - If four drives are supported, or drives 2 and 0 are exchanged, drive 2 is selected.

11 - If four drives are supported, drive 3 is selected.

**Bit 2 - Head Selected**

This bit indicates which side of the Floppy Disk Drive (FDD) is selected. It reflects the status of the $\overline{\text{HDSEL}}$ signal at the end of the execution phase.

The value of this bit is reflected in bit 2 of the SR3 register, described on page 91.

0 - Side 0 is selected.

1 - Side 1 is selected.

**Bit 3 - Not used.**

This bit is not used and is always 0.

**Bit 4 - Equipment Check**

After a RECALIBRATE command, this bit indicates whether the head of the selected drive was at track 0, i.e., whether or not $\overline{TRK0}$ was active. This information is used during the SENSE INTERRUPT command.

0 - Head was at track 0, i.e., a $\overline{TRK0}$ pulse occurred after a RECALIBRATE command.

1 - Head was not at track 0, i.e., no $\overline{TRK0}$ pulse occurred after a RECALIBRATE command.

**Bit 5 - SEEK End**

This bit indicates whether or not a SEEK, RELATIVE SEEK, or RECALIBRATE command was completed by the controller. Used during a SENSE INTERRUPT command.

0 - SEEK, RELATIVE SEEK, or RECALIBRATE command not completed by the controller.

1 - SEEK, RELATIVE SEEK, or RECALIBRATE command was completed by the controller.

**Bits 7,6 - Interrupt Code (IC)**

These bits indicate the reason for an interrupt.

00 - Normal termination of command.

01 - Abnormal termination of command. Execution of command was started, but was not successfully completed.

10 - Invalid command issued. Command issued was not recognized as a valid command.

11 - Internal drive ready status changed state during the drive polling mode. This only occurs after a hardware or software reset.

### 3.5.2 Result Phase Status Register 1 (ST1)

**FIGURE 55. ST1 Result Phase Register Bitmap**

**Bit 0 - Missing Address Mark**

This bit indicates whether or not the Floppy Disk Controller (FDC) failed to find an address mark in a data field during a read, scan, or verify command.

0 - No missing address mark.

1 - Address mark missing.

Bit 0 of the result phase Status register 2 (ST2) indicates the when and where the failure occurred. See Section 3.5.3 on page 90.

**Bit 1 - Drive Write Protected**

When a write or format command is issued, this bit indicates whether or not the selected drive is write protected, i.e., the $\overline{WP}$ signal is active.

0 - Selected drive is not write protected, i.e., $\overline{WP}$ is not active.

1 - Selected drive is write protected, i.e., $\overline{WP}$ is active.

**Bit 2 - Missing Data**

This bit indicates whether or not data is missing for one of the following reasons:

— Controller cannot find the sector specified in the command phase during the execution of a read, write, scan, or VERIFY command. An Address Mark (AM) was found however, so it is not a blank disk.

— Controller cannot read any address fields without a CRC error during a READ ID command.

— Controller cannot find starting sector during execution of READ A TRACK command.

0 - Data is not missing for one of these reasons.

1 - Data is missing for one of these reasons.

**Bit 3 - Not Used**

This bit is not used and is always 0.

**Bit 4 - Overrun or Underrun**

This bit indicates whether or not the FDC was serviced by the microprocessor soon enough during a data transfer in the execution phase. For read operations, this bit indicates a data overrun. For write operations, it indicates a data underrun.

0 - FDC was serviced in time.

1 - FDC was not serviced fast enough. Overrun or underrun occurred.

**Bit 5 - CRC Error**

This bit indicates whether or not the FDC detected a Cyclic Redundancy Check (CRC) error.

0 - No CRC error detected.

1 - CRC error detected.

Bit 5 of the result phase Status register 2 (ST2) indicates when and where the error occurred. See Section 3.5.3.

**Bit 6 - Not Used**

This bit is not used and is always 0.

**Bit 7 - End of Track**

This bit is set to 1 when the FDC transfers the last byte of the last sector without the TC signal becoming active. The last sector is the End of Track sector number programmed in the command phase.

0 - The FDC did not transfer the last byte of the last sector without the TC signal becoming active.

1 - The FDC transferred the last byte of the last sector without the TC signal becoming active.

### 3.5.3 Result Phase Status Register 2 (ST2)

**FIGURE 56. ST2 Result Phase Register Bitmap**

**Bit 0 - Missing Address Mark Location**

If the FDC cannot find the address mark of a data field or of an address field during a read, scan, or verify command, i.e., bit 0 of ST1 is 1, this bit indicates when and where the failure occurred.

0 - The FDC failed to detect an address mark for the address field after two disk revolutions.

1 - The FDC failed to detect an address mark for the data field after it found the correct address field.

**Bit 1 - Bad Track**

This bit indicates whether or not the FDC detected a bad track

0 - No bad track detected.

1 - Bad track detected.

The desired sector is not found. If the track number recorded on any sector on the track is FFh and this number is different from the track address specified in the command phase, then there is a hard error in IBM format.

**Bit 2 - Scan Not Satisfied**

This bit indicates whether or not the value of the data byte from the microprocessor meets any of the conditions specified by the scan command used.

"The SCAN EQUAL, the SCAN LOW OR EQUAL and the SCAN HIGH OR EQUAL Commands" on page 112 and Table 55 describes the conditions.

0 - The data byte from the microprocessor meets at least one of the conditions specified.

1 - The data byte from the microprocessor does not meet any of the conditions specified.

**Bit 3 - Scan Satisfied**

This bit indicates whether or not the value of the data byte from the microprocessor was equal to a byte on the floppy disk during any scan command.

0 - No equal byte was found.

1 - A byte whose value whose values is equal to the byte from the microprocessor was found on the floppy disk.

**Bit 4 - Wrong Track**

This bit indicates whether or not there was a problem finding the sector because of the track number.

0 - Sector found.

1 - Desired sector not found.

The desired sector is not found. The track number recorded on any sector on the track is different from the track address specified in the command phase.

**Bit 5 - CRC Error in Data Field**

When the FDC detected a CRC error in the correct sector (bit 5 of the result phase Status register 1 (ST1) is 1), this bit indicates whether it occurred in the address field or in the data field.

0 - The CRC error occurred in the address field.

1 - The CRC error occurred in the data field.

**Bit 6 - Control Mark**

When the controller tried to read a sector, this bit indicates whether or not it detected a deleted data address mark during execution of a READ DATA or scan commands, or a regular address mark during execution of a READ DELETED DATA command.

0 - No control mark detected.

1 - Control mark detected.

**Bit 7 - Not Used**

This bit is not used and is always 0.

### 3.5.4 Result Phase Status Register 3 (ST3)

**FIGURE 57. ST3 Result Phase Register**

**Bits 1,0 - Logical Drive Selected**

These two binary encoded bits indicate the logical drive selected at the end of the command phase.

The value of these bits is the same as bits 1,0 of the SR0 register, described on page 88.

00 - Drive 0 selected.

01 - Drive 1 selected.

10 - If four drives are supported, or drives 2 and 0 are exchanged, drive 2 is selected.

11 - If four drives are supported, drive 3 is selected.

**Bit 2 - Head Selected**

This bit indicates which side of the Floppy Disk Drive (FDD) is selected. It reflects the status of the $\overline{\text{HDSEL}}$ signal at the end of the command phase.

The value of this bit is the same as bit 2 of the SR0 register, described on page 88.

0 - Side 0 is selected.

1 - Side 1 is selected.

**Bit 3 - Not Used**

This bit is not used and is always 1.

**Bit 4 - Track 0**

This bit Indicates whether or not the head of the selected drive is at track 0.

0 - The head of the selected drive is not at track 0, i.e., $\overline{\text{TRK0}}$ is not active.

1 - The head of the selected drive is at track 0, i.e., $\overline{\text{TRK0}}$ is active.

**Bit 5 - Not Used**

This bit is not used and is always 1.

**Bit 6 - Drive Write Protected**

This bit indicates whether or not the selected drive is write protected, i.e., the $\overline{\text{WP}}$ signal is active (low).

0 - Selected drive is not write protected, i.e., $\overline{\text{WP}}$ is not active.

1 - Selected drive is write protected, i.e., $\overline{\text{WP}}$ is active.

**Bit 7 - Not Used**

This bit is not used and is always 0.

## 3.6 THE FDC COMMAND SET

The first command byte for each command in the FDC command set is the opcode byte. The FDC uses this byte to determine how many command bytes to expect.

If an invalid command byte is issued to the controller, it immediately enters the result phase and the status is 80 (hex), signifying an invalid command.

Table 43 shows the FDC commands in alphabetical order with the opcode, i.e., the first command byte, for each.

In this table:

- MT is a multi-track enable bit (See “Bit 7 - Multi-Track (MT)” on page 106.)
- MFM is a modified frequency modulation parameter (See “Bit 6 - Modified Frequency Modulation (MFM)” on page 96.)
- SK is a skip control bit. (See “Bit 5 - Skip Control (SK)” on page 105.)

Section 3.6.1 explains some symbols and abbreviations you will encounter in the descriptions of the commands.

All phases of each command are described in detail, starting with Section 3.6.2, with bitmaps of each byte in each phase.

Only named bits and fields are described in detail. When a bitmap shows a value (0 or 1) for a bit, that bit must have that value and is not described.

**TABLE 43. FDC Command Set Summary**

| Command | Opcode | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CONFIGURE | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| DUMPREG | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| FORMAT TRACK | 0 | MFM | 0 | 0 | 1 | 1 | 0 | 1 |
| INVALID | Invalid Opcode | | | | | | | |
| LOCK | | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| MODE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| NSC | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| PERPENDICULAR MODE | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| READ DATA | MT | MFM | SK | 0 | 0 | 1 | 1 | 0 |
| READ DELETED DATA | MT | MFM | SK | 0 | 1 | 1 | 0 | 0 |
| READ ID | 0 | MFM | 0 | 0 | 1 | 0 | 1 | 0 |
| READ TRACK | 0 | MFM | 0 | 0 | 0 | 0 | 1 | 0 |
| RECALIBRATE | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| RELATIVE SEEK | 1 | MFM | 0 | 0 | 1 | 1 | 1 | 1 |
| SCAN EQUAL | MT | MFM | SK | 1 | 0 | 0 | 0 | 1 |
| SCAN HIGH OR EQUAL | MT | MFM | SK | 1 | 1 | 1 | 0 | 1 |
| SCAN LOW OR EQUAL | MT | MFM | SK | 1 | 1 | 0 | 0 | 1 |
| SEEK | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| SENSE DRIVE STATUS | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| SENSE INTERRUPT | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| SET TRACK | 0 | | 1 | 0 | 0 | 0 | 0 | 1 |
| SPECIFY | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| VERIFY | MT | MFM | SK | 1 | 0 | 1 | 1 | 0 |
| VERSION | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| WRITE DATA | MT | MFM | 0 | 0 | 0 | 1 | 0 | 1 |
| WRITE DELETED DATA | MT | MFM | 0 | 0 | 1 | 0 | 0 | 1 |

### 3.6.1 Abbreviations Used in FDC Commands

**BFR** Buffer enable bit set in the MODE command. Enabled open-collector output buffers.

**BST** Burst mode disable control bit set in MODE command. Disables burst mode for the FIFO, if the FIFO is enabled.

**DC3-0** Drive Configuration for drives 3-0. Used to configure a logical drive to conventional or perpendicular mode. Used in the PERPENDICULAR MODE command.

**DENSEL**
Density Select control bits set in the MODE command.

**DIR** Direction control bit used in RELATIVE SEEK command to indicate step in or out.

**DMA** DMA mode enable bit set in the SPECIFY command.

**DS1-0** Drive Select for bits 1,0 used in most commands. Selects the logical drive.

**EC** Enable Count control bit set in the VERIFY command. When this bit is 1, SC (Sectors to read Count) command byte is required.

**EIS** Enable Implied Seeks. Set in the CONFIGURE command.

**EOT** End of Track parameter set in read, write, scan, and VERIFY commands.

**ETR** Extended Track Range set in the MODE command.

**FIFO** First-In First-Out buffer. Also a control bit set in the CONFIGURE command to enable or disable the FIFO.

**FRD** FIFO Read Disable control bit set in the MODE command

**FWR** FIFO Write disable control bit set in the MODE command.

**Gap 2** The length of gap 2 in the FORMAT TRACK command and the portion of it that is rewritten in the WRITE DATA command depend on the drive mode, i.e., perpendicular or conventional. Figure 58 on page 99 illustrates gap 2 graphically. For more details, see “Bits 1,0 - Group Drive Mode Configuration (GDC)” on page 105.

**Gap 3** Gap 3 is the space between sectors, excluding the synchronization field. It is defined in the FORMAT TRACK command. See Figure 58 on page 99.

**GDC** Group Drive Configuration for all drives. Configures all logical drives as conventional or perpendicular. Used in the PERPENDICULAR MODE command. Formerly, GAP2 and WG.

**HD** Head Select control bit used in most commands. Selects Head 0 or 1 of the disk.

**IAF** Index Address Field control bit set in the MODE command. Enables the ISO Format during the FORMAT command.

**IPS** Implied Seek enable bit set in the MODE, read, write, and scan commands.

**LOCK** Lock enable bit in the LOCK command. Used to prevent certain parameters from being affected by a software reset.

**LOW PWR**
Low Power control bits set in the MODE command.

**MFM** Modified Frequency Modulation parameter used in FORMAT TRACK, read, VERIFY and write commands.

**MFT** Motor Off Time. Now called Delay After Processing time. This delay is set by the SPECIFY command.

**MNT** Motor On Time. Now called Delay Before Processing time. This delay is set by the SPECIFY command.

**MSB** Most Significant Byte controls which whether the most or least significant byte is read or written in the SET TRACK command.

**MT** Multi-Track enable bit used in read, write, scan and VERIFY commands.

**OW** Overwrite control bit set in the PERPENDICULAR MODE command.

**POLL** Enable Drive Polling bit set in the CONFIGURE command.

**PRETRK**
Precompensation Track Number set in the CONFIGURE command

**PTR** Present Track number. Contains the internal 8-bit track number or the least significant byte of the 12-bit track number of one of the four logical disk drives. PTR is set in the SET TRACK command.

**R255** Recalibration control bit set in MODE command. Sets maximum number of $\overline{\text{STEP}}$ pulses during RECALIBRATE command to 255.

**RTN** Relative Track Number used in the RELATIVE SEEK command.

**SC** Sector Count control bit used in the VERIFY command.

**SK** Skip control bit set in read and scan and VERIFY operations.

**SRT** Step Rate Time set in the SPECIFY command. Determines the time between $\overline{\text{STEP}}$ pulses for SEEK and RECALIBRATE operations.

**ST0-3**
Result phase Status registers 3-0 that contain status information about the execution of a command. See Sections 3.5.1 through 3.5.4.

**THRESH**
FIFO threshold parameter set in the CONFIGURE command

**TMR** Timer control bit set in the MODE command. Affects the timers set in the SPECIFY command.

**WG** Formerly, the Write Gate control bit. Now included in the Group Drive mode Configuration (GDC) bits in the PERPENDICULAR MODE command.

**WLD** Wildcard bit in the MODE command used to enable or disable the wildcard byte (FF) during scan commands.

**WNR** Write Number controls whether to read an existing track number or to write a new one in the SET TRACK command.

### 3.6.2 The CONFIGURE Command

The CONFIGURE command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power up.

The bits in the CONFIGURE registers are set to their default values after a hardware reset.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | EIS | FIFO | POLL | Threshold (THRESH) | | | |
| Precompensation Track Number (PRETRK) | | | | | | | |

**Third Command Phase Byte**

**Bits 3-0 - The FIFO Threshold (THRESH)**

These bits specify the threshold of the FIFO during the execution phase of read and write data transfers.

This value is programmable from 00 to 0F hex. A software reset sets this value to 00 if the LOCK bit (bit 7 of the opcode of the LOCK command) is 0. If the LOCK bit is 1, THRESH retains its value.

Use a high value of THRESH for systems that respond slowly and a low value for fast systems.

**Bit 4 - Disable Drive Polling (POLL)**

This bit enables and disabled drive polling. A software reset clears this bit to 0.

When drive polling is enabled, an interrupt is generated after a reset.

When drive polling is disabled, if the CONFIGURE command is issued within 500 msec of a hardware or software reset, then an interrupt is not generated. In addition, the four SENSE INTERRUPT commands to clear the Ready Changed State of the four logical drives is not required.

0 - Enable drive polling. (Default)

1 - Disable drive polling.

**Bit 5 - Enable FIFO (FIFO)**

This bit enables and disables the FIFO for execution phase data transfers.

If the LOCK bit (bit 7 of the opcode of the LOCK command) is 0, a software reset disables the FIFO, i.e., sets this bit to 1.

If the LOCK bit is 1, this bit retains its previous value after a software reset.

0 - FIFO enabled for read and write operations.

1 - FIFO disabled. (Default)

**Bit 6 - Enable Implied Seeks (EIS)**

This bit enables or disables implied seek operations. A software reset disables implied seeks, i.e., clears this bit to 0.

Bit 5 of the MODE command (Implied Seek (IPS) can override the setting of this bit and enable implied seeks even if they are disabled by this bit.

When implied seeks are enabled, a seek or sense interrupt operation is performed before execution of the read, write, scan, or verify operation.

0 - Implied seeks disabled. The MODE command can still enable implied seek operations. (Default)

1 - Implied seeks enabled for read, write, scan and VERIFY operations, regardless of the value of the IPS bit in the MODE command.

**Fourth Command Phase Byte, Bits 7-0, Precompensation Track Number (PRETRK)**

This byte identifies the starting track number for write precompensation. The value of this byte is programmable from track 0 (00 hex) to track 255 (FF hex).

If the LOCK bit (bit 7 of the opcode of the LOCK command) is 0, after a software reset this byte indicates track 0 (00 hex).

If the LOCK bit is 1, PRETRK retains its previous value after a software reset.

## Execution Phase

Internal registers are written.

## Result Phase

None.

### 3.6.3 The DUMPREG Command

The DUMPREG command supports system run-time diagnostics, and application software development and debugging.

DUMPREG has a one-byte command phase (the opcode) and a 10-byte result phase, which returns the values of parameters set in other commands. See the commands that set each parameter for a detailed description of the parameter.

#### Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

#### Execution Phase

Internal registers read.

#### Result Phase

After a hardware or software reset, parameters in this phase are reset to their default values. Some of these parameters are unaffected by a software reset, depending on the state of the LOCK bit.

See the command that determines the setting for the bit or field for details.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Byte of Present Track Number (PTR) Drive 0 | | | | | | | |
| Byte of Present Track Number (PTR) Drive 1 | | | | | | | |
| Byte of Present Track Number (PTR) Drive 2 | | | | | | | |
| Byte of Present Track Number (PTR) Drive 3 | | | | | | | |
| Step Rate Time (SRT) | | | | Delay After Processing | | | |
| Delay Before Processing | | | | | | | DMA |
| Sectors per Track or End of Track (EOT) Sector # | | | | | | | |
| LOCK | 0 | DC3 | DC2 | DC1 | DC0 | GDC | |
| 0 | EIS | FIFO | POLL | THRESH | | | |
| Precompensation Track Number (PRETRK) | | | | | | | |

**First through Fourth Result Phase Bytes, Bits 7-0, Present Track Number (PTR) Drives 3-0**

Each of these bytes contains either the internal 8-bit track number or the least significant byte of the 12-bit track number of the corresponding logical disk drive.

**Fifth and Sixth Result Phase Bytes, Bits 7-0, Step Rate Time, Motor Off Time, Motor On Time and DMA**

These fields are all set by the SPECIFY command. See Section 3.6.21 on page 116.

**Seventh Result Phase Byte - Sectors Per Track or End of Track (EOT)**

This byte varies depending on what commands have been previously executed.

If the last command issued was a FORMAT TRACK command, and no read or write commands have been issued since then, this byte contains the sectors per track value.

If a read or a write command was executed more recently than a FORMAT TRACK command, this byte specifies the number of the sector at the End of the Track (EOT).

**Eighth Result Phase Byte**

**Bit 7 - LOCK**

This bit controls how the other bits in this command respond to a software reset. See page 100.

The value of this is determined by bit 7 of the opcode of the LOCK command.

0 -Bits in this command are set to their default values after a software reset. (Default)

1 - Bits in this command are unaffected by a software reset.

**Bits 5-0 - DC3-0, GDC**

Bits 5-0 of the second command phase byte of the PERPENDICULAR MODE command set bits 5-0 of this byte. See page 105.

**Ninth and Tenth Result Phase Bytes**

These bytes reflect the values in the third and fourth command phase bytes of the CONFIGURE command. See page 94.

### 3.6.4 The FORMAT TRACK Command

This command formats one track on the disk in IBM, ISO, or Toshiba perpendicular format.

After a pulse from the $\overline{\text{INDEX}}$ signal is detected, data patterns are written on the disk including all gaps, Address Marks (AMs), address fields and data fields. See Figure 58.

The format of the track is determined by the following parameters:

- The MFM bit in the opcode (first command) byte, which indicates the type of the disk drive and the data transfer rate and determines the format of the address marks and the encoding scheme.
- The Index Address Format (IAF) bit (bit 6 in the second command phase byte) in the MODE command, which selects IBM or ISO format.
- The Group Drive Configuration (GDC) bits in the PERPENDICULAR MODE command, which select either conventional or Toshiba perpendicular format.
- A bytes-per-sector code, which determines the sector size. See Table 44 on page 97.
- A sectors per track parameter, which specifies how many sectors are formatted on the track.
- The data pattern byte, which is used to fill the data field of each sector.

Table 45 shows typical values for these parameters for specific PC compatible diskettes.

To allow flexible formatting, the microprocessor must supply the four address field bytes (track number, head number, sector number, bytes-per-sector code) for each sector formatted during the execution phase. This allows non-sequential sector interleaving.

This transfer of bytes from the microprocessor to the controller can be done in DMA or non-DMA mode (See Section 3.4.2 on page 85), with the FIFO enabled or disabled.

The FORMAT TRACK command terminates when a pulse from the $\overline{\text{INDEX}}$ signal is detected a second time, at which point an interrupt is generated.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | MFM | 0 | 0 | 1 | 1 | 0 | 1 |
| X | X | X | X | X | HD | DS1 | DS0 |
| Bytes-Per-Sector Code | | | | | | | |
| Sectors per Track | | | | | | | |
| Bytes in Gap 3 | | | | | | | |
| Data Pattern | | | | | | | |

**First Command Phase Byte, Opcode**

**Bit 6 - Modified Frequency Modulation (MFM)**

This bit indicates the type of the disk drive and the data transfer rate, and determines the format of the address marks and the encoding scheme.

0 - FM mode, i.e., single density.

1 - MFM mode, i.e., double density.

**Second Command Phase Byte**

**Bits 1,0 - Logical Drive Select (DS1,0)**

These bits indicate which logical drive is active. They reflect the values of bits 1,0 of the Digital Output Register (DOR) described on page 88 and of result phase status registers 0 and 3 (ST0 and ST3) described on pages 88 and 91, respectively.

00 - Drive 0 is selected. (Default)

01 - Drive 1 is selected.

10 - If four drives are supported, or drives 2 and 0 are exchanged, drive 2 is selected.

11 - If four drives are supported, drive 3 is selected.

**Bit 2 - Head Select (HD)**

This bit indicates which side of the Floppy Disk Drive (FDD) is selected by the head. Its value is the inverse of the $\overline{\text{HDSEL}}$ disk interface output signal.

This bit reflects the value of bit 3 of Status Register A (SRA) described on page 76 and bit 2 of result phase status registers 0 and 3 (ST0 and ST3) described on pages 88 and 91, respectively.

0 - $\overline{\text{HDSEL}}$ is not active, i.e., the head of the FDD selects side 0. (Default)

1 - $\overline{\text{HDSEL}}$ is active, i.e., the head of the FDD selects side 1.

**Third Command Phase Byte - Bytes-Per-Sector Code**

This byte contains a code in hexadecimal format that indicates the number of bytes in a data field.

Table 44 shows the number of bytes in a data field for each code.

**TABLE 44. Bytes per Sector Codes**

| Bytes-Per-Sector Code (hex) | Bytes in Data Field |
|---|---|
| 00 | 128 |
| 01 | 256 |
| 02 | 512 |
| 03 | 1024 |
| 04 | 2048 |
| 05 | 4096 |
| 06 | 8192 |
| 07 | 16384 |

**Fourth Command Phase Byte - Sectors Per Track**

The value in this byte specifies how many sectors there are in the track.

**Fifth Command Phase Byte - Bytes in Gap 3**

The number of bytes in gap 3 is programmable. The number to program for Gap 3 depends on the data transfer rate and the type of the disk drive. Table 46 shows some typical values to use for Gap 3.

Figure 58 illustrates the track format for each of the formats recognized by the FORMAT TRACK command.

**Sixth Command Phase Byte - Data Pattern**

This byte contains the contents of the data field.

## Execution Phase

The system transfers four ID bytes (track number, head number, sector number and bytes-per-sector code) per sector to the Floppy Disk Controller (FDC) in either a DMA or a non-DMA mode. Section 3.4.2 on page 85 describes these modes.

The entire track is formatted. The data block in the data field of each sector is filled with the data pattern byte.

Only the first three status bytes in this phase are significant.

**TABLE 45. Typical Values for PC Compatible Diskette Media**

| Media Type | Bytes in Data Field (decimal) | Bytes-Per-Sector Code (hex) | End of Track (EOT) Sector # (hex) | Bytes in Gap 2 [a] (hex) | Bytes in Gap 3 [b] (hex) |
|---|---|---|---|---|---|
| 360 KB | 512 | 02 | 09 | 2A | 50 |
| 1.2 MB | 512 | 02 | 0F | 1B | 54 |
| 720 KB | 512 | 02 | 09 | 1B | 50 |
| 1.44 MB | 512 | 02 | 12 | 1B | 6C |
| 2.88 MB[c] | 512 | 02 | 24 | 1B | 53 |

a. Gap 2 is specified in the command phase of read, write, scan, and verify commands. Although this is the recommended value, the FDC ignores this byte in read, write, scan and verify commands.

b. Gap 3 is the suggested value for the programmable GAP3 that is used in the FORMAT TRACK command and is illustrated in Figure 58.

c. The 2.88 MB diskette media is a barium ferrite media intended for use in perpendicular recording drives at the data rate of up to 1 Mbps.

**TABLE 46. Typical Gap Values**

| Drive Type and Data Transfer Rate | Bytes in Data Field (decimal) | Bytes-Per-Sector Code (hex) | End of Track (EOT) Sector # (hex) | Bytes in Gap 2 [a] (hex) | Bytes in Gap 3 [b] (hex) |
|---|---|---|---|---|---|
| 125 Kbps FM | 128 | 00 | 12 | 07 | 09 |
| | 128 | 00 | 10 | 10 | 19 |
| | 256 | 01 | 08 | 18 | 30 |
| | 512 | 02 | 04 | 46 | 87 |
| | 1024 | 03 | 02 | C8 | FF |
| | 2048 | 04 | 01 | C8 | FF |
| 250 Kbps MFM | 256 | 01 | 12 | 0A | 0C |
| | 256 | 01 | 10 | 20 | 32 |
| | 512 | 02 | 08 | 2A | 50 |
| | 512 | 02 | 09 | 2A | 50 |
| | 1024 | 03 | 04 | 80 | F0 |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |
| 250 Kbps FM | 128 | 00 | 1A | 07 | 1B |
| | 256 | 01 | 0F | 0E | 2A |
| | 512 | 02 | 08 | 1B | 3A |
| | 1024 | 03 | 04 | 47 | 8A |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |
| 500 Kbps MFM | 256 | 01 | 1A | 0E | 36 |
| | 512 | 02 | 0F | 1B | 54 |
| | 512 | 02 | 12 | 1B | 6C |
| | 1024 | 03 | 08 | 35 | 74 |
| | 2048 | 04 | 04 | 99 | FF |
| | 4096 | 05 | 02 | C8 | FF |
| | 8192 | 06 | 01 | C8 | FF |

a. Gap 2 is specified in the command phase of read, write, scan, and verify commands. Although this is the recommended value, the FDC ignores this byte in read, write, scan and verify commands.

b. Gap 3 is the suggested value for use in the FORMAT TRACK command. This is the programmable Gap 3 illustrated in Figure 58.

A1* = Data Pattern of A1, Clock Pattern of 0A. All other data rates use gap 2 = 22 bytes.
C2* = Data Pattern of C2, Clock Pattern of 14

**FIGURE 58. IBM, Perpendicular, and ISO Formats Supported by FORMAT TRACK Command**

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Undefined | | | | | | | |
| Undefined | | | | | | | |
| Undefined | | | | | | | |
| Undefined | | | | | | | |

### 3.6.5 The INVALID Command

If an invalid command (illegal opcode byte in the command phase) is received by the Floppy Disk Controller (FDC), the controller responds with the result phase Status register 0 (ST0) in the result phase. See "Result Phase Status Register 0 (ST0)" on page 88

The controller does not generate an interrupt during this condition. Bits 7 and 6 in the MSR (see Section 3.3.6 page 80) are both set to 1, indicating to the microprocessor that the controller is in the result phase and the contents of ST0 must be read.

#### Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Invalid Opcodes | | | | | | | |

#### Execution Phase

None.

#### Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (STO) (80 hex) | | | | | | | |

The system reads 80 (hex) from ST0 indicating that an invalid command was received.

### 3.6.6 The LOCK Command

The LOCK command can be used to keep the FIFO enabled and to retain the values of some parameters after a software reset.

After the command byte of the LOCK command is written, its result byte must be read before the opcode of the next command can be read. The LOCK command is not executed until its result byte is read by the microprocessor.

If the part is reset after the command byte of the LOCK command is written but before its result byte is read, then the LOCK command is not executed. This prevents accidental execution of the LOCK command.

#### Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LOCK | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

**Bit 7 - Control Reset Effect (LOCK)**

This bit determines how the FIFO, THRESH, and PRETRK bits in the CONFIGURE command and, the FWR, FRD, and BST bits in the MODE command are affected by a software reset.

0 -Set default values after a software reset. (Default)

1 - Values are unaffected by a software reset.

#### Execution Phase

Internal register is written.

#### Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | LOCK | 0 | 0 | 0 | 0 |

**Bit 4 - Control Reset Effect (LOCK)**

Same as bit 7 of opcode in command phase.

### 3.6.7 The MODE Command

This command selects the special features of the controller. The bits in the command bytes of the MODE command are set to their default values after a hardware reset.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| TMR | IAF | IPS | 0 | LOW PWR | | 0 | ETR |
| FWR | FRD | BST | R255 | 0 | 0 | 0 | 0 |
| DENSEL | | BFR | WLD | Head Settle Factor | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Second Command Phase Byte**

**Bit 0 - Extended Track Range (ETR)**

This bit determines how the track number is stored. It is cleared to 0 after a software reset.

0 - Track number is stored as a standard 8-bit value compatible with the IBM, ISO, and Toshiba Perpendicular formats.

This allows access of up to 256 tracks during a seek operation. (Default)

1 - Track number is stored as a 12-bit value.

The upper four bits of the track value are stored in the upper four bits of the head number in the sector address field.

This allows access of up to 4096 tracks during a seek operation. With this bit set, an extra byte is required in the SEEK command phase and SENSE INTERRUPT result phase.

**Bits 3,2 - Low-Power Mode (LOW PWR)**

These bits determine whether or not the FDC powers down and, if it does, they specific how long it will take.

These bits disable power down, i.e., are cleared to 0, after a software reset.

00 - Disables power down. (Default)

01 - Automatic power down.

At a 500 Kbps data transfer rate, the FDC will go into low-power mode 512 msec after it becomes idle.

At a 250 Kbps data transfer rate, the FDC will go into low-power mode 1 second after it becomes idle.

10 - Manual power down.

The FDC powers down mode immediately.

11 - Not used.

**Bit 5 - Implied Seek (IPS)**

This bit determines whether the Implied Seek (IPS) bit in a command phase byte of a read, write, scan, or verify command is ignored or READ.

A software reset clears this bit to its default value of 0.

0 - The IPS bit in the command byte of a read, write, scan, or verify is ignored. (Default)

Implied seeks can still be enabled by the Enable Implied Seeks (EIS) bit (bit 6 of the third command phase byte) in the CONFIGURE command.

1 - The IPS bit in the command byte of a read, write, scan, or verify is read.

If it is set to 1, the controller performs seek and sense interrupt operations before executing the command.

**Bit 6 - Index Address Format (IAF)**

This bit determines whether the controller formats tracks with or without an index address field.

A software reset clears this bit to its default value of 0.

0 - The controller formats tracks with an index address field. (IBM and Toshiba Perpendicular format).

1 - The controller formats tracks without an index address field. (ISO format).

**Bit 7 - Motor Timer Values (TMR)**

This bit determines which group of values to use to calculate the Delay Before Processing and Delay After Processing times. The value of each is programmed using the SPECIFY command, which is described on page 116 and in Tables 58 and 59.

A software reset clears this bit to its default value of 0.

0 - Use the TMR = 0 group of values. (Default)

1 - Use the TMR = 1 group of values.

**Third Command Phase Byte**

**Bit 4 - RECALIBRATE Step Pulses (R255)**

This bit determines the maximum number of RECALIBRATE step pulses the controller issues before terminating with an error, depending on the value of the Extended Track Range (ETR) bit, i.e., bit 0 of the second command phase byte in the MODE command.

A software reset clears this bit to its default value of 0.

0 - If ETR (bit 0) = 0, the controller issues a maximum of 85 recalibration step pulses.

If ETR (bit 0) = 1, the controller issues a maximum of 3925 recalibration step pulses. (Default)

1 - If ETR (bit 0) = 0, the controller issues a maximum of 255 recalibration step pulses.

If ETR (bit 0) = 1, the controller issues a maximum of 4095 recalibration step pulses.

**Bit 5 - Burst Mode Disable (BST)**

This bit enables or disables burst mode, if the FIFO is enabled (bit 5 in the CONFIGURE command is 0). If the FIFO is not enabled in the CONFIGURE command, then the value of this bit is ignored.

A software reset enables burst mode, i.e., clears this bit to its default value of 0, if the LOCK bit (bit 7 of the opcode of the LOCK command) is 0. If it is 1, BST retains its value after a software reset.

0 - Burst mode enabled for FIFO execution phase data transfers. (Default)

1 - Burst mode disabled.

The FDC issues one DRQ or IRQ6 pulse for each byte to be transferred while the FIFO is enabled.

**Bit 6 - FIFO Read Disable (FRD)**

This bit enables or disables the FIFO for microprocessor read transfers from the controller, if the FIFO is enabled (bit 5 in the CONFIGURE command is 0). If the FIFO is not enabled in the CONFIGURE command, then the value of this bit is ignored.

A software reset enables the FIFO for reads, i.e., clears this bit to its default value of 0, if the LOCK bit (bit 7 of the opcode of the LOCK command) is 0. If it is 1, FRD retains its value after a software reset.

0 - Enable FIFO. Execution phase of microprocessor read transfers use the internal FIFO. (Default)

1 - Disable FIFO. All read data transfers take place without the FIFO.

**Bit 7 - FIFO Write Enable or Disable (FWR)**

This bit enables or disables write transfers to the controller, if the FIFO is enabled (bit 5 in the CONFIGURE command is 0). If the FIFO is not enabled in the CONFIGURE command, then the value of this bit is ignored.

A software reset enables the FIFO for writes, i.e., clears this bit to its default value of 0, if the LOCK bit (bit 7 of the opcode of the LOCK command) is 0. If it is 1, FWR retains its value after a software reset.

0 - Enable FIFO. Execution phase microprocessor write transfers use the internal FIFO. (Default)

1 - Disable FIFO. All write data transfers take place without the FIFO.

**Fourth Command Phase Byte**

**Bits 3-0 - Head Settle Factor**

This field is used to specify the maximum time allowed for the read/write head to settle after a seek during an implied seek operation.

The value specified by these bits (the head settle factor) is multiplied by the multiplier for selected data rate to specify a head settle time that is within the range for that data rate.

Use the following formula to determine the head settle factor that these bits should specify:

*Head Settle Factor x Multiplier = Head Settle Time*

Table 47 shows the multipliers and head settle time ranges for each data transfer rate.

The default head settle factor, i.e., value for these bits, is 8.

**TABLE 47. Multipliers and Head Settle Time Ranges for Different Data Transfer Rates**

| Data Transfer Rate (Kbps) | Multiplier | Head Settle Time Range (msec) |
|---|---|---|
| 250 | 8 | 0 - 120 |
| 300 | 6.666 | 0 - 100 |
| 500 | 4 | 0 - 60 |
| 1000 | 2 | 0 - 30 |

**Bit 4 - Scan Wild Card (WLD)**

This bit determines whether or not FF (hex) from either the microprocessor or the disk will be recognized during a scan command as a wildcard character.

0 - An FF (hex) from either the microprocessor or the disk during a scan command is interpreted as a wildcard character that always matches. (Default)

1 - The scan commands do not recognize FF (Hex) as a wildcard character.

**Bit 5 - CMOS Disk Interface Buffer Enable (BFR)**

This bit configures drive output signals.

0 - Drive output signals are configured as standard 4 mA push-pull output signals (40 mA sink, 4 mA source). (Default)

1 - Drive output signals are configured as 40 mA open-drain output signals.

**Bits 7,6 - Density Select Pin Configuration (DENSEL)**

This field can configure the polarity of the Density Select output signal (DENSEL) as always low or always high, as shown in Table 4-3. This allows the user more flexibility with new drive types.

This field overrides the DENSEL polarity defined by the DENSEL polarity bit of the Advanced SuperI/O Chip (ASC) configuration register described on page 53.

00 - The DENSEL signal is always low.

01 - The DENSEL signal is always high.

10 - The DENSEL signal is undefined.

11 - The polarity of the DENSEL signal is defined by the DENSEL Polarity bit (bit 6) of the ASC register. See page 53. (Default)

**TABLE 48. DENSEL Encoding**

| Bit 7 | Bit 6 | DENSEL Pin Definition |
|---|---|---|
| 0 | 0 | DENSEL low |
| 0 | 1 | DENSEL high |
| 1 | 0 | undefined |
| 1 | 1 | Set by ASC register. |

## Execution Phase

Internal registers are written.

## Result Phase

None.

## 3.6.8 The NSC Command

The NSC command can be used to distinguish between the FDC versions and the 82077.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

## Execution Phase

## Result Phase

The result phase byte of the NSC command identifies the floppy disk controller (FDC) as a PC87338/PC97338 by returning a value of 73h.

The 82077 and DP8473 return the value 80 hex, signifying an invalid command.

Bits 3-0 of this result byte are subject to change by NSC, and specify the version of the Floppy Disk Controller (FDC).

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |

### 3.6.9 The PERPENDICULAR MODE Command

The PERPENDICULAR MODE command configures each of the four logical disk drives for perpendicular or conventional mode via the logical drive configuration bits 1,0 or 5-2, depending on the value of bit 7. The default mode is conventional. Therefore, if the drives in the system are conventional, it is not necessary to issue a PERPENDICULAR MODE command.

This command supports the unique FORMAT TRACK and WRITE DATA requirements of perpendicular (vertical) recording disk drives with a 4 MB unformatted capacity.

Perpendicular recording drives operate in extra high density mode at 1 or 2 Mbps, and are downward compatible with 1.44 MB and 720 KB drives at 500 kbps (high density) and 250 kbps (double density), respectively.

If the system includes perpendicular drives, this command should be issued during initialization of the FDC. Then, when a drive is accessed for a FORMAT TRACK or WRITE DATA command, the FDC adjusts the command parameters based on the data rate. See Table 49.

Precompensation is set to zero for perpendicular drives at any data rate.

Perpendicular recording type disk drives have a pre-erase head that leads the read or write head by 200 µm, which translates to 38 bytes at a 1 Mbps data transfer rate (19 bytes at 500 Kbps).

The increased space between the two heads requires a larger gap 2 between the address field and data field of a sector at 1 or 2 Mbps. See Perpendicular Format in Figure 58. A gap 2 length of 41 bytes (at 1 or 2 Mbps) ensures that the preamble in the data field is completely pre-erased by the pre-erase head.

Also, during WRITE DATA operations to a perpendicular drive, a portion of gap 2 must be rewritten by the controller to guarantee that the data field preamble has been pre-erased. See Table 49.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| OW | 0 | DC3 | DC2 | DC1 | DC0 | GDC | |

**TABLE 49. Effect of Drive Mode and Data Rate on FORMAT TRACK and WRITE DATA Commands**

| Data Rates | Drive Mode | Length of Gap 2 in FORMAT TRACK Command | Portion of Gap 2 Rewritten in WRITE DATA Command |
|---|---|---|---|
| 250, 300 or 500 Kbps | Conventional | 22 bytes | 0 bytes |
| | Perpendicular | 22 bytes | 19 bytes |
| 1 or 2 Mbps | Conventional | 22 bytes | 0 bytes |
| | Perpendicular | 41 bytes | 38 bytes |

**TABLE 50. Effect of GDC Bits on FORMAT TRACK and WRITE DATA Commands**

| GDC Bits | | Drive Mode | Length of Gap 2 in FORMAT TRACK Command | Portion of Gap 2 Rewritten in WRITE DATA Command |
|---|---|---|---|---|
| 1 | 0 | | | |
| 0 | 0 | Conventional | 22 bytes | 0 bytes |
| 0 | 1 | Perpendicular (≤500 Kbps) | 22 bytes | 19 bytes |
| 1 | 0 | Conventional | 22 bytes | 0 bytes |
| 1 | 1 | Perpendicular (1 or 2 Mbps) | 41 bytes | 38 bytes |

**Second Command Phase Byte**

A hardware reset clears all the bits to zero (conventional mode for all drives). PERPENDICULAR MODE command bits may be written at any time.

The settings of bits 1 and 0 in this byte override the logical drive configuration set by bits 5 through 2. If bits 1 and 0 are both 0, bits 5 through 2 configure the logical disk drives as conventional or perpendicular. Otherwise, bits 2 and 0 configure them. See Table 50.

**Bits 1,0 - Group Drive Mode Configuration (GDC)**

These bits configure all the logical disk drives as conventional or perpendicular. If the Overwrite bit (OW, bit 7) is 0, this setting may be overridden by bits 5-2.

It is not necessary to issue the FORMAT TRACK command if all drives are conventional.

These bits are cleared to 0 by a software reset.

00 - Conventional. (Default)

01 - Perpendicular. (500 Kbps)

10 - Conventional.

11 - Perpendicular. (1 or 2 Mbps)

**Bits 5-2 -Drive 3-0 Mode Configuration (DC3-0)**

If bits 1,0 are both 0, and bit 7 is 1, these bits configure logical drives 3-0 as conventional or perpendicular. Bits 5-2 (DC3–0) correspond to logical drives 3-0, respectively.

These bits are not affected by a software reset.

0 - Conventional drive. (Default)

It is not necessary to issue the FORMAT TRACK command for conventional drives.

1 - Perpendicular drive.

**Bit 7 - Overwrite (OW)**

This bit enables or disables changes in the mode of the logical drives by bits 5-2.

0 - Changes in mode of logical drives via bits 5-2 are ignored. (Default)

1 - Changes enabled.

## Execution Phase

Internal registers are written.

## Result Phase

None.

## 3.6.10 The READ DATA Command

The READ DATA command reads logical sectors that contain a normal data address mark from the selected drive and makes the data available to the host microprocessor.

## Command Phase

The READ DATA command phase bytes must specify the following ID information for the desired sector:

- Track number
- Head number
- Sector number
- Bytes-per-sector code (See Table 44.)
- End of Track (EOT) sector number. This allows the controller to read multiple sectors.
- The value of the data length byte is ignored and must be set to FF (hex).

After the last command phase byte is written, the controller waits the Delay Before Processing time (see Table 59 on page 117) for the selected drive. During this time, the drive motor must be turned on by enabling the appropriate drive and motor select disk interface output signals via the bits of the Digital Output Register (DOR). See “Digital Output Register (DOR), Offset 010” on page 77.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | SK | 0 | 0 | 1 | 1 | 0 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Data Length (Obsolete) | | | | | | | |

**First Command Phase Byte**

**Bit 5 - Skip Control (SK)**

This controls whether or not sectors containing a deleted address mark will be skipped during execution of the READ DATA command. See Table 51.

0 - Do not skip sector with deleted address mark.

1 - Skip sector with deleted address mark.

**Bit 6 - Modified Frequency Modulation (MFM)**

This bit indicates the type of the disk drive and the data transfer rate, and determines the format of the address marks and the encoding scheme.

0 - FM mode, i.e., single density.

1 - MFM mode, i.e., double density.

**Bit 7 - Multi-Track (MT)**

This bit controls whether or not the controller continues to side 1 of the disk after reaching the last sector of side 0.

0 - Single track. The controller stops at the last sector of side 0.

1 - Multiple tracks. the controller continues to side 1 after reaching the last sector of side 0.

**Second Command Phase Byte**

**Bits 1,0 - Logical Drive Select (DS1,0)**

These bits indicate which logical drive is active. See “Bits 1,0 - Logical Drive Select (DS1,0)” on page 96.

00 - Drive 0 is selected. (Default)

01 - Drive 1 is selected.

10 - If four drives are supported, or drives 2 and 0 are exchanged, drive 2 is selected.

11 - If four drives are supported, drive 3 is selected.

**Bit 2 - Head (HD)**

This bit indicates which side of the Floppy Disk Drive (FDD) is selected by the head. Its value is the inverse of the $\overline{\text{HDSEL}}$ disk interface output signal.See “Bit 2 - Head Select (HD)” on page 96.

0 - $\overline{\text{HDSEL}}$ is not active, i.e., the head of the FDD selects side 0. (Default)

1 - $\overline{\text{HDSEL}}$ is active, i.e., the head of the FDD selects side 1.

**Bit 7 - Implied Seek (IPS)**

This bit indicates whether or not an implied seek should be performed. See also, “Bit 5 - Implied Seek (IPS)” on page 101.

0 - No implied seek operations. (Default)

1 - The controller performs seek and sense interrupt operations before executing the command.

**Third Command Phase Byte - Track Number**

The value in this byte specifies the number of the track to read.

**Fourth Command Phase Byte - Head Number**

The value in this byte specifies head to use.

**Fifth Command Phase Byte - Sector Number**

The value in this byte specifies the sector to read.

**Sixth Command Phase Byte - Bytes-Per-Sector Code**

This byte contains a code in hexadecimal format that indicates the number of bytes in a data field. Table 44 on page 97 indicates the number of bytes that corresponds to each code.

**Seventh Command Phase Byte - Bytes Between Sectors - Gap 3**

The value in this byte specifies how many bytes there are between sectors. See “Fifth Command Phase Byte - Bytes in Gap 3” on page 97.

**Eighth Command Phase Byte - Data Length (Obsolete)**

The value in this byte is ignored and must be set to FF (hex).

## Execution Phase

In this phase, data read from the disk drive is transferred to the system via DMA or non-DMA modes. See 3.4.2 on page 85.

The controller looks for the track number specified in the third command phase byte. If implied seeks are enabled, the controller also performs all operations of a SENSE INTERRUPT command and of a SEEK command (without issuing these commands). Then, the controller waits the head settle time. See bits 3-0 of the fourth command phase byte of the MODE command on page 102.

The controller then starts the data separator and waits for the data separator to find the address field of the next sector. The controller compares the ID information (track number, head number, sector number, bytes-per-sector code) in that address field with the corresponding information in the command phase bytes of the READ DATA command.

If the contents of the bytes do not match, then the controller waits for the data separator to find the address field of the next sector. The process is repeated until a match or an error occurs.

Possible errors, the conditions that may have caused them and the actions that result are:

- The microprocessor aborted the command by writing to the FIFO.

  If there is no disk in the drive, the controller gets stuck. The microprocessor must then write a byte to the FIFO to advance the controller to the result phase.

- Two pulses of the $\overline{\text{INDEX}}$ signal were detected since the search began, and no valid ID was found.

If the track address differs, either the Wrong Track bit (bit 4) or the Bad Track bit (bit 1) (if the track address is FF hex) is set in result phase Status register 2 (ST2). See Section 3.5.3 on page 90.

If the head number, sector number or bytes-per-sector code did not match, the Missing Data bit (bit 2) is set in result phase Status register 1 (ST1).

If the Address Mark (AM) was not found, the Missing Address Mark bit (bit 0) is set in ST1.

Section 3.5.2 on page 89 describes the bits of ST1.

- A CRC error was detected in the address field. In this case the CRC Error bit (bit 5) is set in ST1.

Once the address field of the desired sector is found, the controller waits for the data separator to find the data field for that sector.

If the data field (normal or deleted) is not found within the expected time, the controller terminates the operation, enters the result phase and sets bit 0 (Missing Address Mark) in ST1.

If a deleted data mark is found, and Skip (SK) control is set to 1 in the opcode command phase byte, the controller skips this sector and searches for the next sector address field as described above. The effect of Skip Control (SK) on the READ DATA command is summarized in Table 51.

**TABLE 51. Skip Control Effect on READ DATA Command**

| Skip Control (SK) | Data Type | Sector Read? | Control Mark Bit 6 of ST2 | Result |
|---|---|---|---|---|
| 0 | Normal | Y | 0 | Normal Termination |
| 0 | Deleted | Y | 1 | No More Sectors Read |
| 1 | Normal | Y | 0 | Normal Termination |
| 1 | Deleted | N | 1 | Sector Skipped |

After finding the data field, the controller transfers data bytes from the disk drive to the host until the bytes-per-sector count has been reached, or until the host terminates the operation by issuing the Terminal Count (TC) signal, reaching the end of the track or reporting an overrun.

See also, Section “The Phases of FDC Commands” on page 85.

The controller then generates a Cyclic Redundancy Check (CRC) value for the sector and compares the result with the CRC value at the end of the data field.

After reading the sector, the controller reads the next logical sector unless one or more of the following termination conditions occurs:

- The DMA controller asserted the Terminal Count (TC) signal to indicate that the operation terminated. The Interrupt Code (IC) bits (bits 7,6) in ST0 are set to normal termination (00). See page 89.
- The last sector address (of side 1, if the Multi-Track enable bit (MT) was set to 1) was equal to the End of Track sector number. The End of Track bit (bit 7) in ST1 is set. The IC bits in ST0 are set to abnormal termination (01). This is the expected condition during non-DMA transfers.
- Overrun error. The Overrun bit (bit 4) in ST1 is set. The Interrupt Code (IC) bits (bits 7,6) in ST0 are set to abnormal termination (01). If the microprocessor cannot service a transfer request in time, the last correctly read byte is transferred.
- CRC error. CRC Error bit (bit 5) in ST1 and CRC Error in Data Field bit (bit 5) in ST2, are set. The Interrupt Code (IC) bits (bits 7,6) in ST0 are set to abnormal termination (01).

If the Multi-Track (MT) bit was set in the opcode command byte, and the last sector of side 0 has been transferred, the controller continues with side 1.

## Result Phase

Upon terminating the execution phase of the READ DATA command, the controller asserts IRQ6, indicating the beginning of the result phase. The microprocessor must then read the result bytes from the FIFO.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

The values that are read back in the result bytes are shown in Table 52. If an error occurs, the result bytes indicate the sector read when the error occurred.

**TABLE 52. Result Phase Termination Values with No Error**

| Multi-Track (MT) | Head # (HD) | End of Track (EOT) Sector Number | ID Information in Result Phase | | | |
|---|---|---|---|---|---|---|
| | | | Track Number | Head Number | Sector Number | Bytes-per-Sector Code |
| 0 | 0 | < EOT[a] Sector # | No Change | No Change | Sector[b] # + 1 | No Change |
| 0 | 0 | = EOT[a] Sector # | Track[c] # + 1 | No Change | 1 | No Change |
| 0 | 1 | < EOT[a] Sector # | No Change | No Change | Sector[b] # + 1 | No Change |
| 0 | 1 | = EOT[a] Sector # | Track[c] # + 1 | No Change | 1 | No Change |
| 1 | 0 | < EOT[a] Sector # | No Change | No Change | Sector[b] # + 1 | No Change |
| 1 | 0 | = EOT[a] Sector # | No Change | 1 | 1 | No Change |
| 1 | 1 | < EOT[a] Sector # | No Change | No Change | Sector[b] # + 1 | No Change |
| 1 | 1 | = EOT[a] Sector # | Track[c] # + 1 | 0 | 1 | No Change |

a. End of Track sector number from the command phase.
b. The number of the sector last operated on by controller.
c. Track number programmed in the command phase

### 3.6.11 The READ DELETED DATA Command

The READ DELETED DATA command reads logical sectors containing a Address Mark (AM) for deleted data from the selected drive and makes the data available to the host microprocessor.

This command is like the READ DATA command, except for the setting of the Control Mark bit (bit 6) in ST2 and the skipping of sectors. See description of execution phase.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | SK | 0 | 1 | 1 | 0 | 0 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Data Length (Obsolete) | | | | | | | |

See READ DATA command for a description of the command bytes.

## Execution Phase

Data read from disk drive is transferred to the system in DMA or non-DMA modes. See Section 3.4.2 on page 85.

The effect of Skip Control (SK) on the READ DELETED DATA command is summarized in Table 53.

**TABLE 53. SK Effect on READ DELETED DATA Command**

| Skip Control (SK) | Data Type | Sector Read? | Control Mark Bit 6 of ST2 | Result |
|---|---|---|---|---|
| 0 | Normal | Y | 1 | No More Sectors Read |
| 0 | Deleted | Y | 0 | Normal Termination |
| 1 | Normal | N | 1 | Sector Skipped |
| 1 | Deleted | Y | 0 | Normal Termination |

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

See Table 52 for the state of the result bytes when the command terminates normally.

### 3.6.12 The READ ID Command

The READ ID command finds the next available address field and returns the ID bytes (track number, head number, sector number, bytes-per-sector code) to the microprocessor in the result phase.

The controller reads the first ID Field header bytes it can find and reports these bytes to the system in the result bytes.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | MFM | 0 | 0 | 1 | 0 | 1 | 0 |
| X | X | X | X | X | HD | DS1 | DS0 |

After the last command phase byte is written, the controller waits the Delay Before Processing time (see Table 59 on page 117) for the selected drive. During this time, the drive motor must be turned on by enabling the appropriate drive and motor select disk interface output signals via the bits of the Digital Output Register (DOR). See “Digital Output Register (DOR), Offset 010” on page 77.

#### First Command Phase Byte, Opcode

See “Bit 6 - Modified Frequency Modulation (MFM)” on page 96.

#### Second Command Phase Byte

See “Second Command Phase Byte” on page 96 for a description of the Drive Select (DS1,0) and Head Select (HD) bits.

### 3.6.13 The READ A TRACK Command

The READ A TRACK command reads sectors from the selected drive, in physical order, and makes the data available to the host.

## Execution Phase

There is no data transfer during the execution phase of this command. An interrupt is generated when the execution phase is completed.

The READ ID command does not perform an implied seek.

After waiting the Delay Before Processing time, the controller starts the data separator and waits for the data separator to find the address field of the next sector. If an error condition occurs, the Interrupt Code (IC) bits in ST0 are set to abnormal termination (01), and the controller enters the result phase.

Possible errors are:

- The microprocessor aborted the command by writing to the FIFO.

  If there is no disk in the drive, the controller gets stuck. The microprocessor must then write a byte to the FIFO to advance the controller to the result phase.

- Two pulses of the $\overline{\text{INDEX}}$ signal were detected since the search began, and no Address Mark (AM) was found.

  When the Address Mark (AM) is not found, the Missing Address Mark bit (bit 0) is set in ST1. Section 3.5.2 on page 89 describes the bits of ST1.

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | MFM | 0 | 0 | 0 | 0 | 1 | 0 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Data Length (Obsolete) | | | | | | | |

The command phase bytes of the READ A TRACK command are like those of the READ DATA command, except for the MT and SK bits. Multi-track and skip operations are not allowed in the READ A TRACK command. Therefore, bits 7 and 5 of the opcode command phase byte (MT and SK, respectively) must be 0.

**First Command Phase Byte, Opcode**

See “Bit 6 - Modified Frequency Modulation (MFM)” on page 96.

**Second Command Phase Byte**

See “Second Command Phase Byte” on page 96 for a description of the Drive Select (DS1,0) and Head Select (HD) bits.

See “Bit 5 - Implied Seek (IPS)” on page 101 for a description of the Implied Seek (IPS) bit.

**Third through Ninth Command Phase Bytes**

See “The READ DATA Command” on page 105.

## Execution Phase

Data read from the disk drive is transferred to the system in DMA or non-DMA modes. See Section 3.4.2.

Execution of this command is like execution of the READ DATA command except for the following differences:

- The controller waits for a pulse from the $\overline{\text{INDEX}}$ signal before it searches for the address field of a sector.

  If the microprocessor writes to the FIFO before the $\overline{\text{INDEX}}$ pulse is detected, the command enters the result phase with the Interrupt Code (IC) bits (bits 7,6) in ST0 set to abnormal termination (01).
- All the ID bytes of the sector address are compared, except the sector number. Instead, the sector number is set to 1, and then incremented for each successive sector read.
- If no match occurs when the ID bytes of the sector address are compared, the controller sets the Missing Data bit (bit 2) in ST1, but continues to read the sector. If there is a CRC error in the address field being read, the controller sets CRC Error (bit 5) in ST1, but continues to read the sector.
- If there is a CRC error in the data field, the controller sets the CRC Error bit (bit 5) in ST1 and CRC Error in Data Field bit (bit 5) in ST2, but continues reading sectors.
- The controller reads a maximum of End of Track (EOT) physical sectors. There is no support for multi-track reads.

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

## 3.6.14 The RECALIBRATE Command

The RECALIBRATE command issues pulses that make the head of the selected drive step out until it reaches track 0.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| X | X | X | X | X | HD | DS1 | DS0 |

**Second Command Phase Byte**

See “Second Command Phase Byte” on page 96 for a description of the Drive Select (DS1,0) and Head Select (HD) bits.

## Execution Phase

After the last command byte is issued, the Drive Busy bit for the selected drive is set in the Main Status Register (MSR). See bits 3-0 in “Main Status Register (MSR), Offset 100” on page 80.

The controller waits the Delay Before Processing time (see Table 59 on page 117) for the selected drive., and then becomes idle. See “Idle Phase” on page 88.

Then, the controller issues pulses until the $\overline{TRK0}$ disk interface input signal becomes active or until the maximum number of RECALIBRATE step pulses have been issued.

Table 54 shows the maximum number of RECALIBRATE step pulses that may be issued, depending on the RECALIBRATE Step Pulses (R255) bit, bit 0 in the second command phase byte of the MODE command (page 101), and the Extended Track Range (ETR) bit, bit 4 of the third command byte of the MODE command (page 101).

If the number of tracks on the disk drive exceeds the maximum number of RECALIBRATE step pulses, it may be necessary to issue another RECALIBRATE command.

**TABLE 54. Maximum RECALIBRATE Step Pulses for Values of R255 and ETR**

| R255 | ETR | Maximum Number of RECALIBRATE Step Pulses |
|---|---|---|
| 0 | 0 | 85 (default) |
| 1 | 0 | 255 |
| 0 | 1 | 3925 |
| 1 | 1 | 4095 |

The pulses actually occur while the controller is in the drive polling phase. See “Drive Polling Phase” on page 88.

An interrupt is generated after the $\overline{TRK0}$ signal is asserted, or after the maximum number of RECALIBRATE step pulses is issued.

Software should ensure that the RECALIBRATE command is issued for only one drive at a time. This is because the drives are actually selected via the Digital Output Register (DOR), which can only select one drive at a time.

No command, except a SENSE INTERRUPT command, should be issued while a RECALIBRATE command is in progress.

## Result Phase

None.

## 3.6.15 The RELATIVE SEEK Command

The RELATIVE SEEK command issues $\overline{STEP}$ pulses that make the head of the selected drive step in or out a programmable number of tracks.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DIR | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | HD | DS1 | DS0 |
| Relative Track Number (RTN) | | | | | | | |

**First Command Phase Byte, Opcode, Bit - 6 Step Direction DIR**

This bit defines the step direction.

0 - Step head out.

1 - Step head in.

**Second Command Phase Byte**

See “Second Command Phase Byte” on page 96 for a description of the Drive Select (DS1,0) and Head Select (HD) bits.

**Third Command Phase Byte - Relative Track Number (RTN)**

This value specifies how many tracks the head should step in or out from the current track.

## Execution Phase

After the last command byte is issued, the Drive Busy bit for the selected drive is set in the Main Status Register (MSR). See bits 3-0 in Section 3.3.6 on page 80.

The controller waits the Delay Before Processing time (see Table 59 on page 117) for the selected drive., and then becomes idle. See “Idle Phase” on page 88.

Then, the controller enters the idle phase and issues RTN $\overline{STEP}$ pulses until the $\overline{TRK0}$ disk interface input signal becomes active or until the specified number (RTN) of $\overline{STEP}$ pulses have been issued. After the RELATIVE SEEK operation is complete, the controller generates an interrupt.

Software should ensure that the RELATIVE SEEK command is issued for only one drive at a time. This is because the drives are actually selected via the Digital Output Register (DOR), which can only select one drive at a time.

No command, except the SENSE INTERRUPT command, should be issued while a RELATIVE SEEK command is in progress.

## Result Phase

None.

### 3.6.16 The SCAN EQUAL, the SCAN LOW OR EQUAL and the SCAN HIGH OR EQUAL Commands

The scan commands compare data read from the disk with data sent from the microprocessor. This comparison produces a match for each scan command, as follows, and as shown in Table 55:

- SCAN EQUAL - Disk data equals microprocessor data.
- SCAN LOW OR EQUAL - Disk data is less than or equal to microprocessor data.
- SCAN HIGH OR EQUAL - Disk data is greater than or equal to microprocessor data.

## Command Phase

**SCAN EQUAL**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | SK | 1 | 0 | 0 | 0 | 1 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Sector Step Size | | | | | | | |

**SCAN LOW OR EQUAL**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | SK | 1 | 1 | 0 | 0 | 1 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Sector Step Size | | | | | | | |

**SCAN HIGH OR EQUAL**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | SK | 1 | 1 | 1 | 0 | 1 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Sector Step Size | | | | | | | |

**First through Eighth Command Phase Bytes - All Scan Commands**

See READ DATA command for a description of the first eight command phase bytes.

**Ninth Command Phase Byte, Sector Step Size**

During execution, the value of this byte is added to the current sector number to determine the next sector to read.

## Execution Phase

The most significant bytes of each sector are compared first. If wildcard mode is enabled in bit 4 of the fourth command phase byte in the MODE command (page 102), an FF (hex) from either the disk or the microprocessor always causes a match.

After each sector is read, if there is no match, the next sector is read. The next sector is the current sector number plus the Sector Step Size specified in the ninth command phase byte.

The scan operation continues until the condition is met, the End of Track (EOT) is reached or the Terminal Count (TC) signal becomes active.

Read error conditions during scan commands are the same as read error conditions during the execution phase of the READ DATA command. See page 106.

If the Skip Control (SK) bit is set to 1, sectors with deleted data marks are ignored.

If all sectors read are skipped, the command terminates with bit 3 of ST2 set to 1, i.e., disk data equals microprocessor data.

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

Table 55 shows how all the scan commands affect bits 3,2 of the Status 2 (ST2) result phase register. See “Result Phase Status Register 2 (ST2)” on page 90.

**TABLE 55. The Effect of Scan Commands on the ST2 Register**

| Command | Result Phase Status Register 2 (ST2) | | Condition |
|---|---|---|---|
| | Bit 3 - Scan Satisfied | Bit 2 - Scan Not Satisfied | |
| SCAN EQUAL | 1<br>0 | 0<br>1 | Disk = µP<br>Disk ≠ µP |
| SCAN LOW OR EQUAL | 1<br>0<br>0 | 0<br>0<br>1 | Disk = µP<br>Disk < µP<br>Disk > µP |
| SCAN HIGH OR EQUAL | 1<br>0<br>0 | 0<br>0<br>1 | Disk = µP<br>Disk > µP<br>Disk < µP |

## 3.6.17 The SEEK Command

The SEEK command issues pulses of the $\overline{\text{STEP}}$ signal to the selected drive, to move it in or out until the desired track number is reached.

Software should ensure that the SEEK command is issued for only one drive at a time. This is because the drives are actually selected via the Digital Output Register (DOR), which can only select one drive at a time. See “Digital Output Register (DOR), Offset 010” on page 77.

No command, except a SENSE INTERRUPT command, should be issued while a SEEK command is in progress.

## Command Phase

When bit 2 of the second command phase byte (ETR) in the MODE command is set to 1, the track number is stored as a 12-bit value. See “Bit 0 - Extended Track Range (ETR)” on page 101.

In this case, a fourth command byte should be written in the command phase to hold the Most Significant Nibble (MSN), i.e., the four most significant bits, of the number of the track to seek. Otherwise (ETR bit in MODE is 0), this command phase byte is not required. and, only three command bytes should be written.

After the last command byte is issued, the Drive Busy bit for the selected drive is set in the Main Status Register (MSR). See bits 3-0 in Section 3.3.6 on page 80.

The controller waits the Delay Before Processing time (see Table 59 on page 117) for the selected drive, before issuing the first $\overline{\text{STEP}}$ pulse. After waiting the Delay Before Processing time, the controller becomes idle. See “Idle Phase” on page 88.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | HD | DS1 | DS0 |
| Number of Track to Seek | | | | | | | |
| MSN of Track # to Seek | | | | 0 | 0 | 0 | 0 |

**Second Command Phase Byte**

See READ DATA command for a description of these bits.

**Third Command Phase Byte, Number of Track to Seek**

The value in this byte is the number of the track to seek.

**Fourth Command Phase Byte,**
**Bits 7-4 - MSN of Track Number**

If the track number is stored as a 12-bit value, these bits contain the Most Significant Nibble (MSN), i.e., the four most significant bits, of the number of the track to seek. Otherwise (the ETR bit in the MODE command is 0), this command phase byte is not required.

## Execution Phase

During the execution phase of the SEEK command, the track number to seek to is compared with the present track number. The controller determines how many $\overline{\text{STEP}}$ pulses to issue and the $\overline{\text{DIR}}$ disk interface output signal indicates which direction the head should move.

The SEEK command issues step pulses while the controller is in the drive polling phase. The step pulse rate is determined by the value programmed in the second command phase byte of the SPECIFY command.

An interrupt is generated one step pulse period after the last step pulse is issued. A SENSE INTERRUPT command should be issued to determine the cause of the interrupt.

## Result Phase

None.

## 3.6.18 The SENSE DRIVE STATUS Command

The SENSE DRIVE STATUS command indicates which drive and which head are selected, whether or not the head is at track 0 and whether or not the track is write protected in result phase Status register 3 (ST3). See "Result Phase Status Register 3 (ST3)" on page 91. This command does not generate an interrupt.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| X | X | X | X | X | HD | DS1 | DS0 |

See READ DATA command for a description of these bits.

## Execution Phase

Disk drive status information is detected and reported.

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 3 (ST3) | | | | | | | |

See "Result Phase Status Register 3 (ST3)" on page 91.

## 3.6.19 The SENSE INTERRUPT Command

The SENSE INTERRUPT command returns the cause of an interrupt that is caused by the change in status of any disk drive.

If a SENSE INTERRUPT command is issued when no interrupt is pending it is treated as an invalid command.

## When to Issue SENSE INTERRUPT

The SENSE INTERRUPT command is issued to detect either of the following causes of an interrupt:

- The FDC became ready during the drive polling phase for an internally selected drive. See "Drive Polling Phase" on page 88. This can occur only after a hardware or software reset.
- A SEEK, RELATIVE SEEK or RECALIBRATE command terminated.

Interrupts caused by these conditions are cleared after the first result byte has been read. Use the Interrupt Code (IC) (bits 7,6) and SEEK End bits (bit 5) of result phase Status register 0 (ST0) to identify the cause of these interrupts. See page 89 and Table 56.

**TABLE 56. Interrupt Causes Reported by SENSE INTERRUPT**

| Bits of ST0 | | | Interrupt Cause |
|---|---|---|---|
| 7 | 6 | 5 | |
| 1 | 1 | 0 | FDC became ready during drive polling mode.<br>SEEK, RELATIVE SEEK or RECALIBRATE not completed. |
| 0 | 0 | 1 | SEEK, RELATIVE SEEK or RECALIBRATE terminated normally. |
| 0 | 1 | 1 | SEEK, RELATIVE SEEK or RELCALIBRATE terminated abnormally. |

## When SENSE INTERRUPT is not Necessary

Interrupts that occur during most command operations do not need to be identified by the SENSE INTERRUPT. The microprocessor can identify them by checking the Request for Master (RQM) bit (bit 7) of the Main Status Register (MSR). See page "Bit 7 - Request for Master (RQM)" on page 81.

It is not necessary to issue a SENSE INTERRUPT command to detect the following causes of Interrupts:

- The result phase of any of the following commands started:
  - READ DATA, READ DELETED DATA, READ A TRACK, READ ID
  - WRITE DATA, WRITE DELETED
  - FORMAT TRACK
  - SCAN EQUAL, SCAN EQUAL OR LOW, SCAN EQUAL OR HIGH
  - VERIFY
- Data is being transferred in non-DMA mode, during the execution phase of some command.

Interrupts caused by these conditions are cleared automatically, or by reading or writing information from or to the Data Register (FIFO).

### Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

### Execution Phase

Status of interrupt is reported.

### Result Phase

When bit 2 of the second command phase byte (ETR) in the MODE command is set to 1, the track number is stored as a 12-bit value. See “Bit 0 - Extended Track Range (ETR)” on page 101.

In this case, a third result byte should be read to hold the Most Significant Nibble (MSN), i.e., the four most significant bits, of the number of the current track.

Otherwise (ETR bit in MODE is 0), this command phase byte is not required. and, only two result phase bytes should be read.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Byte of Present Track Number (PTR) | | | | | | | |
| MSN of PTR | | | | 0 | 0 | 0 | 0 |

**First Result Phase Byte,**
**Result Phase Status Register 0**

See “Result Phase Status Register 0 (ST0)” on page 88.

**Second Result Phase Byte,**
**Present Track Number (PTR)**

The value in this byte is the number of the current track.

**Third Result Phase Byte,**
**Bits 7-4 - MSN of Track Number**

If the track number is stored as a 12-bit value, these bits contain the Most Significant Nibble (MSN), i.e., the four most significant bits, of the number of the track to seek.

Otherwise (the ETR bit in the MODE command is 0), this result phase byte is not required.

## 3.6.20 The SET TRACK Command

This command is used to verify (read) or change (write) the number of the present track.

This command could be useful for recovery from disk tracking errors, where the true track number could be read from the disk using the READ ID command, and used as input to the SET TRACK command to correct the Present Track number (PTR) stored internally.

Termination of this command does not generate an interrupt

### Command Phase

When bit 2 of the second command phase byte (ETR) in the MODE command is set to 1, the track number is stored as a 12-bit value. See “Bit 0 - Extended Track Range (ETR)” on page 101.

In this case, issue SET TRACK twice - once for the Most Significant Byte (MSB) of the number of the current track and once for the Least Significant Byte (LSB).

Otherwise (ETR bit in MODE is 0), issue SET TRACK only once, with bit 2 (MSB) of the second command phase byte set to 0.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | WNR | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | MSB | DS1 | DS0 |
| Byte of Present Track Number (PTR) | | | | | | | |

**First Command Phase Byte,**
**Bit 6 - Write Track Number (WNR)**

0 - Read the existing track number.

The result phase byte already contains the track number, and the third byte in the command phase is a dummy byte.

1 - Change the track number by writing a new value to the result phase byte.

**Second Command Phase Byte**

**Bits 1,0 - Logical Drive Select (DS1,0)**

These bits indicate which logical drive is active. See “Bits 1,0 - Logical Drive Select (DS1,0)” on page 96.

00 - Drive 0 is selected.

01 - Drive 1 is selected.

10 - If four drives are supported, or drives 2 and 0 are exchanged, drive 2 is selected.

11 - If four drives are supported, drive 3 is selected.

**Bit 2 - Most Significant Byte (MSB)**

This bit, together with bits 1,0, determines the byte to read or write. See also Table 57.

0 - Least significant byte of the track number.

1 - Most significant byte of the track number.

**TABLE 57. Defining Bytes to Read or Write Using SET TRACK**

| MSB | DS1 | DS0 | Byte to Read or Write |
|---|---|---|---|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | Drive 0 (LSB) |
| 1 | 0 | 0 | Drive 0 (MSB) |
| 0 | 0 | 1 | Drive 1 (LSB) |
| 1 | 0 | 1 | Drive 1 (MSB) |
| 0 | 1 | 0 | Drive 2 (LSB) |
| 1 | 1 | 0 | Drive 2 (MSB) |
| 0 | 1 | 1 | Drive 3 (LSB) |
| 1 | 1 | 1 | Drive 3 (MSB) |

## Execution Phase

Internal register is read or written.

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Byte of Present Track Number(PTR) | | | | | | | |

This byte is one byte of the track number that was read or written, depending on the value of WNR in the first command byte.

## 3.6.21 The SPECIFY Command

The SPECIFY command sets initial values for the following time periods:

- The delay before command processing starts, formerly called Motor On Time (MNT)
- The delay after command processing terminates, formerly called Motor Off Time (MFT)
- The interval step rate time.

The FDC uses the Digital Output Register (DOR) to enable the drive and motor select signals. See also, “Digital Output Register (DOR), Offset 010” on page 77.

The delays may be used to support the µPD765, i.e., to insert delays from selection of a drive motor until a read or write operation starts, and from termination of a command until the drive motor is no longer selected, respectively.

The parameters used by this command are undefined after power up, and are unaffected by any reset. Therefore, software should always issue a SPECIFY command as part of an initialization routine to initialize these parameters.

Termination of this command does not generate an interrupt.

## Command Phase.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Step Rate Time (SRT) | | | | Delay After Processing | | | |
| Delay Before Processing | | | | | | | DMA |

**Second Command Phase Byte**

**Bits 3-0 - Delay After Processing Factor**

These bits specify a factor that is multiplied by a constant to determine the delay after command processing ends, i.e., from termination of a command until the drive motor is no longer selected.

The value of the Motor Timer Values (TMR) bit (bit 7) of the second command phase byte in the MODE command determines which group of constants and delay ranges to use. See “Bit 7 - Motor Timer Values (TMR)” on page 101.

The specific constant that will be multiplied by this factor to determine the actual delay after processing for each data transfer rate is shown in Table 58.

Use the smallest possible value for this factor, except 0, i.e., 1. If this factor is 0, the value16 is used.

**TABLE 58. Constant Multipliers for Delay After Processing Factor and Delay Ranges**

| Data Transfer Rate (bps) | Bit 7 of MODE (TMR) = 0 | | Bit 7 of MODE (TMR) = 1 | |
|---|---|---|---|---|
| | Constant Multiplier | Permitted Range (msec) | Constant Multiplier | Permitted Range (msec) |
| 1 M | 8 | 8 -128 | 512 | 512 - 8192 |
| 500 K | 16 | 16 - 256 | 512 | 512 - 8192 |
| 300 K | 80 / 3 | 26.7 - 427 | 2560 / 3 | 853 - 13653 |
| 250 K | 32 | 32 - 512 | 1024 | 1024 -16384 |

**TABLE 59. Constant Multipliers for Delay Before Processing Factor and Delay Ranges**

| Data Transfer Rate (bps) | Bit 7 of MODE (TMR) = 0 | | Bit 7 of MODE (TMR) = 1 | |
|---|---|---|---|---|
| | Constant Multiplier | Permitted Range (msec) | Constant Multiplier | Permitted Range (msec) |
| 1 M | 1 | 1 -128 | 32 | 32 - 4096 |
| 500 K | 1 | 1 -128 | 32 | 32 - 4096 |
| 300 K | 10 / 3 | 3.3 - 427 | 160 / 3 | 53 - 6827 |
| 250 K | 4 | 4 - 512 | 64 | 64 - 8192 |

**Bits 7-4 - $\overline{\text{STEP}}$ Time Interval Value (SRT)**

These bits specify a value that is used to calculate the time interval between successive $\overline{\text{STEP}}$ signal pulses during a SEEK, IMPLIED SEEK, RECALIBRATE, or RELATIVE SEEK command.

Table 60 shows how this value is used to calculate the actual time interval.

**TABLE 60. $\overline{\text{STEP}}$ Time Interval Calculation**

| Data Transfer Rate (bps) | Calculation of Time Interval | Permitted Range (msec) |
|---|---|---|
| 1 M | (16 – SRT) / 2 | 0.5 - 8 |
| 500 K | (16 – SRT) | 1 - 16 |
| 300 K | (16 – SRT) x 1.67 | 1.67 - 26.7 |
| 250 K | (16 – SRT) x 2 | 2 - 32 |

**Third Command Phase Byte**

**Bit 0 - DMA**

This bit selects the data transfer mode in the execution phase of a read, write, or scan operation.

Data can be transferred between the microprocessor and the controller during execution in DMA mode or in non-DMA mode, i.e., interrupt transfer mode or software polling mode.

See “Execution Phase” on page 85 for a description of these modes.

0 - DMA mode is selected.

1 - Non-DMA mode is selected.

**Bits 3-0 - Delay Before Processing Factor**

These bits specify a factor that is multiplied by a constant to determine the delay before command processing starts, i.e., from selection of a drive motor until a read or write operation starts.

The value of the Motor Timer Values (TMR) bit (bit 7) of the second command phase byte in the MODE command determines which group of constants and delay ranges to use. See “Bit 7 - Motor Timer Values (TMR)” on page 101.

The specific constant that will be multiplied by this factor to determine the actual delay before processing for each data transfer rate is shown in Table 59.

Use the smallest possible value for this factor, except 0, i.e., 1. If this factor is 0, the value128 is used.

## Execution Phase

Internal registers are written.

## Result Phase

None.

### 3.6.22 The VERIFY Command

The VERIFY command verifies the contents of data and/or address fields after they have been formatted or written.

VERIFY reads logical sectors containing a normal data Address Mark (AM) from the selected drive, without transferring the data to the host.

The TC signal cannot terminate this command since no data is transferred. Instead, VERIFY simulates a TC signal by setting the Enable Count (EC) bit to1. In this case, VERIFY terminates when the number of sectors read equals the number of sectors to read, i.e., Sectors to read Count (SC). If SC = 0 then 256 sectors will be verified.

When EC is 0, VERIFY ends when the End of the Track (EOT) sector number equals the number of the sector checked. In this case, the ninth command phase byte is not needed and should be set to FF (hex).

Table 61 shows how different values for the VERIFY parameters affect termination.

## Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | SK | 1 | 0 | 1 | 1 | 0 |
| EC | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Sectors to read Count (SC) | | | | | | | |

**First Command Phase Byte**

See READ DATA command for a description of these bits starting on page 105.

**Second Command Phase Byte**

**Bits 2-0 - Drive Select (DS1,0) and Head (HD) Select**

See the description of the Drive Select bits (DS1,0) and the Head (HD) select bit in the READ DATA command, starting on page 106.

**Bit 7 - Enable Count Control (EC)**

This bit controls whether the End of Track sector number or the Sectors to read Count (SC) triggers termination of the VERIFY command.

See also, Table 61.

0 - Terminate VERIFY when the number of the last sector read equals the End of Track (EOT) sector number.

The ninth command phase byte, i.e., Sectors to read Count (SC), is not needed and should be set to FF (hex).

1 - Terminate VERIFY when number of sectors read equals the number of sectors to read, i.e., Sectors to read Count (SC).

**Third through Eighth Command Phase Bytes**

See “The READ DATA Command” on page 105.

Always set the End of Track (EOT) sector number to the number of the last sector to be checked on each side of the disk. If EOT is greater than the number of sectors per side, the command terminates with an error and no useful Address Mark (AM) or CRC data is returned.

**Ninth Command Phase Byte, Sectors to Read Count (SC)**

This byte specifies the number of sectors to read. If the Enable Count (EC) control bit (bit 7) of the second command byte is 0, this byte is not needed and should be set to the value FF (hex).

## Execution Phase

Data is read from the disk, as the controller checks for valid address marks in the address and data fields.

This command is identical to the READ DATA command, except that it does not transfer data during the execution phase. See “The READ DATA Command” on page 105.

If the Multi-Track (MT) parameter is 1 and SC is greater than the number of remaining formatted sectors on side 0, verification continues on side 1 of the disk.

## Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

Table 61 shows how different conditions affect the termination status.

**TABLE 61. VERIFY Command Termination Conditions**

| MT | EC | Sector Count (SC) or End of Track (EOT) Value | Termination Status |
|---|---|---|---|
| 0 | 0 | SC should be FF (hex)<br>EOT ≤ Sectors per Side[a] | No Errors |
| | | SC should be FF (hex)<br>EOT > Sectors per Side | Abnormal Termination |
| 0 | 1 | SC ≤ Sectors per Side<br>and<br>SC ≤ EOT | No Errors |
| | | SC > Sectors Remaining[b]<br>or<br>SC > EOT | Abnormal Termination |
| 1 | 0 | SC should be FF (hex)<br>EOT ≤ Sectors per Side | No Errors |
| | | SC should be FF (hex)<br>EOT > Sectors per Side | Abnormal Termination |
| 1 | 1 | SC ≤ Sectors per Side<br>and<br>SC ≤ EOT | No Errors |
| | | SC ≤ (EOT x 2)<br>and<br>EOT ≤ Sectors per Side | No Errors |
| | | SC > (EOT x 2) | Abnormal Termination |

a. The number of formatted sectors per side of the disk.
b. The number of formatted sectors left, which can be read, including side 1 of the disk if MT is 1.

## 3.6.23 The VERSION Command

The VERSION command returns the version number of the current Floppy Disk Controller (FDC).

### Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

### Execution Phase

None.

### Result Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

The result phase byte returns a value of 90 (hex) for an FDC that is compatible with the 82077.

Other controllers, i.e., the DP8473 and other NEC765 compatible controllers, return a value of 80 hex (invalid command).

### 3.6.24 The WRITE DATA Command

The WRITE DATA command receives data from the host and writes logical sectors containing a normal data Address Mark (AM) to the selected drive.

This command is like the READ DATA command, except that the data is transferred from the microprocessor to the controller instead of the other way around.

#### Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | 0 | 0 | 0 | 1 | 0 | 1 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Data Length (Obsolete) | | | | | | | |

See the READ DATA command starting on page 105 for a description of these bytes.

The controller waits the Delay Before Processing time before starting execution.

If implied seeks are enabled, i.e., IPS in the second command phase byte is 1, the operations performed by SEEK and SENSE INTERRUPT commands are performed (without these commands being issued).

#### Execution Phase

Data is transferred from the system to the controller via DMA or non-DMA modes and written to the disk.See “Execution Phase” starting on page 85 for a description of these data transfer modes.

The controller starts the data separator and waits for it to find the address field of the next sector. The controller compares the address ID (track number, head number, sector number, bytes-per-sector code) with the ID specified in the command phase.

If there is no match, the controller waits to find the next sector address field. This process continues until the desired sector is found. If an error condition occurs, the Interrupt Control (IC) bits (bits 7,6) in ST0 are set to abnormal termination, and the controller enters the result phase. See “Bits 7,6 - Interrupt Code (IC)” on page 89

Possible errors are:

- The microprocessor aborted the command by writing to the FIFO.

  If there is no disk in the drive, the controller gets stuck. The microprocessor must then write a byte to the FIFO to advance the controller to the result phase.

- Two pulses of the $\overline{\text{INDEX}}$ signal were detected since the search began, and no valid ID was found.

  If the track address differs, either the Wrong Track bit (bit 4) or the Bad Track bit (bit 1) (if the track address is FF hex) is set in result phase Status register 2 (ST2). See Section 3.5.3 on page 90.

  If the head number, sector number or bytes-per-sector code did not match, the Missing Data bit (bit 2) is set in result phase Status register 1 (ST1).

  If the Address Mark (AM) is not found, the Missing Address Mark bit (bit 0) is set in ST1.

  Section 3.5.2 on page 89 describes the bits of ST1.

- A CRC error was detected in the address field. In this case the CRC Error bit (bit 5) is set in ST1.

- The controller detected an active the Write Protect ($\overline{\text{WP}}$) disk interface input signal, and set bit 1 of ST1 to 1.

If the correct address field is found, the controller waits for all (conventional drive mode) or part (perpendicular drive mode) of gap 2 to pass. See Figure 58 on page 99. The controller then writes the preamble field, Address Marks (AM) and data bytes to the data field. The microprocessor transfers the data bytes to the controller.

After writing the sector, the controller reads the next logical sector, unless one or more of the following termination conditions occurs:

- The DMA controller asserted the Terminal Count (TC) signal to indicate that the operation terminated. The Interrupt Code (IC) bits (bits 7,6) in ST0 are set to normal termination (00). See page 89.

- The last sector address (of side 1, if the Multi-Track enable bit (MT) was set to 1) was equal to the End of Track sector number. The End of Track bit (bit 7) in ST1 is set. The IC bits in ST0 are set to abnormal termination (01). This is the expected condition during non-DMA transfers.

- Overrun error. The Overrun bit (bit 4) in ST1 is set. The Interrupt Code (IC) bits (bits 7,6) in ST0 are set to abnormal termination (01). If the microprocessor cannot service a transfer request in time, the last correctly written byte is written to the disk.

If the Multi-Track (MT) bit was set in the opcode command byte, and the last sector of side 0 has been transferred, the controller continues with side 1.

### Result Phase

Upon terminating the execution phase of the WRITE DATA command, the controller asserts IRQ6, indicating the beginning of the result phase. The microprocessor must then read the result bytes from the FIFO.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

The values that are read back in the result bytes are shown in Table 52 on page 108. If an error occurs, the result bytes indicate the sector read when the error occurred.

### 3.6.25 The WRITE DELETED DATA Command

he WRITE DELETED DATA command receives data from the host and writes logical sectors containing a deleted data Address Mark (AM) to the selected drive.

This command is identical to the WRITE DATA command, except that a deleted data AM, instead of a normal data AM, is written to the data field.

### Command Phase

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MT | MFM | 0 | 0 | 1 | 0 | 0 | 1 |
| IPS | X | X | X | X | HD | DS1 | DS0 |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |
| End of Track (EOT) Sector Number | | | | | | | |
| Bytes Between Sectors - Gap 3 | | | | | | | |
| Data Length (Obsolete) | | | | | | | |

See the READ DATA command starting on page 105 and WRITE DATA on page 120 for a description of these bytes.

### Execution Phase

Data is transferred from the system to the controller in DMA or non-DMA modes, and written to the disk. See “Execution Phase” starting on page 85 for a description of these data transfer modes.

### Result Phase

Upon terminating the execution phase of the WRITE DATA command, the controller asserts IRQ6, indicating the beginning of the result phase. The microprocessor must then read the result bytes from the FIFO.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Result Phase Status Register 0 (ST0) | | | | | | | |
| Result Phase Status Register 1 (ST1) | | | | | | | |
| Result Phase Status Register 2 (ST2) | | | | | | | |
| Track Number | | | | | | | |
| Head Number | | | | | | | |
| Sector Number | | | | | | | |
| Bytes-Per-Sector Code | | | | | | | |

The values that are read back in the result bytes are shown in Table 52 on page 108. If an error occurs, the result bytes indicate the sector read when the error occurred.

## 3.7 EXAMPLE OF A FOUR-DRIVE CIRCUIT USING THE PC87338/PC97338

Figure 59 shows one implementation of a four-drive circuit. Refer to Table 36 on page 77 to see how to encode the drive and motor bits for this configuration.

**FIGURE 59. PC87338/PC97338 Four Floppy Disk Drive Circuit**

# 4.0 Parallel Port

## 4.1 INTRODUCTION

The Parallel Port is a communications device that enables transfer of parallel data bytes between the system and an external device. Originally designed to output data to an external printer, the use of this port has grown to include additional capabilities such as bidirectional communications, increased data rates and additional applications (such as network adaptors). Despite additional parallel port capability, backward compatability is maintained to support existing hardware and software.

### 4.1.1 The Chip Parallel Port Modes

This parallel interface fully supports the IEEE 1284 standard and EPP 1.7 modes of parallel communications, in both Legacy or Plug and Play configurations. It supports two Standard Parallel Port (SPP) modes of operation for parallel printer ports (as found in the IBM PC-AT, PS/2 and Centronics systems), two Enhanced Parallel Port (EPP) modes of operation, and one Extended Capabilities Port (ECP) mode.

The parallel port output pins are protected against potential damage from connecting an unpowered port to a powered-up printer.

The functional modes supported by the Chip parallel port are as follows:

- The Standard Parallel Port (SPP) configuration supports two operation modes:
  - In Compatible SPP mode the port is write-only (for data). Data transfers are software-controlled, accompanied by status and control handshake lines.
  - In Extended SPP mode, the parallel port becomes a read/write port, transferring a full data byte in both directions.

  In these modes, low data rates are achieved (several hundred bytes per second).
- The Enhanced Parallel Port (EPP) configuration supports two modes that offer higher bi-directional throughput and more efficient hardware-based handling.
  - The EPP revision 1.7 mode has the above advantages but lacks a comprehensive handshaking scheme to ensure data transfer integrity between communicating devices with dissimilar data rates.

    The IEEE 1284 standard establishes a widely accepted handshake and transfer protocol that ensures transfer data integrity. This standard is met by all modes in this module except the EPP revision 1.7 mode.
  - EPP revision 1.9 mode offers data transfer enhancement, while meeting the IEEE 1284 standard.
- The Extended Capabilities Port (ECP) mode extends the port capabilities beyond EPP modes by adding a bi-directional 16-level FIFO with threshold interrupts, for PIO and DMA operation. In this mode, the device becomes a hardware state-machine with highly efficient hardware real-time data transfer control.

### 4.1.2 Device Configuration

The functional mode of the parallel port is determined by setting the appropriate bits in the system configuration registers:

All parallel port functions are enabled by setting bit 0 of the system Function Enable Register (FER) to 1.

SPP is the default mode. In this mode, bit 7 of the PTR register selects Compatible SPP mode when it is 0 and Extended SPP mode when it is 1.

If bit 0 of the Parallel Port Control Register (PCR) is set to 1, the device enters EPP mode. Bit 1 of this registers dictates whether mode 1.7 or 1.9 is active, unless the Zero Wait State Enable bit 5 of the Function Control configuration register (FCR) is set to 1. In this case, the device is in revision 1.7 mode, regardless of the value of bit 1 of the PCR register.

When bit 2 of the PCR is set to 1, ECP mode is enabled.

The parallel port supports plug and play operation; its interrupt can be routed on one of the following ISA interrupts: IRQ7-IRQ3, IRQ12-IRQ9 or IRQ15 (see PNP0 register); its DMA signals can be routed to one of three 8-bit ISA DMA channels (see PNP2 register); and its base address is software configurable (see PBAL and PBAH registers)

## 4.2 STANDARD PARALLEL PORT MODES

The two Standard Parallel Port (SPP) modes Compatible SPP and Extended SPP modes.

Compatible SPP mode is a data write-only mode that outputs data to a parallel printer, using handshake bits, under software control.

In Extended SPP mode, parallel data transfer is bi-directional.

The list of output signals for the standard 25-pin, D-type connector appears in Table 72 on page 145.

The reset states for handshake output pins in this mode are listed below in Table 62.

A single Data Register DTR is used for data input and output (see Section 4.2.3). The direction of data flow is determined by the system setting in bit 5 of the Control Register CTR.

**TABLE 62. Parallel Port Reset States**

| Signal | Reset Control | State After Reset |
|---|---|---|
| SLIN | MR | TRI-STATE |
| INIT | MR | Zero |
| AFD | MR | TRI-STATE |
| STB | MR | TRI-STATE |
| IRQ5,7 | MR | TRI-STATE |

### 4.2.1 Standard Parallel Port (SPP) Modes Register Set

All SPP mode port operation is controlled by three registers. Table 63 shows the registers of the parallel port in the Standard Parallel Port (SPP) modes.

The register bits assignments are compatible with the assignments in existing SPP devices.

**TABLE 63. Standard Parallel Port Registers**

| Offset | A1 | A0 | Symbol | Description | R/W |
|---|---|---|---|---|---|
| 0 | 0 | 0 | DTR | Data | R/W |
| 1 | 0 | 1 | STR | Status | R |
| 2 | 1 | 0 | CTR | Control | R/W |
| 3 | 1 | 1 | | - | TRI-STATE |

### 4.2.2 SPP Mode Parallel Port Register Bitmaps

### 4.2.3 Data Register (DTR), Offset 0

This bidirectional data port transfers 8-bit data in the direction determined by bit 7 of configuration Register PTR and bit 5 of SPP register CTR.

Bit 7 of the PTR selects the port mode - compatible mode, with no data input capability, or extended mode, having data input capability.

Bit 5 of the CTR determines the direction of the data flow - whether from the Data register DTR to the system, or from DTR to the external pins PD7-0.

The actual read or write to the data register is activated by the system $\overline{RD}$ and $\overline{WR}$ strobes.

Table 64 tabulates DTR register operation.

**TABLE 64. SPP Data Register Read and Write Modes**

| Bit 7 of PTR | Bit 5 of CTR | $\overline{RD}$ | $\overline{WR}$ | Result |
|---|---|---|---|---|
| 0 | x | 1 | 0 | Data written to PD7-0. |
| 0 | x | 0 | 1 | Data read from the output latch |
| 1 | 0 | 1 | 0 | Data written to PD7-0. |
| 1 | 1 | 1 | 0 | Data written is latched |
| 1 | 0 | 0 | 1 | Data read from output latch. |
| 1 | 1 | 0 | 1 | Data read from PD7-0. |

When bit 7 of the PTR is zero, the device is in SPP compatible mode, and does not write data to the output pins. Bit 5 of the CTR register has no effect in this state. If data is written ($\overline{WR}$ goes low), the data will be sent to the output pins PD7-0. If a Read cycle is initiated ($\overline{RD}$ goes low), the system will read the contents of the output latch, and not data from the output pins PD7-0.

When bit 7 of the PTR is 1, the device is in the Extended SPP mode and can read and write external data via PD7-0. In this mode, bit 5 sets the direction for data in or data out, while read or write cycles are possible in both settings of bit 5.
If CTR bit 5 is cleared to 0, data is written to the output pins PD7-0 when a write cycle occurs. (if a read cycle occurs in this setting, the system will read the output latch, not data from PD7-0).
If CTR bit 5 is set to 1, data is read from the output pins PD7-0 when a read cycle occurs. A write cycle in this setting will only write to the output latch, not to the output pins PD7-0.

The reset value of this register is 0.

**FIGURE 60. DTR Register Bitmap (SPP Mode)**

### 4.2.4 Status Register (STR), Offset 1

This read-only register holds status information. A system write operation to STR is an invalid operation that has no effect on the parallel port.

**FIGURE 61. STR Register Bitmap (SPP Mode)**

**Bit 0 - Time-Out Status**

In EPP mode only, this is the time-out status bit. In all other modes this bit has no function and has the constant value 1.

This bit is cleared when EPP mode is enabled, i.e., when bit 0 of PCR is changed from 0 to 1. Thereafter, this bit is set to 1 when a time-out occurs in an EPP cycle and is cleared when STR is read.

In EPP mode:

0 - EPP mode set. No time-out occurred since STR was last read.

1 - Time-out occurred on EPP cycle (minimum of 10 µsec). (Default)

**Bit 1 - Reserved**

This bit is reserved and is always 1.

**Bit 2 - IRQ Status**

In all modes except Extended SPP, this bit is always 1.

In Extended SPP mode (bit 7 of PTR is 1) this bit is the IRQ status bit. It remains high unless the interrupt request is enabled (bit 4 of CTR set high). This bit is high except when latched low when the $\overline{ACK}$ signal makes a low to high transition, indicating a character is now being transferred to the printer.

Reading this bit resets it to 1.

0 - Interrupt requested in Extended SPP mode.

1 - No interrupt requested. (Default)

**Bit 3 - $\overline{ERR}$ Status**

This bit reflects the current state of the printer error signal, $\overline{ERR}$. The printer sets this bit low when there is a printer error.

0 - Printer error.

1 - No printer error.

**Bit 4 - SLCT Status**

This bit reflects the current state of the printer select signal, SLCT. The printer sets this bit high when it is online and selected.

0 - No printer selected.

1 - Printer selected and online.

**Bit 5 - PE Status**

This bit reflects the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper.

0 - Printer has paper.

1 - End of paper in printer.

**Bit 6 - $\overline{ACK}$ Status**

This bit reflects the current state of the printer acknowledge signal, $\overline{ACK}$. The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the $\overline{ACK}$ pin.

0 - Character reception complete.

1 - No character received .

**Bit 7 - Printer Status**

This bit reflects the current state of the printer BUSY signal. The printer sets this bit low when it is busy and cannot accept another character.

This bit is the inverse of the (BUSY/$\overline{WAIT}$) pin.

0 - Printer busy.

1 - Printer not busy.

### 4.2.5 Control Register (CTR), Offset 2

The control register provides all the output signals that control the printer. Except for bit 5, it is a read and write register.

Normally when the Control Register is read, the bit values are provided by the internal output data latch. These bit values can be superseded by the logic level of the $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, and $\overline{SLIN}$ pins, if these pins are forced high or low by an external voltage. To force these signals high or low the corresponding bits should be set to their inactive state (e.g., AFD, STB and SLIN should all be 0, $\overline{INIT}$ should be 1).

Section 4.3.11 describes the transfer operations that are possible in EPP mode.

**FIGURE 62. CTR Register Bitmap (SPP Mode) in PC87338**

**FIGURE 63. CTR Register Bitmap (SPP Mode)**

**Bit 0 - Data Strobe Control**

Bit 0 directly controls the data strobe signal to the printer via the $\overline{STB}$ pin.

This bit is the inverse of the $\overline{STB}$ pin.

**Bit 1 - Automatic Line Feed Control**

This bit directly controls the automatic line feed signal to the printer via the $\overline{AFD}$ pin. Setting this bit high causes the printer to automatically feed after each line is printed.

This bit is the inverse of the $\overline{AFD}$ pin.

0 - No automatic line feed. (Default)

1 - Automatic line feed

**Bit 2 - Printer Initialization Control ($\overline{INIT}$)**

This bit directly controls the signal to initialize the printer via the $\overline{INIT}$ pin. Setting this bit to low initializes the printer.

The value of the $\overline{INIT}$ signal reflects the value of this bit.

In the PC87338 this bit is 0 after reset (activate $\overline{INIT}$ signal to initialized the printer).

*In the PC97338 this bit is 1 after reset, so the printer can stay in ECP mode if it was programmed to this mode, and not initialized to SPP mode.*

0 - Initialize Printer (Default in PC87338).

1 - No action (Default in PC97338).

**Bit 3 - Select Input Signal Control**

This bit directly controls the select in signal to the printer via the $\overline{SLIN}$ pin. Setting this bit high selects the printer.

It is the inverse of the $\overline{SLIN}$ pin.

This bit must be set to 1 before enabling the EPP or ECP modes via bits 0 or 2 of the PCR register.

0 - Printer not selected. (Default)

1 - Printer selected and online.

**Bit 4 - Interrupt Enable**

Bit 4 controls the interrupt generated by the $\overline{ACK}$ signal. Its function changes slightly depending on the parallel port mode selected.

In ECP mode, this bit should be set to 0.

In the following description, IRQx indicates an interrupt line allocated for the parallel port.

0 - In Compatible SPP, Extended SPP and EPP modes, IRQx is floated. (Default)

1 - In Compatible SPP mode, IRQx follows $\overline{ACK}$ transitions.

In Extended SPP mode, IRQx is set active on the trailing edge of $\overline{ACK}$.

In EPP mode, IRQx follows $\overline{ACK}$ transitions, or is set when an EPP time-out occurs.

**Bit 5 - Direction Control**

This bit determines the direction of the parallel port in Extended SPP mode (when bit 7 of PTR is 1). In the (default) Compatible SPP mode, this pin has no effect, since the port functions for output only.

This is a read/write bit in EPP modes. In SPP modes it is a write only bit. A read from it returns 1. In Compatible SPP mode and in EPP modes it does not control the direction. See Table 64.

0 - Data output to PD7-0 in Extended SPP mode during write cycles (Default)

1- Data input from PD7-0 in Extended SPP mode during read cycles.

**Bits 7,6 - Reserved**

These bits are reserved and are always 1.

## 4.3 ENHANCED PARALLEL PORT (EPP) MODES

EPP modes allow greater throughput than Compatible SPP and Extended SPP modes by supporting faster transfer times (8, 16 or 32 bit data transfers in a single read/write operation) and a mechanism that allows the system to address peripheral device registers directly. Faster transfers are achieved by automatically generating the address and data strobes.

The connector pin assignments for these modes are listed in “Parallel Port Pin Out” on page 145.

EPP modes support revision 1.7 and revision 1.9 of the IEEE 1284 standard, as shown in Table 65. When bit 5 of FCR is 1 (configured for zero wait states), the EPP revision is always 1.7, i.e., it is not affected by bit 1 of PCR.

**TABLE 65. EPP Revision Selection**

| EPP Mode | Bit 5 of the FCR Configuration register | Bit 1 of PCR | Bit 0 of PCR |
|---|---|---|---|
| EPP Revision 1.7 | 1 | x | 1 |
| | 0 | 0 | 1 |
| EPP Revision 1.9 (IEEE 1284) | 0 | 1 | 1 |

In Legacy mode, EPP modes are supported for a parallel port whose base address is 278h or 378h, but not for a parallel port whose base address is 3BCh. (There are no EPP registers at 3BFh.)

SPP-type data transactions may be conducted in either EPP mode. The appropriate registers are available for this type of transaction. (See Table 66.) As in the SPP modes, software must generate the control signals required to send or receive data.

The output of the control signals in PC87338 are in level 2 (pushpull) when in EPP1.9 mode

*The output of the control signals in PC97338 are in level 2 (pushpull) always when in EPP mode.*

### 4.3.1 Enhanced Parallel Port (EPP) Modes Register Set

Table 66 lists the EPP mode registers. All are single-byte registers.

Bits 0, 1 and 3 of the CTR register must be 0 before the EPP registers can be accessed, since the pins controlled by these bits are controlled by hardware during EPP accesses. Once these bits are set to 0 by the software driver, multiple EPP access cycles may be invoked. Bit 7 of the PTR register must be set to 0, when EPP mode is enabled.

Bit 7 of STR ($\overline{BUSY}$ status) must be set to 1 before writing to DTR in EPP mode to ensure data output to PD7-0.

The EPP monitors the IOCHRDY pin during EPP cycles. If IOCHRDY is driven low for more then 10 µsec, an EPP time-out event occurs, which aborts the cycle by asserting IOCHRDY, thus releasing the system from a stuck EPP peripheral device. When the cycle is aborted, $\overline{ASTRB}$ or $\overline{DSTRB}$ becomes inactive, and the time-out event is signaled by asserting bit 0 of the STR. If bit 4 of the CTR is 1, the time-out event also pulses the IRQ5 or IRQ7 lines.

EPP cycles to the external device are activated by invoking read or write cycles to the EPP.

**TABLE 66. Parallel Port Registers in EPP Modes**

| Offset | Symbol | Description | Mode | R/W |
|---|---|---|---|---|
| 0 | DTR | SPP Data | SPP or EPP | R/W |
| 1 | STR | SPP Status | SPP or EPP | R |
| 2 | CTR | SPP Control | SPP or EPP | R/W |
| 3 | EPP Address | | EPP | R/W |
| 4 | EPP Data Port 0 | | EPP | R/W |
| 5 | EPP Data Port 1 | | EPP | R/W |
| 6 | EPP Data Port 2 | | EPP | R/W |
| 7 | EPP Data Port 3 | | EPP | R/W |

### 4.3.2 EPP Modes Parallel Port Register Bitmaps

### 4.3.3 SPP or EPP Data Register (DTR), Offset 0

The DTR register is the SPP Compatible or SPP Extended data register. A write to DTR sets the state of the eight data pins on the 25-pin D-shell connector.

**FIGURE 64. DTR Register Bitmap (EPP Mode)**

### 4.3.4 SPP or EPP Status Register (STR), Offset 1

This status port is read only. A read presents the current status of the five pins on the 25-pin D-shell connector, and the IRQ as shown in Figure 65.

**FIGURE 65. STR Register Bitmap (EPP Mode)**

The bits of this register have the identical function in EPP mode as in SPP mode. See Section 4.2.4 for a detailed description of each bit.

### 4.3.5 SPP or EPP Control Register (CTR), Offset 2

This control port is read or write. A write operation to it sets the state of four pins on the 25-pin D-shell connector, and controls both the parallel port interrupt enable and direction.

**FIGURE 66. CTR Register Bitmap (EPP Mode)**

The bits of this register have the identical function in EPP modes as in SPP modes. See Section 4.2.5 for a detailed description of each bit.

### 4.3.6 EPP Address Register, Offset 3

This port is added in EPP mode to enhance system throughput by enabling registers in the remote device to be directly addressed by hardware.
This port can be read or written. Writing to it initiates an EPP device or register selection operation.

**FIGURE 67. DTR Register Bitmap (EPP Mode)**

### 4.3.7 EPP Data Port 0, Offset 4

This is a read/write port. Accessing it initiates device read or write operations of bits 7-0.

**FIGURE 68. DTR Register Bitmap (EPP Mode)**

### 4.3.8 EPP Data Port 1, Offset 5

This is the second EPP data port. It is only accessed to transfer bits 15 through 8 of a 16-bit read or write to data port 0.

**FIGURE 69. DTR Register Bitmap (EPP Mode)**

### 4.3.9 EPP Data Port 2, Offset 6

This is the third EPP data port. It is only accessed to transfer bits 16 to 23 of a 32-bit read or write to data port 0.

**FIGURE 70. EPP Data Port 2 Bitmap**

### 4.3.10 EPP Data Port 3, Offset 7

This is the fourth EPP data port. It is only accessed to transfer bits 24 to 31 of a 32-bit read or write to data port 0.

**FIGURE 71. EPP Data Port 3 Bitmap**

### 4.3.11 EPP Mode Transfer Operations

The EPP transfer operations are: address read or write, and data read or write. An EPP transfer operation is composed of a system read or write cycle (from or to an EPP register) and an EPP read or write cycle (from a peripheral device to an EPP register, or from an EPP register to a peripheral device).

### EPP 1.7 Address Write

The following procedure selects a peripheral device or register as illustrated in Figure 72.

1. The system writes a byte to the EPP address register.
   $\overline{WR}$ becomes low to latch D7-0 into the address register. The latch drives the address register onto PD7-0 and the EPP pulls $\overline{WRITE}$ low.
2. The EPP pulls $\overline{ASTRB}$ low to indicate that data was sent.
3. If $\overline{WAIT}$ was low during the system write cycle, IOCHRDY becomes low. When $\overline{WAIT}$ becomes high, the EPP pulls IOCHRDY high.
4. When IOCHRDY becomes high, it causes $\overline{WR}$ to become high. If $\overline{WAIT}$ is high during the system write cycle, then the EPP does not pull IOCHRDY to low.
5. When $\overline{WR}$ becomes high, it causes the EPP to pull $\overline{ASTRB}$ to high, and then to pull $\overline{WRITE}$ to high. The EPP can change PD7-0 only when $\overline{WRITE}$ and $\overline{ASTRB}$ are both high.

**FIGURE 72. EPP 1.7 Address Write**

### EPP 1.7 Address Read

The following procedure reads from the address register as shown in Figure 73.

1. The system reads a byte from the EPP address register. $\overline{RD}$ goes low to gate PD7-0 into D7-0.
2. The EPP pulls $\overline{ASTRB}$ low to signal the peripheral to start sending data.
3. If $\overline{WAIT}$ is low during the system read cycle. Then the EPP pulls IOCHRDY low. When $\overline{WAIT}$ becomes high, the EPP stops pulling IOCHRDY to low.
4. When IOCHRDY becomes high, it causes $\overline{RD}$ to become high. If $\overline{WAIT}$ is high during the system read cycle then the EPP does not pull IOCHRDY to low.
5. When $\overline{RD}$ becomes high, it causes the EPP to pull $\overline{ASTRB}$ high. The EPP can change PD7-0 only when $\overline{ASTRB}$ is high. After $\overline{ASTRB}$ becomes high, the EPP puts D7-0 in TRI-STATE.

**FIGURE 73. EPP 1.7 Address Read**

## EPP 1.7 Data Write and Read

This procedure writes to the selected peripheral device or register.

An EPP 1.7 data read or write operations are similar to the EPP 1.7 address read or write operations, except that the data strobe (DSTRB signal), and a data register, replace the address strobe (ASTRB signal) and the address register respectively.

## EPP Revision 1.7 Zero Wait State (ZWS) Address and Data Write and Read Operations

To configure the device for zero wait states, set bit 5 of FCR to 1 and clear bit 6 of FCR to 0. When bit 5 of FCR is 1, the EPP revision is always 1.7, i.e., it is not affected by bit 1 of PCR.

The following procedure performs a short write to the selected peripheral device or register. See also Figure 74.

1. The system writes a byte to the EPP address register. WR goes low to latch D7-0 into the data register. The latch drives the data register to PD7-0.
2. The EPP first pulls WRITE low, and then pulls ASTRB low to indicate that data has been sent.
3. If WAIT was high during the system write cycle, ZWS goes low and IOCHRDY stays high.
4. When the system pulls WR high, the EPP pulls ASTRB, ZWS and then WRITE to high. The EPP can change PD7-0 only when WRITE and ASTRB are high.
5. If the peripheral is fast enough to pull WAIT low before the system terminates the write cycle, the EPP pulls IOCHRDY to low, but does not pull ZWS to low, thus carrying out a normal (non-ZWS EPP 1.7) write operation.

**FIGURE 74. EPP Write with Zero Wait States**

A read operation is similar, except for the data direction, activation of RD instead of WR, and WRITE stays high.

EPP 1.7 zero wait state data write and read operations are similar to EPP zero wait state address write and read operations, with the exception that the data strobe (DSTRB signal), and a data register, replace the address strobe (ASTRB signal) and the address register, respectively.

## EPP 1.9 Address Write

The following procedure selects a peripheral or register as shown in Figure 75.

1. The system writes a byte to the EPP address register.
2. The EPP pulls IOCHRDY low, and waits for WAIT to become low.
3. When WAIT becomes low, the EPP pulls WRITE to low and drives the latched byte onto PD7-0. If WAIT was already low, steps 2 and 3 occur concurrently.
4. The EPP pulls ASTRB low and waits for WAIT to become high.
5. When WAIT becomes high, the EPP stops pulling IOCHRDY low, and waits for WR to become high.
6. When WR becomes high, the EPP pulls ASTRB high, and waits for WAIT to become low.
7. If no EPP write is pending when WAIT becomes low, the EPP pulls WRITE to high. Otherwise, WRITE remains low, and the EPP may change PD7-0.

**FIGURE 75. EPP 1.9 Address Write**

## EPP 1.9 Address Read

The following procedure reads from the address register.

1. The system reads a byte from the EPP address register. When RD becomes low, the EPP pulls IOCHRDY low, and waits for WAIT to become low.
2. When WAIT becomes low, the EPP pulls ASTRB low and waits for WAIT to become high. If WAIT was already low, steps 2 and 3 occur concurrently.
3. When WAIT becomes high, the EPP stops pulling IOCHRDY low, and waits for RD to become high.
4. When RD becomes high, the EPP latches PD7-0 (to provide sufficient hold time), pulls ASTRB high, and puts D7-0 in TRI-STATE.

**FIGURE 76. EPP 1.9 Address Read**

## EPP 1.9 Data Write and Read

This procedure writes to the selected peripheral drive or register.

EPP 1.9 data read and write operations are similar to EPP 1.9 address read and write operations, respectively, except that the data strobe (DSTRB signal) and a data register replace the address strobe (ASTRB signal) and the address register, respectively.

## 4.4 EXTENDED CAPABILITIES PARALLEL PORT (ECP) MODES

In the Extended Capabilities Port (ECP) modes, the device is a state machine that supports a 16-byte FIFO that can be configured for either direction, command and data FIFO tags (one per byte), a FIFO threshold interrupt for both directions, FIFO empty and full status bits, automatic generation of strobes (by hardware) to fill or empty the FIFO, transfer of commands and data, and Run Length Encoding (RLE) expanding (decompression) as explained below. The FIFO can be accessed by PIO or system DMA cycles.

The ECP modes are enabled when bit 2 of PCR is 1. Once enabled, the mode is controlled via the mode field of ECR, i.e., bits 7-5 of the ECR register as shown in Table 71 on page 141 and described in detail in “ECP Mode Descriptions” on page 142.

The ECP modes and their code designations are listed in Table 67.

**TABLE 67. ECP Modes Encoding**

| ECR Bit Encoding | | | Mode Name |
|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | |
| 0 | 0 | 0 | Standard |
| 0 | 0 | 1 | PS/2 |
| 0 | 1 | 0 | Parallel port FIFO |
| 0 | 1 | 1 | ECP FIFO |
| 1 | 1 | 0 | FIFO test |
| 1 | 1 | 1 | Configuration |

The output of the control signals in PC87338 are in level 2 (pushpull) when:

- in ECP mode 011
- in ECP mode 010 and PCR[1]=1

*The output of the control signals in PC97338 are in level 2 (pushpull) in all ECP modes besides 000.*

**TABLE 68. Parallel Port Registers in ECP Modes**

| Offset | Symbol | Description | Modes (ECR Bits) 7 6 5 | R/W |
|---|---|---|---|---|
| 000h | DATAR | Parallel Port Data Register | 0 0 0<br>0 0 1 | R/W |
| 000h | AFIFO | ECP Address FIFO | 0 1 1 | W |
| 001h | DSR | Status Register | All Modes | R |
| 002h | DCR | Control Register | All Modes | R/W |
| 400h | CFIFO | Parallel Port Data FIFO | 0 1 0 | W |
| 400h | DFIFO | ECP Data FIFO | 0 1 1 | R/W |
| 400h | TFIFO | Test FIFO | 1 1 0 | R/W |
| 400h | CNFGA | Configuration Register A | 1 1 1 | R |
| 401h | CNFGB | Configuration Register B | 1 1 1 | R |
| 402h | ECR | Extended Control Register | All Modes | R/W |

### 4.4.1 Accessing the ECP Registers

The AFIFO, CFIFO, DFIFO and TFIFO registers access the same ECP FIFO. The FIFO is accessed at Base + 000h, or Base + 400h, depending on the mode field of ECR and the register.

The FIFO can be accessed by system DMA cycles, as well as system PIO cycles.

When the DMA is configured and enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically (by hardware) issues DMA requests to fill the FIFO (in the forward direction when bit 5 of DCR is 0) or to empty the FIFO (in the reverse direction when bit 5 of DCR is 1). All DMA transfers are to or from these registers. The ECP does not assert DMA requests for more than 32 consecutive DMA cycles. The ECP stops requesting the DMA when TC is detected during an ECP DMA cycle.

Writing into a full FIFO, and reading from an empty FIFO, are ignored. The written data is lost, and the read data is undefined. The FIFO empty and full status bits are not affected by such accesses.

Some registers are not accessible in all modes of operation, or may be accessed in one direction only. Accessing a non accessible register has no effect. Data read is undefined; data written is ignored; and the FIFO does not update. The Chip SPP registers (DTR, STR and CTR) are not accessible when the ECP is enabled.

To improve noise immunity in ECP cycles, the state machine does not examine the control handshake response lines until the data has had time to switch.

In ECP modes:

- DATAR replaces DTR of SPP/EPP
- DSR replaces STR of SPP/EPP
- DCR replaces CTR of SPP/EPP

The base address is 278h, 378h or 3BCh, as specified in the FAR register in Legacy mode.

### 4.4.2 Software Operation in ECP Modes

Software should operate as described in "*Extended Capabilities Port Protocol and ISA Interface Standard*".

Some of these operations are:

- Software should enable ECP (bit 2 of PCR is 1) after bits 3-0 of the parallel port Control Register (CTR) are set to 0100.
- When ECP is enabled, software should switch modes only through modes 000 or 001.
- When ECP is enabled, the software should change direction only in mode 001.
- Software should not switch from mode 010 or 011, to mode 000 or 001, unless the FIFO is empty.
- Software should switch to mode 011 when bits 0 and 1 of DCR are 0.
- Software should switch to mode 010 when bit 0 of DCR is 0.
- Software should disable ECP (bit 2 of PCR is 0) only in mode 000 or 001.

Software may switch from mode 011 backward to modes 000 or 001, when there is an on-going ECP read cycle. In this case, the read cycle is aborted by deasserting $\overline{AFD}$. The FIFO is reset (empty) and a potential byte expansion (RLE) is automatically terminated since the new mode is 000 or 001.

### 4.4.3 Hardware Operation in ECP Modes

The $\overline{ZWS}$ signal is asserted by the ECP when ECP modes are enabled, and an ECP register is accessed by system PIO instructions, thus using a system zero wait states cycle (except during read cycles from ECR).

The ECP uses an internal clock, which can be frozen to reduce power consumption during power down. In this power-down state the DMA is disabled, all interrupts (except $\overline{ACK}$) are masked, and the FIFO registers are not accessible (access is ignored). The other ECP registers are unaffected by power-down and are always accessible when the ECP is enabled. During power-down the FIFO status and contents become inaccessible, and the system reads bit 2 of ECR as 0, bit 1 of ECR as 1 and bit 0 of ECR as 1, regardless of the actual values of these bits. The FIFO status and contents are not lost, however, and when the clock activity resumes, the values of these bits resume their designated functions.

When the clock is frozen, an on-going ECP cycle may be corrupted, but the next ECP cycle will not start even if the FIFO is not empty in the forward direction, or not full in the backward direction. If the ECP clock starts or stops toggling during a system cycle that accesses the FIFO, the cycle may yield wrong data.

ECP output signals are inactive when the ECP is disabled.

Only the FIFO, DMA and RLE do not function when the clock is frozen. All other registers are accessible and functional. The FIFO, DMA and RLE are affected by ECR modifications, i.e., they are reset when exits from modes 010 or 011 are carried out even while the clock is frozen.

### 4.4.4 ECP Modes Parallel Port Register Bitmaps

**Bits 7-5 of ECR = 000 or 001**

**ECP Data Register (DATAR) Offset 000h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

D0, D1, D2, D3, D4, D5, D6, D7

**Bits 7-5 of ECR = 011**

**ECP Address Register (AFIFO) Offset 000h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

A0, A1, A2, A3, A4, A5, A6, A7

**All ECP Modes**

**ECP Status Register (DSR) Offset 001h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | 1 | 1 | 1 | Reset |
| | | | | | 1 | 1 | 1 | Required |

Reserved
Reserved
Reserved
$\overline{ERR}$ Status
SLCT Status
PE Status
$\overline{ACK}$ Status
Printer Status

**All ECP Modes**

**ECP Control Register (DCR) Offset 002h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

Data Strobe Control
Automatic Line Feed Control
Printer Initialization Control($\overline{INIT}$)
Parallel Port Input Control
Interrupt Enable
Direction Control
Reserved
Reserved

### 4.4.5 ECP Data Register (DATAR), Bits 7-5 of ECR = 000 or 001, Offset 000h

The ECP Data Register (DATAR) register is the same as the DTR register (see Section 4.2.3), except that a read always returns the values of the PD7-0 signals instead of the register latched data.

**FIGURE 77. DATAR Register Bitmap**

### 4.4.6 ECP Address FIFO (AFIFO) Register, Bits 7-5 of ECR = 011, Offset 000h

The ECP Address FIFO Register (AFIFO) is write only. In the forward direction (bit 5 of DCR is 0) a byte written into this register is pushed into the FIFO and tagged as a command.

Reading this register returns undefined contents. Writing to this register in a backward direction (bit 5 of DCR is 1) has no effect and the data is ignored.

**FIGURE 78. AFIFO Register Bitmap**

### 4.4.7 ECP Status Register (DSR), Offset 001h

This read-only register displays device status. Writes to this DSR have no effect and the data is ignored.

This register should not be confused with the DSR register of the Floppy Disk Controller (FDC).

**FIGURE 79. ECP DSR Register Bitmap**

**Bits 0 - 2 - Reserved**

These bits are reserved and are always 1.

**Bit 3 - $\overline{\text{ERR}}$ Status**

This bit reflects the status of the $\overline{\text{ERR}}$ signal.

0 - Printer error

1 - No printer error

**Bit 4 - SLCT Status**

This bit reflects the status of the Select signal. The printer sets this signal high when it is online and selected

0 - Printer not selected (default)

1 - Printer selected and online

**Bit 5 - PE Status**

This bit reflects the status of the Paper End (PE) signal.

0 - Paper not ended

1 - NO paper in printer.

**Bit 6 - $\overline{\text{ACK}}$ Status**

This bit reflects the status of the $\overline{\text{ACK}}$ signal. This signal is pulsed low after a character is received.

0 - Character received.

1 - No character received (Default)

**Bit 7 -Printer Status**

This bit reflects the inverse of the state of the BUSY signal.

0 - Printer is busy (cannot accept another character now)

1 - Printer not busy - ready for another character.

### 4.4.8 ECP Control Register (DCR), Offset 002h

Reading this register returns the register content (not the pin values, as in SPP mode).

**FIGURE 80. DCR Register Bitmap**

**Bit 0 - Data Strobe Control**

Bit 0 directly controls the data strobe signal to the printer via the $\overline{STB}$ signal. This bit is the inverse of the $\overline{STB}$ signal.

0 - The $\overline{STB}$ signal is inactive in all modes except 010 and 011. In these modes, it may be active or inactive as set by the software.

1 - In all modes, $\overline{STB}$ is active.

**Bit 1 - Automatic Line Feed Control**

This bit directly controls the automatic feed XT signal to the printer via the $\overline{AFD}$ signal. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the $\overline{AFD}$ signal.

In mode 011, $\overline{AFD}$ is activated by both ECP hardware and by software using this bit.

0 - No automatic line feed. (Default)

1 - Automatic line feed.

**Bit 2 - Printer Initialization Control**

Bit 2 directly controls the signal to initialize the printer via the $\overline{INIT}$ signal. Setting this bit to low initializes the printer. The $\overline{INIT}$ signal follows this bit.

0 - Initialize printer (Default)

1 - No action.

**Bit 3 - Parallel Port Input Control**

This bit directly controls the select input device signal to the printer via the $\overline{SLIN}$ signal. It is the inverse of the $\overline{SLIN}$ signal.

This bit must be set to 1 before enabling the EPP or ECP modes via bits 0 or 2 of the PCR register.

0 - The printer is not selected.

1 - The printer is selected.

**Bit 4 - Interrupt Enable**

Bit 4 enables the interrupt generated by the $\overline{ACK}$ signal. In ECP mode, this bit should be set to 0. This bit does not float the IRQ pin.

0 - Masked. (Default)

1 - Enabled.

**Bit 5 - Direction Control**

This bit determines the direction of the parallel port when bit 7 of PTR is 1. The default condition is parallel port in output mode.

In the PC87338, this bit is a read only bit (return 0) in ECP modes 000 and 010. In all other ECP modes, it is a read/write bit.

*In the PC97338, this bit is a read/write bit in all ECP modes.*

This bit is a read/write bit in EPP mode. In SPP mode it is a write only bit. A read from it returns 1. In SPP Compatible mode and in EPP mode it does not control the direction. See Table 64.

0 - The ECP is in forward direction.

1 - The ECP is in backward direction.

The ECP drives the PD7-0 pins in the forward direction, but does not drive them in the backward direction.

The direction bit, bit 5, is readable and writable. In modes 000 and 010 the direction bit is forced to 0, internally, regardless of the data written into this bit.

0 - ECP drives forward in output mode. (Default)

1 - ECP direction is backward.

**Bits 7,6 - Reserved**

These bits are reserved and are always 1.

### 4.4.9 Parallel Port Data FIFO (CFIFO) Register, Bits 7-5 of ECR = 010, Offset 400h

The Parallel Port FIFO (CFIFO) register is write only. A byte written to this register by PIO or DMA is pushed into the FIFO and tagged as data.

Reading this register has no effect and the data read is undefined.

**FIGURE 81. CFIFO Register Bitmap**

### 4.4.10 ECP Data FIFO (DFIFO) Register, Bits 7-5 of ECR = 011, Offset 400h

This bi-directional FIFO functions as either a write-only device (when DCR bit 5 is 0) or a read-only device (DCR bit 5 is 1).

In the forward direction (bit 5 of DCR is 0), a byte written to the ECP Data FIFO (DFIFO) register by PIO or DMA is pushed into the FIFO and tagged as data. Reading this register when set for write-only has no effect and the data read is undefined.

In the backward direction (bit 5 of DCR is 1), the ECP automatically issues ECP read cycles to fill the FIFO.

Reading from this register pops a byte from the FIFO. Writing to this register when it is set for read-only has no effect, and the data written is ignored.

**FIGURE 82. DFIFO Register Bitmap**

### 4.4.11 Test FIFO (TFIFO) Register, Bits 7-5 of ECR = 110, Offset 400h

A byte written into the Test FIFO (TFIFO) register is pushed into the FIFO. A byte read from this register is popped from the FIFO. The ECP does not issue an ECP cycle to transfer the data to or from the peripheral device.

The TFIFO is readable and writable in both directions. In the forward direction (bit 5 of DCR is 0) PD7-0 are driven, but the data is undefined.

The FIFO does not stall when overwritten or underrun (access is ignored). Bytes are always read from the top of the FIFO, regardless of the direction bit setting (bit 5 of DCR). For example if 44h, 33h, 22h, 11h is written into the FIFO, reading the FIFO returns 44h, 33h, 22h, 11h (in the same order it was written).

**FIGURE 83. TFIFO Register Bitmap**

### 4.4.12 Configuration Register A (CNFGA), Bits 7-5 of ECR = 111, Offset 400h

This register is read only. Reading CNFGA always returns 100 on bits 2 to 0 and 0001 on bits 7 to 4; bit 3 is a reflection of bit 5 of ASC. Writing this register has no effect and the data is ignored.

**FIGURE 84. CNFGA Register Bitmap**

**Bits 2-0 - Reserved**

These bits are reserved and are always 100.

**Bit 3 - Bit 5 of ASC**

This bit reflects the value of bit 5 of the ASC configuration register, which has no specific function. Bit 5 of ASC may be used at the discretion of system programmers, for any purpose. Whatever value is put in bit 5 of the ASC register will appear in bit 3 of the CNFGA register.

The CNFGA register bit reflects a specific system configuration parameter, as opposed to other devices, e.g., 8-bit data word length.

**Bit 7-4 - Reserved**

These bits are reserved and are always 0001.

### 4.4.13 Configuration Register B (CNFGB), Bits 7-5 of ECR = 111, Offset 401h

Configuration register B (CNFGB) is read only. Reading this register returns the configured parallel port interrupt line and DMA channel, and the state of the interrupt line.

Writing to this register has no effect and the data is ignored.

**FIGURE 85. CNFGB Register Bitmap**

**Bits 1,0 - DMA Select Bits**

These bits reflect the value of bits 2 and 1 of the SCF1 configuration register. Microsoft's ECP Protocol and ISA Interface Standard defines these bits shown in Table 69.

Note that bits 2-1 of SCF1 are read/write bits but CNFGB bits are read only.

Upon reset, these bits are initialized to 00.

**TABLE 69. ECP Mode DMA Selection**

| Bit 1 | Bit 0 | DMA Configuration |
|---|---|---|
| 0 | 0 | 8-bit DMA selected by jumpers. (Default) |
| 0 | 1 | DMA channel 1 selected. |
| 1 | 0 | DMA channel 2 selected. |
| 1 | 1 | DMA channel 3 selected. |

**Bit 2 - Reserved**

This bit is reserved and is always 0.

**Bits 5-3 - Interrupt Select Bits**

These bits reflect the value of bits 2-0 of the PNP0 configuration register. Microsoft's ECP Protocol and ISA Interface Standard defines these bits as shown in Table 70.

Bits 2-0 of PNP0 are normal read/write bits but CNFGB bits are read only.

Upon reset, these bits have an undefined value.

**TABLE 70. ECP Mode Interrupt Selection**

| Bit 5 | Bit 4 | Bit 3 | Interrupt Selection |
|---|---|---|---|
| 0 | 0 | 0 | Jumper selection. |
| 0 | 0 | 1 | IRQ7 selected. |
| 0 | 1 | 0 | IRQ9 selected. |
| 0 | 1 | 1 | IRQ10 selected. |
| 1 | 0 | 0 | IRQ11 selected. |
| 1 | 0 | 1 | IRQ14 selected. |
| 1 | 1 | 0 | IRQ15 selected. |
| 1 | 1 | 1 | IRQ5 selected. |

**Bit 6 - IRQ Signal Value**

This bit holds the value of the configured IRQ signal. The value of this bit will be undetermined if the interrupt is not correctly configured on configuration register PNP0, bits 1 and bits 7-4.

**Bit 7 - Reserved**

This bit is reserved and is always 0.

### 4.4.14 Extended Control Register (ECR), Offset 402h

This register controls the ECP and parallel port functions. On reset this register is initialized to 00010101. IOCHRDY is driven low on ECR read when the ECR status bits do not hold updated data.

**FIGURE 86. ECR Register Bitmap**

**Bit 0 - FIFO Empty**

This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored.

When the ECP clock is frozen this bit is read as 1, regardless of the actual FIFO state.

0 - The FIFO has at least one byte of data.

1 - The FIFO is empty or ECP clock is frozen.

**Bit 1 - FIFO Full**

This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored.

When the ECP clock is frozen this bit is read as 1, regardless of the actual FIFO state.

0 - The FIFO has at least one free byte.

1 - The FIFO is full or ECP clock frozen.

**Bit 2 - ECP Service**

This bit enables servicing of interrupt requests. It is set to 1 upon reset, and by the occurrence of interrupt events.

While set to 1, neither DMA nor the interrupt events listed below will generate an interrupt. It is set to 0 by software.

When set to 0, the interrupt setup is "armed" and an interrupt will be generated on occurrence of an interrupt event.

While the ECP clock is frozen, it will always return a 0 value, although it retains its proper value and may be modified while the clock is frozen.

When one of the following interrupt events occurs while this bit is 0, an interrupt is generated and this bit is set to 1 by hardware.

— DMA is enabled (Bit 3 of ECR is 1) and terminal count is reached.

— FIFO write threshold reached (no DMA -Bit 3 of ECR is 0; forward direction - bit 5 of DCR is 0, and there are eight or more bytes free in the FIFO).

— FIFO read threshold reached (no DMA - bit 3 of ECR is 0; read direction set - bit 5 of DCR is 1, and there are eight or more bytes to be read from the FIFO).

0 - The DMA and the above three interrupts are not disabled.

1 - The DMA and the above three interrupts are disabled.

**Bit 3 - ECP DMA Enable**

0 - Depending on the value of bits 7 and 6 of the PNP2 register, the selected pin DRQ0, DRQ1 or DRQ2 is in TRI-STATE, and the appropriate signal $\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$ or $\overline{\text{DACK2}}$ is assumed inactive.

1 - The DMA is enabled and the DMA starts when bit 2 of ECR is 0.

**Bit 4 - ECP Interrupt Mask**

0 - An interrupt is generated on $\overline{\text{ERR}}$ assertion (the high-to-low edge of $\overline{\text{ERR}}$). An interrupt is also generated while $\overline{\text{ERR}}$ is asserted when this bit is changed from 1 to 0; this prevents the loss of an interrupt between ECR read and ECR write.

1 - No interrupt is generated.

**Bits 7-5 - ECP Mode Control**

These bits set the mode for the ECP device. See Section 4.5 for a more detailed description of operation in each of these ECP modes. The ECP modes are listed in Table 71.

**TABLE 71. ECP Modes**

| Mode Code | | | Mode Name | Operation Description |
|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | | |
| 0 | 0 | 0 | Standard mode | Write cycles are under software control.<br>Bit 5 of DCR is forced to 0 (forward direction) and PD7-0 are driven.<br>The FIFO is reset (empty).<br>Reading DATAR returns the last value written to DATAR. |
| 0 | 0 | 1 | PS/2 mode | Read and write cycles are under software control.<br>The FIFO is reset (empty). |
| 0 | 1 | 0 | Parallel port FIFO mode | Write cycles are automatic, i.e., under hardware control ($\overline{\text{STB}}$ is controlled by hardware).<br>Bit 5 of DCR is forced to 0 internally (forward direction) and PD7-0 are driven. |
| 0 | 1 | 1 | ECP FIFO mode | The FIFO direction is automatic, i.e., controlled by bit 5 of DCR.<br>Read and write cycles to the device are controlled by hardware ($\overline{\text{STB}}$ and $\overline{\text{AFD}}$ are controlled by hardware). |
| 1 | 0 | 0 | Reserved | |
| 1 | 0 | 1 | Reserved | |
| 1 | 1 | 0 | FIFO test mode | The FIFO is accessible via the TFIFO register.<br>The ECP does not issue ECP cycles to fill or empty the FIFO. |
| 1 | 1 | 1 | Configuration mode | CNFGA and CNFGB registers are accessible. |

## 4.5 ECP MODE DESCRIPTIONS

### 4.5.1 Software Controlled Data Transfer (Modes 000 and 001)

Software controlled data transfer is supported in modes 000 and 001. The software generates peripheral-device cycles by modifying the DATAR and DCR registers and reading the DSR, DCR and DATAR registers. The negotiation phase and nibble mode transfer, as defined in the IEEE 1284 standard, are performed in these modes.

In these modes the FIFO is reset (empty) and is not functional, the DMA and RLE are idle.

Mode 000 is for the forward direction only; the direction bit (DCR Bit 5) is forced to 0 and PD7-0 are driven. Mode 001 is for both the forward and backward directions. The direction bit controls whether or not pins PD7-0 are driven.

### 4.5.2 Automatic Data Transfer (Modes 010 and 011)

Automatic data transfer (ECP cycles generated by hardware) is supported only in modes 010 and 011 (Parallel Port and ECP FIFO modes). Automatic DMA access to fill or empty the FIFO is supported in modes 010, 011 and 110. Mode 010 is for the forward direction only; the direction bit is forced to 0 and PD7-0 are driven. Mode 011 is for both the forward and reverse directions. The direction bit controls whether PD7-0 are driven.

Automatic Run Length Expanding (RLE) is supported in the reverse direction.

#### Forward Direction (bit 5 of DCR=0)

When the ECP is in forward direction and the FIFO is not full (bit 1 of ECR is 0) the FIFO can be filled by software writes to the FIFO registers (AFIFO and DFIFO in mode 011, and CFIFO in mode 010).

When DMA is enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically issues DMA requests to fill the FIFO with data bytes (not including command bytes).

When the ECP is in forward direction and the FIFO is not empty (bit 0 of ECR is 0) the ECP pops a byte from the FIFO and issues a write signal to the peripheral device. The ECP drives $\overline{AFD}$ according to the operation mode (bits 7-5 of ECR) and according to the tag of the popped byte as follows: In Parallel Port FIFO mode (mode 010) $\overline{AFD}$ is controlled by bit 1 of DCR. In ECP mode (mode 011) $\overline{AFD}$ is controlled by the popped tag. $\overline{AFD}$ is driven high for normal data bytes and driven low for command bytes.

#### ECP (Forward) Write Cycle

An ECP write cycle starts when the ECP drives the popped tag onto $\overline{AFD}$ and the popped byte onto PD7-0. When BUSY is low the ECP asserts $\overline{STB}$. In 010 mode the ECP deasserts $\overline{STB}$ to terminate the write cycle. In 011 mode the ECP waits for BUSY to be high.

When BUSY is high, the ECP deasserts $\overline{STB}$, and changes $\overline{AFD}$ and PD7-0 only after BUSY is low.

**FIGURE 87. ECP Forward Write Cycle**

#### Reverse Direction (Bit 5 of DCR is 1)

When the ECP is in the reverse direction, and the FIFO is not full (bit 1 of ECR is 0), the ECP issues a read cycle to the peripheral device and monitors the BUSY signal. If BUSY is high the byte is a data byte and it is pushed into the FIFO. If BUSY is low the byte is a command byte. The ECP checks bit 7 of the command byte, if it is high the byte is ignored, if it is low the byte is tagged as an RLC byte (not pushed into the FIFO but used as a Run Length Count to expand the next byte read). Following an RLC read the ECP issues a read cycle from the peripheral device to read the data byte to be expanded. This byte is considered a data byte, regardless of its BUSY state (even if it is low). This byte is pushed into the FIFO (RLC+1) times (e.g. for RLC=0, push the byte once. For RLC=127 push the byte 128 times).

When the ECP is in the reverse direction, and the FIFO is not empty (bit 0 of ECR is 0), the FIFO can be emptied by software reads from the FIFO register (true only for the TFIFO in mode 011, not for AFIFO or CFIFO reads).

When DMA is enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically issues DMA requests to empty the FIFO (only in mode 011).

#### ECP (Reverse) Read Cycle

An ECP read cycle starts when the ECP drives $\overline{AFD}$ low.

The peripheral device drives BUSY high for a normal data read cycle, or drives BUSY low for a command read cycle, and drives the byte to be read onto PD7-0.

When $\overline{ACK}$ is asserted the ECP drives $\overline{AFD}$ high. When $\overline{AFD}$ is high the peripheral device deasserts $\overline{ACK}$. The ECP reads the PD7-0 byte, then drives $\overline{AFD}$ low. When $\overline{AFD}$ is low the peripheral device may change BUSY and PD7-0 states in preparation for the next cycle

.

**FIGURE 88. ECP (Reverse) Read Cycle**

**Notes:**

1. FIFO-full condition is checked before every expanded byte push.
2. Switching from modes 010 or 011 to other modes removes pending DMA requests and aborts pending RLE expansion.
3. FIFO pushes and pops are neither synchronized nor linked at the hardware level. The FIFO will not delay these operations, even if performed concurrently. Care must be taken by the programmer to utilize the empty and full FIFO status bits to avoid corrupting PD7-0 or D7-0 while a previous FIFO port access not complete.
4. In the forward direction, the empty bit is updated when the ECP cycle is completed, not when the last byte is popped from the FIFO (valid cleared on cycle end).
5. $\overline{ZWS}$ is not asserted for DMA cycles.
6. The one-bit command/data tag is used only in the forward direction.
7. The DRQ (DMA Request) signal is always deasserted for a minimum of 330 µs after, at most, 32 consecutive DMA acess cycles.
8. If the FDC, UART, and UIR are not enabled (FER Configuration Register) after power-up, the ECP clock is blocked. To enable the ECP clock, set PCR bit 3 (ECP Clock Freeze Control) to enable ECP mode, or set the FER register bit 3 (FDC Enable) and then reset it.

### 4.5.3 FIFO Test Access (Mode 110)

Mode 110 is for testing the FIFO in PIO and DMA cycles. Both read and write operations (pop and push) are supported, regardless of the direction bit.

In the forward direction PD7-0 are driven, but the data is undefined. This mode can be used to measure the system-ECP cycle throughput, usually with DMA cycles. This mode can also be used to check the FIFO depth and its interrupt threshold, usually with PIO cycles.

### 4.5.4 Configuration Registers Access (Mode 111)

The two configuration registers, CNFGA and CNFGB, are accessible only in this mode.

### 4.5.5 Interrupt Generation

An interrupt is generated according to bit 5 and 6 setting in the PCR, when any of the events described in this section occurs. Interrupt events 2, 3 and 4 are level events. They are shaped as interrupt pulses, and are masked (inactive) when the ECP clock is frozen.

**Event 1**

Bit 2 of ECR is 0, bit 3 of ECR is 1 and TC is asserted during ECP DMA cycle. Interrupt event 1 is a pulse event.

**Event 2**

Bit 2 of ECR is 0, bit 3 of ECR is 0, bit 5 of DCR is 0 and there are eight or more bytes free in the FIFO.

This event includes the case when bit 2 of ECR is cleared to 0 and there are already eight or more bytes free in the FIFO (modes 010, 011 and 110 only).

**Event 3**

Bit 2 of ECR is 0, bit 3 of ECR is 0, bit 5 of DCR is 1 and there are eight or more bytes to be read from the FIFO.

This event includes the case when bit 2 of ECR is cleared to 0 and there are already eight or more bytes to be read from the FIFO (modes 011 and 110 only).

**Event 4**

Bit 4 of ECR is 0 and $\overline{ERR}$ is asserted (high to low edge) or $\overline{ERR}$ is asserted when bit 4 of ECR is modified from 1 to 0.

This event may be lost when the ECP clock is frozen.

**Event 5**

When bit 4 of DCR is 1 and $\overline{ACK}$ is deasserted (low-to-high edge).

This event behaves as in the normal SPP mode, i.e., the IRQ signal follows the $\overline{ACK}$ signal transition (when bit 5 of PCR is 0 and bit 6 of PCR is 0).

## 4.6 THE PARALLEL PORT MULTIPLEXER (PPM)

A PPM is used for a PC, which may have an internal Floppy Disk Drive (FDD) connected via regular FDC pins, to interface with either a printer or an external FDD, via a 25-pin DIN connector.

The printer and external FDD may be exchanged, without turning the PC off, and without updating the DOS device tables. The software may assign A to the FDD connected to the regular FDC pins and B to the FDD connected to the PPM pins (the default assignment), or vice versa.

The FDC output signals are always connected to the regular FDC output pins.

The FDC output signals are connected to the PPM output pins when the PPM is enabled (bits 7 and 6 of SIRQ3 are 1 and 0, respectively) and a floppy drive is connected to it (PNF = 0). See Table 72.

The FDC input signals are connected to the regular FDC pins when either bits 7 and 6 of SIRQ3 are not equal to 1 and 0, respectively, or when the PNF signal is active (high).

The FDC input pins are internally multiplexed between the regular FDC pins and the PPM pins when bits 7 and 6 of SIRQ3 are 1 and 0, respectively, and PNF = 0 as follows:

- The PPM pins are connected to the FDC input signals when $\overline{DR1}$=0.
- The regular pins are connected to the FDC input signals when $\overline{DR1}$=1.

To support true floating pins, the pins are back-drive protected.

When bit 3 of FCR is 1, the PPM pins are floated.

When the PPM is not enabled, the parallel port signals are connected to the PPM pins. (The PPM is configured when bits 7,6 of SIRQ3 are 10, and bit 1 of SCF3 is 0.)

When bits 7,6 of SIRQ3 are 10, and PNF=1, the parallel port signals are connected to the PPM pins.

When bits 7,6 of SIRQ3 are 10, and PNF=0, the FDC output signals are connected to the PPM pins.

Reading back the DTR or CTR returns their written values.

Input signals assume their default values (STR register): $\overline{BUSY}$ = 0, PE = 0, SLCT = 0, $\overline{ACK}$ = 1 and thus the parallel port module sees cable not connected.

## 4.7 PARALLEL PORT PIN/SIGNAL LIST

Table 72 on the following page shows the standard 25-pin, D-type connector definition for various parallel port operations

**TABLE 72. Parallel Port Pin Out**

| Connector Pin | PQFP Pin | TQFP Pin | SPP, ECP Mode | I/O | EPP Mode | I/O | PPM Mode and PNF=0 | I/O |
|---|---|---|---|---|---|---|---|---|
| 1 | 95 | 93 | $\overline{STB}$ | I/O | $\overline{WRITE}$ | I/O | - | I |
| 2 | 94 | 92 | PD0 | I/O | PD0 | I/O | $\overline{INDEX}$ | I |
| 3 | 93 | 91 | PD1 | I/O | PD1 | I/O | $\overline{TRK0}$ | I |
| 4 | 92 | 90 | PD2 | I/O | PD2 | I/O | $\overline{WP}$ | I |
| 5 | 91 | 89 | PD3 | I/O | PD3 | I/O | $\overline{RDATA}$ | I |
| 6 | 89 | 87 | PD4 | I/O | PD4 | I/O | $\overline{DSKCHG}$ | I |
| 7 | 88 | 86 | PD5 | I/O | PD5 | I/O | MSEN0 | I |
| 8 | 87 | 85 | PD6 | I/O | PD6 | I/O | DRATE0 | 0 |
| 9 | 86 | 84 | PD7 | I/O | PD7 | I/O | MSEN1 | I |
| 10 | 85 | 83 | $\overline{ACK}$ | I | $\overline{ACK}$ | I | $\overline{DR1}$ | O |
| 11 | 84 | 82 | BUSY | I | $\overline{WAIT}$ | I | $\overline{MTR1}$ | O |
| 12 | 83 | 81 | PE | I | PE | I | $\overline{WDATA}$ | O |
| 13 | 82 | 80 | SLCT | I | SLCT | I | $\overline{WGATE}$ | O |
| 14 | 78 | 76 | $\overline{AFD}$ | I/O | $\overline{DSTRB}$ | I/O | DENSEL | O |
| 15 | 79 | 77 | $\overline{ERR}$ | I | $\overline{ERR}$ | I | $\overline{HDSEL}$ | O |
| 16 | 80 | 78 | $\overline{INIT}$ | I/O | $\overline{INIT}$ | I/O | $\overline{DIR}$ | O |
| 17 | 81 | 79 | $\overline{SLIN}$ | I/O | $\overline{ASTRB}$ | I/O | $\overline{STEP}$ | O |
| 18 - 23 | | | GND | | GND | | GND | |
| 24 | 49 | 47 | PNF = 1 | I | PNF = 1 | I | PNF = 0 | I |
| 25 | | | GND | | GND | | GND | |

# 5.0 Serial Communications Controllers (SCC1 and SCC2)

Two serial communications control modules are provided: SCC1 and SCC2. Either module supports a UART mode of operation and is backward compatible with the 16550 and 16450. In addition to UART mode, SCC2 also provides infrared capabilities by supporting 5 additional operating modes.

The description of the UART mode in the following sections applies to both SCC1 and SCC2; the description of the infrared modes applies to SCC2 only.

The infrared modes supported by SCC2 are: Sharp-IR, IrDA 1.0 SIR, IrDA 1.1 MIR and FIR, and Consumer Electronics IR (also referred to as TV Remote or Consumer Remote Control).

In order to support existing legacy software based upon the 16550 UART, both modules provide a special fallback mechanism that automatically sets the operational mode to 16550 compatibility mode when the baud generator divisor is accessed through the legacy ports in bank 1.

The modules' architecture has been optimized to meet the requirements of a variety of UART and infrared based applications. DMA support for all operational modes has been incorporated into the architecture.

The modules can use either 1 or 2 DMA channels. One channel is required for infrared based applications since infrared communications work in half duplex fashion. Two channels would normally be needed to handle high-speed full duplex UART based applications.

To further ease driver design and simplify the implementation of infrared protocols, a 12-bit timer with 125 us resolution has also been included.

Note: Upon reset, SCC2 can wake up in either UART mode or SIR mode depending on the state of the CFG0 strap pin.

— If CFG0 is sampled low, SCC2 wakes up in SIR mode.

— If CFG0 is sampled high, SCC2 wakes up in UART mode.

## 5.1 FEATURES

- Fully compatible with 16550 and 16450
- Extended UART mode
- Sharp-IR with selectable internal or external modulation/demodulation
- IrDA 1.0 SIR with up to 115.2 kbaud data rate
- IrDA 1.1 MIR and FIR with 0.576, 1.152 and 4.0 Mbps data rates
- Consumer Electronic IR mode
- UART mode data rates up to 1.5 Mbps
- Back-to-Back infrared frame transmission and reception
- Full duplex infrared frame transmission and reception
- Transmit deferral
- Automatic fallback to 16550 compatibility mode
- IrDA modes pipelining
- Selectable 16 or 32 level FIFOs
- Support for Plug-n-Play Infrared Adapters
- Automatic or manual transceiver configuration
- 12-bit timer for infrared protocol support

## 5.2 FUNCTIONAL MODES OVERVIEW

This multi-mode module can be configured to act as any one of several different functions. Although each mode is unique, certain system resources and features are common to some or to all modes.

## 5.3 UART MODE

This mode is designed to support serial data communications with a remote peripheral module or modem using a wired interface. The module provides transmit and receive channels that can operate concurrently to handle full-duplex operation. They perform parallel-to-serial conversion on data characters received from the CPU or a DMA controller, and serial-to-parallel conversion on data characters received from the serial interface. The format of the serial data stream is shown in Figure 88. A data character contains 5 to 8 data bits. It is preceded by a start bit and is followed by an optional parity bit and a stop bit. Data is transferred in Little Endian order (LEAST significant bit first).

**FIGURE 88. Composite Serial Data**

The UART mode is the default mode of operation after power up or reset. In fact, after reset, the module enters the 16450 compatibility mode. In addition to the 16450 and 16550 compatibility modes, an extended mode of operation is also available. When the extended mode is selected, the module architecture changes slightly and a variety of additional features are made available. The interrupt sources are no longer prioritized, and an auxiliary status and control register replaces the scratch pad register. The additional features include: transmitter FIFO thresholding, DMA capability, and interrupts on transmitter empty and DMA event.

The clock for both transmit and receive channels is provided by an internal baud generator that divides its input clock by any divisor value from 1 to $2^{16}$ –1. The output clock frequency of the baud generator must be programmed to be sixteen times the baud rate value. The baud generator input clock is derived from a 24 MHz clock through a programmable prescaler. The prescaler value is determined by the PRESL bits in the EXCR2 register. Its default value is 13. This allows all the standard baud rates, up to 115.2 kbaud to be obtained. Smaller prescaler values will allow baud rates up to 921.6 kbaud (standard) and 1.5 Mbaud (non standard).

Before operation can begin, both the communications format and baud rate must be programmed by the software. The communications format is programmed by loading a control byte into the LCR register, while the baud rate is selected by loading an appropriate value into the baud generator divisor register. The software can read the status of the module at any time during operation. The status information includes FULL/EMPTY state for both transmit and receive channels, and any other condition detected on the received data stream, like a parity error, framing error, data overrun, or break event.

## 5.4 SHARP-IR MODE

This mode supports bi-directional data communication with a remote module using infrared radiation as the transmission medium. Sharp-IR uses Digital Amplitude Shift Keying (DASK) and allows serial communication at baud rates up to 38.4 kbaud. The format of the serial data is similar to the UART data format. Each data word is sent serially beginning with a zero value start bit, an optional parity bit, and ending with at least one stop bit with a binary value of one. A zero is signalled by sending a 500 kHz continuous pulse train of infrared radiation. A one is signaled by the absence of any infrared signal. The PC97338 can perform the modulation and demodulation operations internally, or it can rely on the external optical module to perform them.

Operation in Sharp-IR is similar to the operation in UART mode. The main difference being that data transfer operations are normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of the Sharp-IR mode is controlled by the MDSL bits in the MCR register when the module is in extended mode, or by the IR_SL bits in the IRCR1 register when the module is in non-extended mode. This prevents legacy software, running in non-extended mode, from spuriously switching the module to UART mode, when the software writes to the MCR register.

## 5.5 IrDA 1.0 SIR MODE

This is the first operational mode that has been defined by the IrDA committee and, similarly to Sharp-IR, it also supports bi-directional data communication with a remote module using infrared radiation as the transmission medium. IrDA 1.0 SIR allows serial communication at baud rates up to 115.2 kbaud. The format of the serial data is similar to the UART data format. Each data word is sent serially beginning with a zero value start bit, followed by 8 data bits, and ending with at least one stop bit with a binary value of one. A zero is signaled by sending a single infrared pulse. A one is signaled by not sending any pulse. The width of each pulse can be either 1.6 µs or 3/16ths of a single bit time. (1.6 µs equals 3/16ths of a bit time at 115.2 kbaud). This way, each word begins with a pulse for the start bit.

Operation in IrDA 1.0 SIR is similar to the operation in UART mode. The main difference being that data transfer operations are normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of the IrDA 1.0 SIR mode is controlled by the MDSL bits in the MCR register when the module is in extended mode, or by the IR_SL bits in the IRCR1 register when the module is in non-extended mode. This prevents legacy software, running in non-extended mode, from spuriously switching the module to UART mode, when the software writes to the MCR register.

## 5.6 IrDA 1.1 MIR AND FIR MODES

The PC97338 supports both IrDA 1.1 MIR and FIR modes, with data rates of 576 kbps, 1.152 Mbps and 4.0 Mbps. Details on the frame format, encoding schemes, CRC sequences, etc. are provided in the appropriate IrDA documents. The MIR transmitter front-end section performs bit stuffing on the outbound data stream and places the Start and Stop flags at the beginning and end of MIR frames. The MIR receiver front-end section removes flags and “destuffs” the inbound bit stream, and checks for abort conditions.

The FIR transmitter front-end section adds the Preamble as well as Start and Stop flags to each frame and encodes the transmit data into a 4PPM (Four Pulse Position Modulation) data stream. The FIR receiver front-end section strips the Preamble and flags from the inbound data stream and decodes the 4PPM data while also checking for coding violations.

Both MIR and FIR front-ends also automatically append CRC sequences to transmitted frames and check for CRC errors on received frames.

### 5.6.1 High Speed Infrared Transmit Operation

When the transmitter is empty, if either the CPU or the DMA controller writes data into the TX_FIFO, transmission of a frame will begin. Frame transmission can be normally completed by using one of the following methods:

1. **S_EOT bit (Set End of Transmission).** This method is used when data transfers are performed in PIO mode. When the CPU sets the S_EOT bit before writing the last byte into the TX_FIFO, the byte will be tagged with an EOF indication. When this byte reaches the TX_FIFO bottom, and is read by the transmitter front-end, a CRC is appended to the transmitted DATA and the frame is normally terminated.
2. **DMA TC Signal (DMA Terminal Count).** This method is used when data transfers are performed in DMA mode. It works similarly to the previous method except that the tagging of the last byte of a frame occurs when the DMA controller asserts the TC signal during the write of the last byte to the TX_FIFO.
3. **Frame Length Counter.** This method can be used when data transfers are performed in either PIO or DMA mode. The value of the FEND_MD bit in the IRCR2 register determines whether the Frame Length Counter is effective in the PIO or DMA mode. The counter is loaded from the Frame Length Register (TFRL) at the beginning of each frame, and it is decremented as each byte is transmitted. An EOF is generated when the counter reaches zero. When used in DMA mode with an 8237 type DMA controller, this method allows a large data block to be automatically split into equal-size back-to-back frames, plus a shorter frame that is terminated by the DMA TC signal, if the block size is not an exact multiple of the frame size.

   An option is also provided to stop transmission at the end of each frame. This happens when the transmitter Frame-End stop mode is enabled (TX_MS bit in the IRCR2 register set to 1). By using this option, the software can send frames of different sizes without re-initializing the DMA controller for each frame. After transmission of each frame, the transmitter stops and generates an interrupt. The software loads the length of the next frame into the TFRL register and restarts the transmitter by clearing the TXHFE bit in the ASCR register.

**Note:** PIO or DMA mode is only controlled by the setting of the DMA_EN bit in the extended-mode MCR register. The module treats CPU and DMA access cycles the same except that DMA cycles always access the TX or RX_FIFO, regardless of the selected bank. When DMA_EN is set to 1, the CPU can still access the TX_FIFO and RX_FIFO. The CPU accesses will, however, be treated as DMA accesses as far as the function of the FEND_MD bit is concerned.

While a frame is being transmitted, data must be written to the TX_FIFO at a rate dictated by the transmission speed. If the CPU or DMA controller fails to meet this requirement, a transmitter underrun will occur, an inverted CRC is appended to the frame being transmitted, and the frame is terminated with a Stop flag. Data transmission will then stop. Transmission of the inverted CRC will guarantee that the remote receiving module will receive the frame with a CRC error and will discard it.

Following an underrun condition, data transmission always stops at the next frame boundary. The frame bytes from the point where the underrun occurred to the end of the frame will not be sent out to the external infrared interface. Nonetheless, they will be removed from the TX_FIFO by the transmitter and discarded. The underrun indication will be reported only when the transmitter detects the end of frame via one of the methods described above. The software can do various things to recover from an underrun condition. For example, it can simply clear the underrun condition by writing a 1 into bit 6 of ASCR and re-transmit the underrun frame later, or it can re-transmit it immediately, before transmitting other frames.

If it chooses to re-transmit the frame immediately, it needs to perform the following steps:

1. Disable DMA controller, if DMA mode was selected.
2. Read the TXFLV register to determine the number of bytes in the TX_FIFO. (This is needed to determine the exact point where the underrun occurred, and whether or not the first byte of a new frame is in the TX_FIFO).
3. Reset TX_FIFO.
4. Backup DMA controller registers.
5. Clear Transmitter underrun bit.
6. Re-enable DMA controller.

### 5.6.2 High Speed Infrared Receive Operation

When the receiver front-end detects an incoming frame, it will start de-serializing the infrared bit stream and load the resulting data bytes into the RX_FIFO. When the EOF is detected, two or four CRC bytes are appended to the received data, and an EOF flag is written into the tag section of the RX_FIFO along with the last byte. In the present implementation, the CRC bytes are always transferred to the RX_FIFO following the data. Additional status information, related to the received frame, is also written into the RX_FIFO tag section at this time. The status information will be loaded into the LSR register when the last frame byte reaches the RX_FIFO bottom.

The receiver keeps track of the number of received bytes from the beginning of the current frame. It will only transfer to the RX_FIFO a number of bytes not exceeding the maximum frame length value which is programmed via the RFRML register in bank 4. Any additional frame bytes will be discarded. When the maximum frame length value is exceeded, the MAX_LEN error flag will be set.

Although data transfers from the RX_FIFO to memory can be performed either in PIO or DMA mode, DMA mode should be used due to the high data rates.

In order to handle back-to-back incoming frames, when DMA mode is selected and an 8237 type DMA controller is used, an 8-level ST_FIFO (Status FIFO) is provided. When an EOF is detected, in 8237 DMA mode, the status and byte count information for the frame is written into the ST_FIFO. An interrupt is generated when the ST_FIFO level reaches a programmed threshold or an ST_FIFO time-out occurs.

The CPU uses this information to locate the frame boundaries in the memory buffer where the data, belonging to the received frames, has been transferred by the 8237 type DMA controller.

During reception of multiple frames, if the RX_FIFO and/or the ST_FIFO fills up, due to the DMA controller or CPU not serving them in time, one or more frames can be crushed and lost. This means that no bytes belonging to these frames were written to the RX_FIFO. In fact, a frame will be lost in 8237 mode when the ST_FIFO is full for the entire time during which the frame is being received, even though there were empty locations in the RX_FIFO. This is because no data bytes can be loaded into the RX_FIFO and then transferred to memory by the DMA controller, unless there is at least one available entry in the ST_FIFO to store the number of received bytes. This information, as mentioned before, is needed by the software to locate the frame boundaries in the DMA memory buffer.

In the event that a number of frames are lost, for any of the reasons mentioned above, one or more lost-frame indications including the number of lost frames, are loaded into the ST_FIFO.

Frames can also be lost in PIO mode, but only when the RX_FIFO is full. The reason being that, in these cases, the ST_FIFO is only used to store lost-frame indications. It will not store frame status and byte count.

## 5.7 CONSUMER ELECTRONIC IR (CEIR) MODE

The CEIR circuitry is designed to optimally support all the major protocols presently used in remote-controlled home entertainment equipment. The main protocols currently in use are: RC-5, RC-6, RECS 80, NEC and RCA. The PC87108, in conjunction with an external optical module, provides the physical layer functions necessary to support these protocols. These functions include modulation, demodulation, serialization, de-serialization, data buffering, status reporting, interrupt generation, etc. The software is responsible for the generation of the infrared code to be transmitted, and for the interpretation of the received code.

### 5.7.1 CEIR Transmit Operation

The code to be transmitted consists of a sequence of bytes that represent either a bit string or a set of run-length codes. The number of bits or run-length codes usually needed to represent each infrared code bit depends on the infrared protocol used. The RC-5 protocol, for example, needs two bits or between one and two run-length codes to represent each infrared code bit.

CEIR transmission starts when the transmitter is empty and either the CPU or the DMA controller writes code bytes into the TX_FIFO. The transmission is normally completed when the CPU sets the S_EOT bit in the ASCR register before writing the last byte, or when the DMA controller activates the TC signal. Transmission is also completed if the CPU simply stops transferring data and the transmitter becomes empty. In this case however, a transmitter underrun condition will be generated. The underrun must be cleared before the next transmission can occur. The code bytes written into the TX_FIFO are either de-serialized or run-length decoded, and the resulting bit string is modulated by a subcarrier signal and sent to the transmitter LED. The bit rate of this bit string, like in the UART mode, is determined by the value programmed in the baud generator divisor register. Unlike a UART transmission, start, stop and parity bits are not included in the transmitted data stream. A logic 1 in the bit string will keep the LED off, so no infrared signal is transmitted. A logic 0 will generate a sequence of modulating pulses which will turn on the transmitter LED. Frequency and pulse width of the modulating pulses are programmed by the MCFR and MCPW bits in the IRTXMC register as well as the TXHSC bit in the RCCFG register.

The RC_MMD bits select the transmitter modulation mode. If C_PLS mode is selected, modulation pulses are generated continuously for the entire time in which one or more logic 0 bits are being transmitted. If 6_PLS or 8_PLS modes are selected, 6 or 8 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit. C_PLS modulation mode is used for RC-5, RC-6, NEC and RCA protocols. 8_PLS or 6_PLS modulation mode is used for the RECS 80 protocol. The 8_PLS or 6_PLS mode allows minimization of the number of bits needed to represent the RECS 80 infrared code sequence. The current transmitter implementation supports only the modulated modes of the RECS 80 protocol. The flash mode is not supported since it is not popular and is becoming less frequently used.

**Note:** The total transmission time for the logic 0 bits must be equal or greater than 6 or 8 times the period of the modulation subcarrier, otherwise fewer pulses will be transmitted.

### 5.7.2 CEIR Receive Operation

The CEIR receiver is significantly different from a UART receiver for two basic reasons. First, the incoming infrared signals are DASK modulated. Therefore, a demodulation operation may be necessary. Second, there are no start bits in the incoming data stream.

Whenever an infrared signal is detected, the operations performed by the receiver are slightly different depending on whether or not receiver demodulation is enabled. If the demodulator is not enabled, the receiver will immediately switch to the active state. If the demodulator is enabled, the receiver checks the subcarrier frequency of the incoming signal, and it switches to the active state only if the frequency falls within the programmed range. If this is not the case, the signal is ignored and no other action is taken.

When the receiver active state is entered, the RXACT bit in the ASCR register is set to 1. Once in the active state, the receiver keeps sampling the infrared input signal and generates a bit stream where a logic 1 indicates an idle condition and a logic 0 indicates the presence of infrared energy. The infrared input is sampled regardless of the presence of infrared pulses at a rate determined by the value loaded into the baud generator divisor register. The received bit string is either de-serialized and assembled into 8-bit characters, or it is converted to run-length encoding values. The resulting data bytes are then transferred to the RX_FIFO.

The receiver also sets the RXWDG bit in the ASCR register each time an infrared pulse signal is detected. This bit is automatically cleared when the ASCR register is read, and it is intended to assist the software in determining when the infrared link has been idle for a certain time. The software can then stop the data reception by writing a 1 into the RXACT bit to clear it and return the receiver to the inactive state.

The frequency bandwidth for the incoming modulated infrared signal is selected by DFR and DBW bits in the IRRXDC register. There are two CEIR receiver data modes: “Over-sampled” and “Programmed-T-Period” mode. For either mode the sampling rate is determined by the setting of the baud generator divisor register.

The “Over-sampled” mode can be used with the receiver demodulator either enabled or disabled. It should be used with the demodulator disabled when a detailed snapshot of the incoming signal is needed, for example to determine the period of the subcarrier signal. If the demodulator is enabled, the stream of samples can be used to reconstruct the incoming bit string. To obtain a good resolution, a fairly high sampling rate should be selected.

The “Programmed-T-Period” mode should be used with the receiver demodulator enabled. The T Period represents one half bit time, for protocols using biphase encoding, or the basic unit of pulse distance, for protocols using pulse distance encoding. The baud rate is usually programmed to match the T Period. For long periods of logic low or high, the receiver samples the demodulated signal at the programmed sampling rate.

Whenever a new infrared energy pulse is detected, the receiver will re-synchronize the sampling process to the incoming signal timing. This reduces timing related errors and eliminates the possibility of missing short infrared pulse sequences, especially when dealing with the RECS 80 protocol. In addition, the “Programmed-T-Period” sampling minimizes the amount of data used to represent the incoming infrared signal, therefore reducing the processing overhead in the host CPU.

## 5.8 FIFO TIME-OUTS

In order to prevent received data from sitting in the RX_FIFO and/or the ST_FIFO indefinitely, if the programmed interrupt or DMA thresholds are not reached, time-out mechanisms are provided.

An RX_FIFO time-out generates a receiver High-Data-Level interrupt and/or a Receiver DMA request if bit 0 of IER and/or bit 2 of MCR (in extended mode) are set to 1 respectively. An RX_FIFO time-out also sets bit 0 of ASCR to 1 if the RX_FIFO is below the threshold. This bit is tested by the software, when a

receiver High-Data-Level interrupt occurs, to decide whether a number of bytes, as indicated by the RX_FIFO threshold, can be read without checking bit 0 of the LSR register. An ST_FIFO time-out is enabled only in MIR and FIR modes, and generates an interrupt if bit 6 of IER is set to 1.

The conditions that must exist for a time-out to occur in the various modes of operation, are described below. When a time-out has occurred, it can only be reset when the FIFO that caused the time-out is read by the CPU or DMA controller.

***MIR or FIR Modes***

**RX_FIFO Time-out Conditions:**

1. At least one byte is in the RX_FIFO, and
2. More than 64 µs have elapsed since the last byte was loaded into the RX_FIFO from the receiver logic, and
3. More than 64 µs have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

**ST_FIFO Time-out Conditions:**

1. At least one entry is in the ST_FIFO, and
2. More than 1 ms has elapsed since the last byte was loaded into the RX_FIFO by the receiver logic, and
3. More than 1 ms has elapsed since the last entry was read from the ST_FIFO by the CPU.

***UART, Sharp-IR, SIR Modes***

**RX_FIFO Time-out Conditions:**

1. At least one byte is in the RX_FIFO, and
2. More than four character times have elapsed since the last byte was loaded into the RX_FIFO from the receiver logic, and
3. More than four character times have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

***CEIR Mode***

**RX_FIFO Time-out Conditions:**

The RX_FIFO Time-out, in CEIR mode, is disabled while the receiver is active. The conditions for this time-out to occur are as follows:

1. At least one byte has been in the RX_FIFO for 64 µs or more, and
2. The receiver has been inactive (RXACT=0) for 64 µs or more, and
3. More than 64 µs have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

## 5.9 TRANSMIT DEFERRAL

This feature allows the software to send short high-speed data frames in PIO mode without the risk of a transmitter underrun being generated. Even though this feature is available and works the same way in all modes, it will most likely be used in MIR and FIR modes to support high-speed negotiations. This is because in other modes, either the transmit data rate is relatively low and thus the CPU can keep up with it without letting an underrun occur, as in the case CEIR Mode, or transmit underruns are allowed and are not considered to be error conditions.

Transmit deferral is available only in extended mode and when the TX_FIFO is enabled. When transmit deferral is enabled (TX_DFR bit of MCR set to 1) and the transmitter becomes empty, an internal flag will be set that locks the transmitter. If the CPU now writes data into the TX_FIFO, the transmitter will not start sending the data until the TX_FIFO level reaches either 14 for a 16-level TX_FIFO, or 30 for a 32-level TX_FIFO, at which time the internal flag is cleared. The internal flag is also cleared and the transmitter starts transmitting when a time-out condition is reached. This prevents some bytes from being in the TX_FIFO indefinitely if the threshold is not reached.

The time-out mechanism is implemented by a timer that is enabled when the internal flag is set and there is at least one byte in the TX_FIFO. Whenever a byte is loaded into the TX_FIFO the timer gets reloaded with the initial value. If no bytes are loaded for a 64-s time, the timer times out and the internal flag gets cleared, thus enabling the transmitter.

## 5.10 AUTOMATIC FALLBACK TO 16550 COMPATIBILITY MODE

This feature is designed to support existing legacy software packages using the 16550 UART.

For proper operation, many of these software packages require that the module look identical to a plain 16550 since they access the UART registers directly.

Due to the fact that several extended features as well as new operational modes are provided, the user must make sure that the module is in the proper state before a legacy program can be executed.

The fallback mechanism is designed for this purpose. It eliminates the need for user intervention to change the state of the module, when a legacy program must be executed following completion of a program that used any of the module's extended features.

This mechanism automatically switches the module to 16550 compatibility mode and turns off any extended features whenever the baud generator divisor register is accessed through the LBGD(L) or LBGD(H) ports in register bank 1.

In order to avoid spurious fallbacks, baud generator divisor ports are provided in bank 2. Accesses of the baud generator divisor through these ports will change the baud rate setting but will not cause a fall back.

New programs, designed to take advantage of the extended features, should not use LBGD(L) and LBGD(H) to change the baud rate. They should use BGD(L) and BGD(H) instead.

A fallback can occur from either extended or non-extended modes. If extended mode is selected, fallback is always enabled. In this case, when a fallback occurs, the following happens:

1. Transmitter and receiver FIFOs will switch to 16 levels.
2. A value of 13 will be selected for the baud generator prescaler.
3. The ETDLBK and BTEST bits in the EXCR1 Register will be cleared.
4. UART mode will be selected.
5. A switch to non-extended mode will occur.

When a fallback occurs from non-extended mode, only the first three of the above actions will take place. No switching to UART mode occurs if either Sharp_IR or SIR infrared modes were selected. This prevents spurious switchings to UART mode when a legacy program, running in infrared mode, accesses the baud generator divisor register from bank 1.

Fallback from non-extended mode can be disabled by setting the LOCK bit in the EXCR2 register. When Lock is set to 1 and the module is in non-extended mode, two scratchpad registers overlayed with LBGD(L) and LBGD(H) are enabled. Any attempted CPU access of the baud generator divisor register through LBGD(L) and LBGD(H) will access the scratchpad registers, and the baud rate setting will not be affected. This feature allows existing legacy programs to run faster than 115.2 kbaud without their being aware of it.

## 5.11 PIPELINING

This feature is designed to support the IrDA infrared modes and it allows minimization of the time delay from the end of a negotiation phase to the subsequent data transfer phase.

The module accomplishes this objective by automatically selecting a new mode and/or loading new values into the baud generator divisor register as soon as the current data transmission completes and the transmitter becomes empty. The new operational mode and the baud divisor value are programmed into special pipeline registers.

Pipelining is automatically disabled after a pipeline operation takes place. It should be re-enabled by the software after the special pipeline registers have been reloaded.

Even though there are no other restrictions between source and target modes, aside from having to be IrDA modes, pipelining will most likely be used from SIR as the source mode, since SIR is the mode used by the negotiation procedures in the presently defined IrDA protocols.

Following a pipeline operation, the transmitter will be halted for 250 μs to allow the newly selected receive filter in the remote optical transceiver to stabilize. If a switch from either MIR or FIR to SIR occurred as a result of pipelining, the transmitter will be halted for 250 μs or a character time (at the newly selected baud rate), whichever is greater. This is to guarantee that reception at a remote station of any character triggered by an interaction pulse is complete before the next SIR data transmission begins.

Since a pipelining operation is performed without software intervention, automatic transceiver configuration must be enabled.

## 5.12 OPTICAL TRANSCEIVER INTERFACE

The PC97338 implements a very flexible interface for the external infrared transceiver. Several signals are provided for this purpose. A transceiver module with one or two receive signals, or two transceiver modules can be directly interfaced without any additional logic.

Since various operational modes are supported, the transmitter power as well as the receiver filter in the transceiver module must be configured according to the selected mode.

The PC97338 provides three special interface pins ID/IRSL[2–0] to control the infrared transceiver. The logic levels of the ID/IRSL[2–0] pins can be either directly controlled by the software (through the setting of bits 2–0 in the IRCFG1 register), or can be automatically selected by the module whenever a new mode is entered.

The automatic transceiver configuration is enabled by setting the AMCFG bit in the IRCFG4 register to 1. One of its advantages is that it allows the low-level functional details of the transceiver module being used to be hidden from the software drivers. It also speeds up the transceiver mode selection, and it must be enabled if the pipelining feature is to be used.

The operational mode settings for the automatic configuration are determined by various bit fields in the IRCFGn registers that must be programmed when the module is initialized.

The ID/IR_SL[2–0] pins will power up as inputs and can be driven by an external source. When in input mode, they can be used to read the identification data of Plug-n-Play infrared adapters.

The ID0/IRSL0/IRRX2 pin can also function as an input to support an additional infrared receive signal. In this case, however, only two configuration pins will be available. The IRSL0_DS and IRSL21_DS bits in the IRCFG4 register determine the direction of the ID/IRSL[2–0] pins.

## 5.13 ARCHITECTURAL DESCRIPTION

Eight register banks are provided to control the operation of the UIR module. These banks are mapped into the same address range, and only the selected bank is directly accessible by the software. The address range spans 8 byte locations. The BSR register is used to select the bank and is common to all banks. Therefore, each bank defines seven new registers. The register banks can be divided into two sets. Banks 0–3 are used to control both UART and infrared modes of operation; banks 4–7 are used to control and configure the infrared modes only. The register bank main functions are listed in Table 73. Descriptions of the various registers are given in the following sections.

**FIGURE 88. Register Bank Architecture**

**TABLE 73. Register Bank Summary**

| Bank | UART Mode | IR Mode | Description |
|---|---|---|---|
| 0 | ✓ | ✓ | Global Control and Status Registers |
| 1 | ✓ | ✓ | Legacy Bank |
| 2 | ✓ | ✓ | Baud Generator Divisor and Extended Control |
| 3 | ✓ | ✓ | Identification and Shadow Registers |
| 4 | | ✓ | Timer and Counters |
| 5 | | ✓ | Infrared Control and Status FIFO |
| 6 | | ✓ | Infrared Physical Layer Configuration |
| 7 | | ✓ | CEIR and Optical Transceiver Configuration |

## 5.14 BANK 0

**TABLE 74. Bank 0 Serial Controller Base Registers þ**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | TXD/ RXD | Transmitter/Receiver Data Ports |
| 01h | IER | Interrupt Enable Register |
| 02h | EIR/ FCR | Event Identification/ FIFO Control Registers |
| 03h | LCR/ BSR | Link Control/Bank Select Registers |
| 04h | MCR | Modem/Mode Control Register |
| 05h | LSR | Link Status Register |
| 06h | MSR | Modem Status Register |
| 07h | SPR/ ASCR | Scratchpad/ Auxiliary Status and Control Registers |

### 5.14.1 TXD/RXD – Transmit/Receive Data Ports

These ports share the same address.

TXD is accessed during CPU write cycles. It provides the write data path to the transmitter holding register when the FIFOs are disabled, or to the TX_FIFO top location when the FIFOs are enabled.

RXD is accessed during CPU read cycles. It provides the read data path from the receiver holding register when the FIFOs are disabled, or from the RX_FIFO bottom location when the FIFOs are enabled.

DMA cycles always access the transmitter and receiver holding registers or FIFOs, regardless of the selected bank.

### 5.14.2 IER – Interrupt Enable Register

This register controls the enabling of the various interrupts. Some interrupts are common to all operating modes, while others are only available with specific modes. Bits 4 to 7 can be set in extended mode only. They are cleared in non-extended mode. When a bit is set to 1, an interrupt is generated when the corresponding event occurs. In the non-extended mode most events can be identified by reading the LSR and MSR registers. The receiver high-data-level event can only be identified by reading the EIR register after the corresponding interrupt has been generated. In the extended mode events are identified by event flags in the EIR register. Upon reset, all bits are set to 0.

**Note 1:** If the interrupt signal drives an edge-sensitive interrupt controller input, it is advisable to disable all interrupts by clearing all the IER bits upon entering the interrupt routine, and re-enable them just before exiting it. This will guarantee proper interrupt triggering in the interrupt controller in case one or more interrupt events occur during execution of the interrupt routine.If an interrupt source must be disabled, the CPU can do so by clearing the corresponding bit in the IER register. However, if an interrupt event occurs just before the corresponding enable bit in the IER register is cleared, a spurious interrupt may be generated. To avoid this problem, the clearing of any IER bit should be done during execution of the interrupt service routine.

**Note 2:** If the interrupt controller is programmed for level-sensitive interrupts, the clearing of IER bits can also be performed outside the interrupt service routine, but with the CPU interrupt disabled.

**Note 3:** If the LSR, MSR or EIR registers are to be polled, the interrupt sources which are identified via self-clearing bits should have their corresponding IER bits set to 0. This will prevent spurious pulses on the interrupt output pin.

**FIGURE 88. Interrupt Enable Register**

**B0 RXHDL_IE – Receiver High-Data-Level Interrupt Enable.**

**B1 TXLDL_IE – Transmitter Low-Data-Level Interrupt Enable.**

**B2** *UART, Sharp-IR, SIR Modes*

**LS_IE – Link Status Interrupt Enable.**

*MIR, FIR, CEIR Modes*

**LS_IE/TXHLT_IE – Link Status/Transmitter Halted Interrupt Enable.**

**B3 MS_IE – Modem Status Interrupt Enable.**

**B4 DMA_IE – DMA Interrupt Enable.**

**B5** ***UART, Sharp-IR, CEIR Modes***

**TXEMP_IE – Transmitter Empty Interrupt Enable.**

*SIR, MIR, FIR Modes*

**TXEMP_IE/PLD_IE – Transmitter Empty/Pipeline Load Interrupt Enable.**

**B6** *MIR, FIR Modes*

**SFIF_IE – ST_FIFO Interrupt Enable.**

**B7 TMR_IE – Timer Interrupt Enable.**

### 5.14.3 EIR/FCR – Event Identification/FIFO Control Registers

These registers share the same address.

EIR is accessed during CPU read cycles while FCR is accessed during CPU write cycles.

**EIR** – **Event Identification Register, Read-Only.**

The function of this register changes depending upon whether the module is in extended or non-extended mode.

## Non-Extended Mode

The function of EIR is the same as in the 16550. It returns an encoded value representing the highest priority pending interrupt. While a CPU access is occurring, the module records new interrupts, but it does not change the currently encoded value until the access is complete. Table 75 shows the interrupt priorities and the EIR encoded values.

**FIGURE 88. Event Identification Register, Non-Extended Mode**

**B0 IPF – Interrupt Pending Flag.**
When this bit is 0, an interrupt is pending.
When it is 1, no interrupt is pending.

**B2–1 IPR [1–0] – Interrupt Priority.**
When bit 0 is 0, these bits identify the highest priority pending interrupt.

**B3 RXFT – RX_FIFO Time-out.**
In the 16450 mode this bit is always 0.
In the 16550 mode (FIFOs enabled), this bit is set when an RX_FIFO time-out occurred and the associated interrupt is currently the highest priority pending interrupt.

**B5–4 These bits always return 0.**

**B7–6 FEN [1–0] – FIFOs Enabled.**
These bits are set to 1 when the FIFOs are enabled (bit 0 of FCR set to 1).

**TABLE 75. Non-Extended Mode Interrupt Priorities**

| EIR Bits 3 2 1 0 | Priority Level | Interrupt Type | Interrupt Source | Interrupt Reset Control |
|---|---|---|---|---|
| 0 0 0 1 | N/A | None | None | N/A |
| 0 1 1 0 | Highest | Link Status | Parity error, framing error, data over-run or break event | Reading LSR Register |
| 0 1 0 0 | Second | Receiver High-Data-Level Event | Receiver Holding Register (RXD) full, or RX_FIFO level equal to or above threshold | Reading the RXD port, or RX_FIFO level drops below threshold |
| 1 1 0 0 | Second | RX_FIFO Time-Out | At least one character in RX_FIFO, and no character has been input to or read from the RX_FIFO for 4 character times | Reading the RXD port |
| 0 0 1 0 | Third | Transmitter Low-Data-Level Event | Transmitter Holding Register or TX_FIFO empty | Reading the EIR Register if this interrupt is currently the highest priority pending interrupt, or writing into the TXD port |
| 0 0 0 0 | Fourth | Modem Status | Any transition on $\overline{CTS}$, $\overline{DSR}$, or $\overline{DCD}$, or a low-to-high transition on $\overline{RI}$ | Reading the MSR Register |

## Extended Mode

The EIR register does not return an encoded value like in the non-extended mode. Each bit represents an event flag and is set to 1 when the corresponding event occurred or is pending, regardless of the setting of the corresponding bit in the IER register. Bit 4 is cleared when this register is read if an 8237 type DMA controller is used. All other bits are cleared when the corresponding interrupts are acknowledged.

**FIGURE 88. Event Identification Register, Extended Mode**

**B0 RXHDLEV – Receiver High-Data-Level Event.**

FIFOs Disabled: Set to 1 when one character is in the receiver holding register.

FIFOs Enabled: Set to 1 when the RX_FIFO level is equal to or above the threshold level, or an RX_FIFO time-out has occurred.

**B1 TXLDL_EV – Transmitter Low-Data-Level Event.**

FIFOs Disabled: Set to 1 when the transmitter holding register is empty.

FIFOs Enabled: Set to 1 when the TX_FIFO level is below the threshold level.

**B2** *UART, Sharp-IR, SIR Modes*

**LS_EV – Link Status Event.**

Set to 1 when a receiver error or break condition is reported.

Note that, when the FIFOs are enabled, the PE, FE and BRK conditions are only reported when the associated character reaches the bottom of the RX_FIFO. An overrun error (OE) is reported as soon as it occurs.

*MIR, FIR Modes*

**LS_EV/TX_HLT_EV – Link Status/Transmitter Halted Event.**

Set to 1 when any of the following conditions occur:

1. Last byte of received frame reaches the bottom of the RX_FIFO
2. Receiver overrun
3. Transmitter underrun
4. Transmitted halted on frame end CEIR Mode

*Consumer_IR Mode*

**LS_EV/TXHLT_EV – Link Status/Transmitter Halted.**

Set to 1 when a receiver overrun or a transmitter underrun condition occurs.

**Note:** A high speed CPU can service the interrupt generated by the last frame byte reaching the RX_FIFO bottom before that byte is transferred to memory by the DMA controller. This can happen when the CPU interrupt latency is shorter than the RX_FIFO Time-out (Refer to the "FIFO Time-outs" section). A DMA request is generated only when the RX_FIFO level reaches the DMA threshold or when a FIFO time-out occurs, in order to minimize the performance degradation due to DMA signal handshake sequences. If the DMA controller must be set up before receiving each frame, the software in the interrupt routine should make sure that the last byte of the frame just received has been transferred to memory before re-initializing the DMA controller, otherwise that byte could appear as the first byte of the next received frame.

**B3** *UART Mode*

**MS_EV – Modem Status Event.**

Set to 1 when any of the bits 0 to 3 in the MSR register is set to 1.

*Any Infrared Mode*

**MS_EV/Unused – Modem Status Event.**

The function of this bit depends on the setting of the IRMSSL bit in the IRCR2 register.

| ISMSSL Value | Bit Function |
|---|---|
| 0 | Modem Status interrupt event |
| 1 | Forced to 0 |

**B4 DMA_EV – DMA Event.**

When an 8237 type DMA controller is used, this bit is set to 1 when a DMA terminal count (TC) is signaled. It is cleared upon read.

**B5** *UART, Sharp-IR, CEIR Modes*

T**XEMP_EV – Transmitter Empty.**

This bit is the same as bit 6 of the LSR register.

It is set to 1 when the transmitter is empty.

*MIR, FIR, SIR Modes*

**TXEMPEV/PLDEV – Transmitter Empty/Pipeline Load Event.**

Set to 1 when the transmitter is empty or a pipeline operation occurs.

**B6** *MIR, FIR Modes*

**SFIF_EV – ST_FIFO Event.**

Set to 1 when the ST_FIFO level is equal to or above the threshold, or an ST_FIFO time-out occurs. This bit is cleared when the CPU reads the ST_FIFO and its level drops below the threshold.

**B7 TMR_EV – Timer Event.**

Set to 1 when the timer reaches 0.

Cleared by writing 1 into bit 7 of the ASCR register.

### FCR – FIFO Control Register Write Only

Used to enable the FIFOs, clear the FIFOs and set the interrupt threshold levels.

Upon reset, all bits are set to 0.

**FIGURE 88. FIFO Control Register**

**B0 FIFO_EN – Enable FIFOs.**

When set to 1, both TX_FIFO and RX_FIFO are enabled.

In MIR, FIR and CEIR modes, the FIFOs are always enabled, and the setting of this bit is ignored.

**B1 RXSR – Receiver Soft Reset.**

Writing a 1 to this bit position generates a receiver soft reset, whereby the receiver logic as well as the RX_FIFO are both cleared.

This bit is automatically cleared by the hardware.

**B2 TXSR – Transmitter Soft Reset.**

Writing a 1 to this bit position generates a transmitter soft reset, whereby the transmitter logic as well as the TX_FIFO are both cleared.

This bit is automatically cleared by the hardware.

**B3 Reserved.**

Write 0.

**B5–4 TXFTH [1–0] – TX_FIFO Interrupt Threshold.**

In non-extended mode, these bits have no effect, regardless of the values written into them.

In extended mode, these bits select the TX_FIFO interrupt threshold level.

An interrupt is generated when the TX_FIFO level drops below the threshold.

**TABLE 76. TX_FIFO Level Selection**

| TXFTH (Bits 5-4) | TX_FIF0 Tresh. (16 Levels) | TX_FIF0 Tresh. (32 Levels) |
|---|---|---|
| 00(Default) | 1 | 1 |
| 01 | 3 | 7 |
| 10 | 9 | 17 |
| 11 | 13 | 25 |

**B7–6 RXFTH [1–0] – RX_FIFO Interrupt Threshold.**

These bits select the RX_FIFO interrupt threshold level.

An interrupt is generated when the RX_FIFO level is equal to or above the threshold.

**TABLE 77. RX_FIFO Level Selection**

| RXFTH (Bits 7-6) | RX_FIF0 Tresh. (16 Levels) | RX_FIF0 Tresh. (32 Levels) |
|---|---|---|
| 00(Default) | 1 | 1 |
| 01 | 4 | 8 |
| 10 | 8 | 16 |
| 11 | 14 | 26 |

## 5.14.4 LCR/BSR – Link Control/Bank Select Register

These registers share the same address.

The Link Control Register (LCR) is used to select the communications format for data transfers in UART, Sharp-IR and SIR modes.

The Bank select register (BSR) is used to select the register bank to be accessed next.

When the CPU performs a read cycle from this address location, the BSR content is returned. The content of LCR is returned when the CPU reads the SH_LCR register in bank 3.

During CPU write cycles, the setting of bit 7 (BKSE, bank select enable) determines the register to be accessed.

If bit 7 is 0, both LCR and BSR are written into. If bit 7 is 1, only BSR is written into, and LCR is not affected. This prevents the communications format from being spuriously affected when a bank other than bank 0 is accessed. Upon reset, all bits are set to 0.

### LCR – Link Control Register

The Format of LCR is shown in Figure 88.

Bits 0 to 6 are only effective in UART, Sharp-IR and SIR modes.

They are ignored in MIR, FIR and CEIR modes.

**FIGURE 88. Link Control Register**

**B1–0 WLS [1–0] – Character Length.**

These bits specify the length of each transmitted or received serial character.

**TABLE 78. Word Length Select Encoding**

| Bits 1-0 | Character Length |
|---|---|
| 00 | 5 Bits(Default) |
| 01 | 6 Bits |
| 10 | 7 Bits |
| 11 | 8 Bits |

**B2 STB – Stop Bits.**

Number of stop bits in each transmitted serial character. If this bit is 0, 1 stop bit is generated in the transmitted data. If it is 1 and a 5-bit character length is selected via bits 0 and 1, 1.5 stop bits are generated. If it is 1 and a 6, 7 or 8-bit character length is selected, 2 stop bits are generated. The receiver checks 1 stop bit only, regardless of the number of stop bits selected.

**B3 PEN – Parity Enable.**

When set to 1, parity bits are generated and checked by the transmitter and receiver channels respectively.

**B4 EPS – Even Parity.**

Used in conjunction with the STKP bit to determine the parity bit. See encodings below.

**B5 STKP – Stick Parity.**

The encodings of this and the previous two bits, for control of the parity bit, are as follows:

**TABLE 79. Bit Settings for Parity Control**

| PEN | EPS | STKP | Selected Parity |
|---|---|---|---|
| 0 | x | x | None |
| 1 | 0 | 0 | Odd |
| 1 | 1 | 0 | Even |
| 1 | 0 | 1 | Logic 1 |
| 1 | 1 | 1 | Logic 0 |

**B6 SBRK – Set Break.**

When set to 1, the following occurs:

— If UART mode is selected, the SOUT pin is forced to a logic 0 state.

— If SIR mode is selected, pulses are issued continuously on the IRTX pin.

— If Sharp-IR mode is selected and internal modulation is enabled, pulses are issued continuously on the IRTX pin.

— If Sharp-IR mode is selected and internal modulation is disabled, the IRTX pin is forced to a logic 1 state.

The break is disabled by setting this bit to 0. This bit acts only on the transmitter front-end and has no effect on the rest of the transmitter logic.

The following sequence should be followed to avoid transmission of erroneous characters because of the break.

1. Wait for the transmitter to be empty (TXEMP = 1).
2. Set SBRK to 1.
3. Wait for the transmitter to be empty, and clear SBRK when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

**B7 BKSE – Bank Select Enable.**

In the LCR register this bit is always 0.

### BSR – Bank Select Register

When bit 7 is 1, bits 0–6 of BSR are used to select the bank. The encodings are shown in Table 80.

**TABLE 80. Bank Selection Encoding**

| BSR Bits | | | | | | | | Bank Selected |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | x | x | x | x | x | x | x | 0 |
| 1 | 0 | x | x | x | x | x | x | 1 |
| 1 | 1 | x | x | x | x | 1 | x | 1 |
| 1 | 1 | x | x | x | x | x | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 2 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 3 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 4 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 5 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 6 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 7 |
| 1 | 1 | 1 | 1 | 1 | x | 0 | 0 | Reserved |
| 1 | 1 | 0 | x | x | x | 0 | 0 | Reserved |

## 5.14.5 MCR – Modem/Mode Control Register

Used to control the interface with the modem or data set, as well as the module operational mode. The function of this register changes depending upon whether the module is in extended or non-extended mode. In extended mode the interrupt output signal is always enabled and loopback can be selected by setting bit 4 of the EXCR1 register. Upon reset, all bits are set to 0.

### Non-Extended Mode

The format of the non-extended mode MCR is shown in Figure 88.

**FIGURE 88. Modem Control Register, Non-Extended Mode**

**B0 DTR – Data Terminal Ready.**

This bit controls the $\overline{DTR}$ signal output.

When it is set to 1, $\overline{DTR}$ is driven low.

In loopback mode this bit internally drives DSR.

**B1 RTS – Request to Send.**

This bit controls the $\overline{RTS}$ signal output.

When it is set to 1, $\overline{RTS}$ is driven low.

In loopback mode this bit internally drives CTS.

**B2 RILP – Loopback RI.**

In normal operation this bit is unused.

In loopback mode this bit internally drives RI.

**B3 ISEN/DCDL – Interrupt Signal Enable/Loopback DCD.**

In normal operation this bit controls the interrupt signal, and it must be set to 1 in order to enable it.

In loopback mode, this bit internally drives DCD, and the interrupt signal is always enabled.

**Note:** New programs should always keep this bit set to 1 during normal operation. The interrupt signal should be controlled through the Plug-n-Play logic.

**B4 LOOP – Loopback Enable.**

When set to 1, loopback mode is selected.

This bit accesses the same internal register as bit 4 of the EXCR1 register.

Refer to the section describing the EXCR1 register for more information on the loopback mode.

**B7–5 Reserved.**

Forced to 0.

### Extended Mode

The format of the extended mode MCR is shown in Figure 88.

**Note:** Bits 2 to 7 should always be initialized after the operational mode is changed from non-extended to extended.

**FIGURE 88. Modem Control Register, Extended Modes**

**B0 DTR – Data Terminal Ready.**

This bit controls the $\overline{DTR}$ signal output.

When it is set to 1, $\overline{DTR}$ is driven low.

In loopback mode this bit internally drives both DSR and RI.

**B1 RTS – Request to Send.**

This bit controls the $\overline{RTS}$ signal output.

When it is set to 1, $\overline{RTS}$ is driven low.

In loopback mode this bit internally drives both CTS and DCD.

**B2 DMA_EN – DMA Mode Enable.**

When set to 1, DMA mode of operation is enabled.

When data transfers are performed by a DMA controller, the transmit and/or receive data interrupts should be disabled to avoid spurious interrupts.

Note that DMA cycles always access the data holding registers or FIFOs, regardless of the selected bank.

**B3 TX_DFR – Transmit Deferral.**

When set to 1, transmit deferral is enabled.

Effective only when the TX_FIFO is enabled.

**B4 IR_PLS – Send Interaction Pulse.**

This bit is effective only in MIR and FIR Modes.

It is set to 1 by writing 1 into it.

Writing 0 into it has no effect.

When set to 1, a 2 µs infrared interaction pulse is transmitted at the end of the frame and the bit is automatically cleared by the hardware.

This bit is also cleared when the transmitter is soft reset.

The interaction pulse must be emitted at least once every 500 ms, as long as the high-speed connection lasts, in order to quiet slower (115.2 kbps or below) systems that might otherwise interfere with the link.

**B7–5 MDSL [2–0] – Mode Select.**

These bits are used to select the operational mode as shown in Table 81.

When the mode is changed, the transmitter and receiver are soft reset, and the modem status events are cleared.

**TABLE 81. The Module Operation Modes**

| MDSL2 (Bit 7) | MDSL1 (Bit 6) | MDSL0 (Bit 5) | Operational Mode |
|---|---|---|---|
| 0 | 0 | 0 | UART (Default) |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Sharp-IR |
| 0 | 1 | 1 | SIR |
| 1 | 0 | 0 | MIR |
| 1 | 0 | 1 | FIR |
| 1 | 1 | 0 | CEIR |
| 1 | 1 | 1 | Reserved |

## 5.14.6 LSR – Link Status Register

This register provides status information to the CPU concerning the data transfer.

Bits 1 through 4 (and 7 when in MIR or FIR mode) indicate link status events.

These bits are sticky, and accumulate any conditions occurred since the last time the register was read.

These bits are cleared when any of the following events occurs:

1. Hardware reset.
2. The receiver is soft reset.
3. The LSR register is read.

**Note:** This register is intended for read operations only. Writing to this register is not recommended as it may cause indeterminate results.

**FIGURE 88. Link Status Register**

**B0 RXDA – Receiver Data Available.**

Set to 1 when the Receiver Holding Register is full.

If the FIFOs are enabled, this bit is set when at least one character is in the RX_FIFO.

Cleared when the CPU reads all the data in the Holding Register or in the RX_FIFO.

**B1** ***UART, Sharp-IR, SIR, CEIR Modes***

**OE – Overrun Error.**

This bit is set to 1 as soon as an overrun condition is detected by the receiver.

Cleared upon read.

FIFOs Disabled: An overrun occurs when a new character is completely received into the receiver front-end section and the CPU has not yet read the previous character in the receiver holding register. The new character is discarded, and the receiver holding register is not affected.

FIFOs Enabled: An overrun occurs when a new character is completely received into the receiver front-end section and the RX_FIFO is full.

The new character is discarded, and the RX_FIFO is not affected.

*MIR, FIR Modes*

**OE – Overrun Error.**

An overrun occurs when a new character is completely received into the receiver front-end section and the RX_FIFO or the ST_FIFO is full.

The new character is discarded, and the RX_FIFO is not affected.

Cleared upon read.

**B2** *UART, Sharp-IR, SIR Modes*

**PE – Parity Error.**

This bit is set to 1 if the received character did not have the correct parity, as selected by the parity control bits in the LCR register.

If the FIFOs are enabled, the Parity Error condition will be associated with the particular character in the RX_FIFO it applies to.

In which case, the PE bit is set when the character reaches the bottom of the RX_FIFO.

Cleared upon read.

*MIR, FIR Modes*

**BAD_CRC – CRC Error.**

Set to 1 when a mismatch between the received CRC and the receiver-generated CRC is detected, and the last byte of the received frame has reached the bottom of the RX_FIFO.

Cleared upon read.

**B3** *UART, Sharp-IR, SIR Modes*

**FE – Framing Error.**

This bit indicates that the received character did not have a valid stop bit.

It is set to 1 when the stop bit is detected as a logic 0.

If the FIFOs are enabled, the Framing Error condition will be associated with the particular character in the RX_FIFO it applies to.

In which case, the FE bit is set when the character reaches the bottom of the RX_FIFO.

After a Framing Error is detected, the receiver will try to resynchronize.

If the bit following the stop bit position is 0, the receiver assumes it to be a valid start bit and the next character is shifted in.

If that bit is 1, the receiver will enter the idle state looking for the next start bit.

Cleared upon read.

*MIR Mode*

**PHY_ERR – Physical Layer Error.**

Set to 1 when an abort condition is detected during the reception of a frame, and the last byte of the frame has reached the bottom of the RX_FIFO.

Cleared upon read.

*FIR Mode*

**PHY_ERR – Physical Layer Error.**

Set to 1 when an encoding error or the sequence BOF-data-BOF is detected (missing EOF) during the reception of a frame, and the last byte of the frame has reached the bottom of the RX_FIFO.

Cleared upon read.

**B4** *UART, Sharp-IR, SIR Modes*

**BRK – Break Event Detected.**

Set to 1 when a sequence of logic 0 bits, equal or longer than a full character transmission, is received.

If the FIFOs are enabled, the Break condition will be associated with the particular character in the RX_FIFO it applies to.

In which case, the BRK bit is set when the character reaches the bottom of the RX_FIFO. When a Break occurs only one zero character is transferred to the receiver holding register or to the RX_FIFO.

The next character transfer takes place after at least one logic 1 bit is received followed by a valid start bit. Cleared upon read.

*MIR, FIR Modes*

**MAX_LEN – Maximum Length.**

Set to 1 when a frame exceeding the maximum length has been received, and the last byte of the frame has reached the bottom of the RX_FIFO.

Cleared upon read.

**B5 TXRDY – Transmitter Ready.**

This bit is set to 1 when the Transmitter Holding Register or the TX_FIFO is empty.

It is cleared when a data character is written to the TXD port.

**B6 TXEMP – Transmitter Empty.**

Set to 1 when the Transmitter is empty. The transmitter empty condition occurs when the Holding Register or the TX_FIFO is empty, and the transmitter front-end is idle.

**B7** *UART, Sharp-IR, SIR Modes*

**ER_INF – Error in RX_FIFO.**

Set to 1 when at least one character with a PE, FE or BRK condition is in the RX_FIFO.

This bit is always 0 in 16450 mode.

*MIR, FIR Modes*

**FR_END – Frame End.**

Set to 1 when the last byte (Frame End Byte) of a received frame reaches the bottom of the RX_FIFO.

Cleared upon read.

### 5.14.7 MSR – Modem Status Register

The function of this register depends on the selected operational mode. When UART Mode is selected, this register provides the current-state as well as state-change information of the status lines from the MODEM or Data Set. When any one of the Infrared Modes is selected, the register function is controlled by the setting of the IRMSSL bit in the IRCR2 register. If IRMSSL is 0, the MSR register works the same as in UART mode. If IRMSSL is 1, the MSR register returns the value 30h, regardless of the state of the MODEM input lines.

In Loopback mode, the MSR register works similarly except that its status inputs are internally driven by appropriate bits in the MCR register since the MODEM input lines are internally disconnected. Refer to the sections describing the MCR and EXCR1 register for more information.

A description of the various bits of MSR, with Loopback disabled and UART Mode selected, is provided below. When any of the bits 0 to 3 is set to 1, a Modem Status Interrupt is generated. Bits 0 to 3 are set to 0 when any of the following events occurs.

1. Hardware reset.
2. The MSR register is read.
3. The operational mode is changed and the IRMSSL bit is 0.

**Note:** The modem status lines have no effect on transmitter and receiver operation. They can be used as general purpose inputs.

**FIGURE 88. Modem Status Register**

**B0 DCTS – Delta Clear to Send.**
Set to 1 when the $\overline{CTS}$ input changes state. Cleared upon read.

**B1 DDSR – Delta Data Set Ready.**
Set to 1 when the $\overline{DSR}$ input changes state. Cleared upon read.

**B2 TERI – Ring Indicator Trailing Edge.**
Set to 1 when the $\overline{RI}$ input changes from a low state to a high state. Cleared upon read.

**B3 DDCD – Delta Data Carrier Detect.**
Set to 1 when the $\overline{DCD}$ input changes state. Cleared upon read.

**B4 CTS – Clear to Send.**
This bit returns the complement of the $\overline{CTS}$ input.

**B5 DSR – Data Set Ready.**
This bit returns the complement of the $\overline{DSR}$ input.

**B6 RI – Ring Indicator.**
This bit returns the complement of the $\overline{RI}$ input.

**B7 DCD – Data Carrier Detect.**
This bit returns the complement of the $\overline{DCD}$ input.

### 5.14.8 SPR/ASCR – Scratchpad/Auxiliary Status and Control Register

These registers share the same address.

**SPR**–Scratchpad Register.

This register is accessed when the module is in non-extended mode.

It does not control the module in any way, and is intended to be used by the programmer to hold data temporarily.

**ASCR**–Auxiliary Status and Control Register.

This register is accessed when the extended mode of operation is selected.

All the ASCR bits are cleared when a hardware reset occurs or when the operational mode changes.

Bits 2 and 6 are cleared when the transmitter is soft reset.

Bits 0, 1, 4 and 5 are cleared when the receiver is soft reset.

The format of ASCR is shown in Figure 88.

**FIGURE 88. Auxillary Status and Control Register**

**B0 RXF_TOUT – RX_FIFO Time-out.**
This bit is read-only, and is set to 1 when an RX_FIFO Time-out occurs.

In MIR or FIR modes this bit can be used in conjunction with bit 1 to determine whether a number of bytes, as determined by the RX_FIFO threshold, can be read without checking the RXDA bit in the LSR register for each byte. Cleared when a character is read from the RX_FIFO.

**B1** *MIR, FIR Modes*

**FEND_INF – Frame End Bytes in RX_FIFO.**

This bit is read-only, and is set to 1 when one or more Frame End bytes are in the RX_FIFO.

Cleared when no Frame End byte is in the RX_FIFO.

**B2** *MIR, FIR Modes*

**S_EOT – Set End of Transmission.**

When a 1 is written into this bit position before writing the last character into the TX_FIFO, frame transmission is completed and a CRC + EOF is sent. This bit can be used as an alternative to the Transmitter Frame Length register. If this method is to be used, the FEND_MD bit in the IRCR2 register should be set to 1, or the Transmitter Frame Length register should be set to maximum count.

This bit is automatically cleared by the hardware when a character is written into the TX_FIFO.

*CEIR Mode*

**S_EOT – Set End of Transmission.**

When a 1 is written into this bit position before writing the last character into the TX_FIFO, data transmission is gracefully completed. If the CPU simply stops writing data into the TX_FIFO at the end of the data stream, a transmitter underrun is generated and the transmitter stops. In this case, this is not an error, however the software needs to clear the underrun before the next transmission can occur.

This bit is automatically cleared by the hardware when a character is written into the TX_FIFO.

**B3** *MIR, FIR Modes*

**TXHFE – Transmitter Halted on Frame End.**

This bit is used only when the transmitter frame-end stop mode is selected (TX_MS bit in IRCR2 set to 1). It is set to 1 by the hardware when transmission of a frame is complete and the end-of-frame condition was generated by the TFRCC counter reaching 0.

This bit must be cleared, by writing 1 into it, to re-enable transmission.

**B4** *MIR, FIR Modes*

**LOST_FR – Lost Frame Flag.**

This bit is read-only, and reflects the setting of the lost-frame indicator flag at the bottom of the ST_FIFO.

*CEIR Mode*

**RXWDG – Receiver Watch Dog.**

Set to 1 each time an infrared pulse or pulse-train is detected by the receiver.

Can be used by the software to detect a receiver idle condition.

Cleared upon read.

**B5** *MIR, FIR Modes*

**RXBSY – Receiver Busy.**

This bit is read-only, and returns a 1 when reception of a frame is in progress.

*CEIR Mode*

**RXACT – Receiver Active.**

Set to 1 when an infrared pulse or pulse-train is received. If a 1 is written into this bit position, the bit is cleared and the receiver is deactivated. When this bit is set, the receiver samples the infrared input continuously at the programmed baud rate and transfers the data to the RX_FIFO.

**B6** *MIR, FIR, CEIR Modes*

**TXUR – Transmitter Underrun.**

This bit is set to 1 when a transmitter underrun occurs.

It is always cleared when a mode other than MIR, FIR or CEIR is selected.

This bit must be cleared, by writing 1 into it, to re-enable transmission.

**B7** *UART, Sharp-IR, CEIR Modes*

**CTE - Clear Timer Event**

Writing 1 into this bit position clears the TMR_EV bit in the EIR register. Writing 0 into it has no effect.

*MIR, FIR, SIR Modes*

**PLD/CTE – Pipeline Load Status/Clear Timer Event.**

Reading this bit returns the pipeline load status. It is set to 1 by the hardware when a pipeline load operation occurs. It is cleared upon read.

Writing 1 into this bit position clears the TMREV bit in the EIR register. Writing 0 into it has no effect. The write operation has no effect on the Pipeline Load Status.

## 5.15 BANK 1

**TABLE 82. Bank 1 Register Set**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | LBGD(L) | Legacy Baud Generator Divisor Port (Low Byte) |
| 01h | LBGD(H) | Legacy Baud Generator Divisor Port (High Byte) |
| 02h | | Reserved |
| 03h | LCR/ BSR | Link Control / Bank Select Register |
| 04h - 07h | | Reserved |

### 5.15.1 LBGD – Legacy Baud Generator Divisor Port

This port provides an alternate data path to the baud generator divisor register. It is implemented for compatibility with the 16550 and to support existing legacy software packages. New software should use the BGD port in bank 2 to access the baud generator devisor register. Like the BGD port, LBGD is 16 bits wide and is split into two 8-bit parts, LBGD(L) and LBGD(H), occupying consecutive address locations. A CPU read or write access of the divisor register, through either LBGD(L) or LBGD(H), will affect the module operational mode as follows.

If the module is in extended mode, the module is switched back to 16550 compatibility mode.

In addition to the EXT_SL bit, the following bits are also cleared.

1. Bits 2 to 7 of extended-mode MCR.
2. Bit 5 and 7 of EXCR1.
3. Bits 0 to 5 of EXCR2.
4. Bits 2 and 3 of IRCR1.

If the module is in non-extended mode and the LOCK bit is 0, the following bits will be cleared.

1. Bits 5 and 7 of EXCR1.
2. Bits 0 to 5 of EXCR2.

If the module is in non-extended mode and the LOCK bit is 1, the content of the divisor register will not be affected and no other action is taken.

### 5.15.2 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

## 5.16 BANK 2

**TABLE 83. Bank 2 Register Set**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | BGD(L) | Baud Generator Divisor Port (Low byte) |
| 01h | BGD(H) | Baud Generator Divisor Port (High byte) |
| 02h | EXCR1 | Extended Control Register 1 |
| 03h | LCR/BSR | Link Control/ Bank Select Register |
| 04h | EXCR2 | Extended Control Register 2 |
| 05h | | Reserved |
| 06h | TXFLV | TX_FIFO Level |
| 07h | RXFLV | RX_FIFO Level |

### 5.16.1 BGD – Baud Generator Divisor Port

This port provides the data path to the baud generator divisor register that holds the reload value for the baud generator counter. Divisor values from 1 to $2^{16}$ –1 can be used. See Table 84. The zero value is reserved and must not be used. The programmed value must be such that the baud generator output clock frequency is sixteen times the desired baud rate value. The baud generator divisor register is 16 bits wide and is split into two independently accessible 8-bit parts. Correspondingly, the BGD port is also 16 bits wide and is split into two 8-bit parts, occupying consecutive address locations. BGD(L) is located at the lower address and accesses the least significant part of the baud generator divisor register, whereas BGD(H) is located at the higher address and accesses the most significant part. The baud generator divisor register must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either part of it, the baud generator counter is immediately loaded.

After reset, the content of the baud generator divisor register is indeterminate.

**TABLE 84. Baud Generator Divisor Settings**

| Prescaler Value | 13 | | 1.625 | | 1 | |
|---|---|---|---|---|---|---|
| **Baud Rate** | **Divisor** | **% Error** | **Divisor** | **% Error** | **Divisor** | **% Error** |
| 50 | 2304 | 0.16% | 18461 | 0.00% | 30000 | 0.00% |
| 75 | 1536 | 0.16% | 12307 | 0.01% | 20000 | 0.00% |
| 110 | 1047 | 0.19% | 8391 | 0.01% | 13636 | 0.00% |
| 134.5 | 857 | 0.10% | 6863 | 0.00% | 11150 | 0.02% |
| 150 | 768 | 0.16% | 6153 | 0.01% | 10000 | 0.00% |
| 300 | 384 | 0.16% | 3076 | 0.03% | 5000 | 0.00% |
| 600 | 192 | 0.16% | 1538 | 0.03% | 2500 | 0.00% |
| 1200 | 96 | 0.16% | 769 | 0.03% | 1250 | 0.00% |
| 1800 | 64 | 0.16% | 512 | 0.16% | 833 | 0.04% |
| 2000 | 58 | 0.53% | 461 | 0.12% | 750 | 0.00% |
| 2400 | 48 | 0.16% | 384 | 0.16% | 625 | 0.00% |
| 3600 | 32 | 0.16% | 256 | 0.16% | 416 | 0.16% |
| 4800 | 24 | 0.16% | 192 | 0.16% | 312 | 0.16% |
| 7200 | 16 | 0.16% | 128 | 0.16% | 208 | 0.16% |
| 9600 | 12 | 0.16% | 96 | 0.16% | 156 | 0.16% |
| 14400 | 8 | 0.16% | 64 | 0.16% | 104 | 0.16% |
| 19200 | 6 | 0.16% | 48 | 0.16% | 78 | 0.16% |
| 28800 | 4 | 0.16% | 32 | 0.16% | 52 | 0.16% |
| 38400 | 3 | 0.16% | 24 | 0.16% | 39 | 0.16% |
| 57600 | 2 | 0.16% | 16 | 0.16% | 26 | 0.16% |
| 115200 | 1 | 0.16% | 8 | 0.16% | 13 | 0.16% |
| 230400 | --- | --- | 4 | 0.16% | --- | --- |
| 460800 | --- | --- | 2 | 0.16% | --- | --- |
| 750000 | --- | --- | --- | --- | 2 | 0.00% |
| 921600 | --- | --- | 1 | 0.16% | --- | --- |
| 1500000 | --- | --- | --- | --- | 1 | 0.00% |

### 5.16.2 EXCR1 – Extended Control Register 1

Used to control the extended mode of operation.

Upon reset all bits are set to 0.

**FIGURE 88. Extended Control Register 1**

**B0 EXTSL – Extended Mode Select.**

When set to 1, extended mode is selected.

**B1 DMANF – DMA Fairness Control.**

This bit controls the maximum duration of DMA burst transfers.

0 → DMA requests are forced inactive after approximately 10.5 µs of continuous transmitter and/or receiver DMA operation.

1 → A TXDMA request is deactivated when the TX_FIFO is full.

An RX_DMA request is deactivated when the RX_FIFO is empty.

**B2 DMATH – DMA Threshold Levels Select.**

This bit selects the TX_FIFO and RX_FIFO threshold levels used by the DMA request logic to support demand transfer mode.

A TX_DMA request is generated when the TX_FIFO level is below the threshold.

An RXDMA request is generated when the RX_FIFO level reaches the threshold or when an RX_FIFO time-out occurs.

| Bit Value | RX_FIFO DMA Thrsh. | TX_FIFO DMA Thresh. (16-Levels) | TX_FIFO DMA Thresh. (32-Levels) |
|---|---|---|---|
| 0 | 4 | 13 | 29 |
| 1 | 10 | 7 | 23 |

**B3 DMASWP – DMA Swap.**

This bit selects the routing of the DMA control signals between the internal DMA logic and the configuration module. When this bit is 0, the transmitter and receiver DMA control signals are not swapped. When it is 1, they are swapped. A block diagram illustrating the control signals routing is given in Table 88.

The swap feature is particularly useful when only one 8237 DMA channel is used to serve both transmitter and receiver. In this case only one external DRQ/$\overline{\text{DACK}}$ signal pair will be interconnected to the swap logic by the configuration module. Routing the external DMA channel to either the transmitter or the receiver DMA logic is then simply controlled by the DMASWP bit. This way, the infrared module drivers do not need to know the details of the configuration module.

**B4 LOOP – Loopback Enable.**

When set to 1, loopback mode is selected. This bit accesses the same internal register as bit 4 in the MCR register, when the module is in non-extended mode.

Loopback mode behaves similarly in both non-extended and extended modes.

When extended mode is selected, the DTR bit in the MCR register internally drives both $\overline{\text{DSR}}$ and $\overline{\text{RI}}$, and the $\overline{\text{RTS}}$ bit drives $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$.

During loopback the following occur:

1. The transmitter and receiver interrupts are fully operational. The modem status interrupts are also fully operational, but the interrupts' sources are now the lower bits of the MCR register. Modem interrupts in infrared modes are disabled unless the IRMSSL bit in the IRCR2 register is 0. Individual interrupts are still controlled by the IER register bits.
2. The DMA control signals are fully operational.
3. UART and infrared receiver serial input pins are disconnected. The internal receiver serial inputs are connected to the corresponding internal transmitter serial outputs.
4. The UART transmitter serial output pin is forced high and the infrared transmitter serial output pin is forced low, unless the ETDLBK bit is set to 1. In which case they will function normally.
5. The modem status input pins ($\overline{\text{DSR}}$, $\overline{\text{CTS}}$, $\overline{\text{RI}}$ and $\overline{\text{DCD}}$) are disconnected. The internal modem status signals, are driven by the lower bits of the MCR register.

**B5 ETDLBK – Enable Transmitter Output During Loopback.**

When set to 1, the transmitter serial output is enabled and functions normally when loopback is selected.

**B6 Reserved.**

Write 1.

**B7 BTEST – Baud Generator Test.**

When set to 1, the output of the baud generator is routed to the DTR pin.

**FIGURE 88. DMA Control Signals Routing**

### 5.16.3 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

### 5.16.4 EXCR2 – Extended Control Register 2

This register is used to configure the transmitter and receiver FIFOs, and the baud generator prescaler.

Upon reset all bits are set to 0.

**FIGURE 88. Extended Control Register 2**

**B1–0** TF_SIZ [1–0] – TX_FIFO Levels Select.

These bits select the number of levels for the TX_FIFO.

They are effective only when the FIFOs are enabled.

| Bits 1–0 | TXFIFO Levels |
|---|---|
| 00 | 16 |
| 01 | 32 |
| 1x | Reserved |

**B3–2** RF_SIZ [1–0] – RX_FIFO Levels Select.

These bits select the number of levels for the RX_FIFO.

They are effective only when the FIFOs are enabled.

| Bits 3–2 | RX_FIFO Levels |
|---|---|
| 00 | 16 |
| 01 | 32 |
| 1x | Reserved |

**B5–4** PRESL [1–0] – Prescaler Select.

The prescaler divides the 24 MHz input clock frequency to provide the clock for the baud generator.

| Bits 5–4 | Prescaler Value |
|---|---|
| 00 | 13.0 |
| 01 | 1.625 |
| 10 | Reserved |
| 11 | 1.0 |

**B6** Reserved.

Read/write 0.

**B7** LOCK – Lock Bit.

When set to 1, accesses to the baud generator divisor register through LBGD(L) and LBGD(H) as well as fallback are disabled from non-extended mode.

In this case two scratchpad registers overlayed with LBGD(L) and LBGD(H) are enabled, and any attempted CPU access of the baud generator divisor register through LBGD(L) and LBGD(H) will access the scratchpad registers instead. This bit must be set to 0 when extended mode is selected.

### 5.16.5 TXFLV – TX_FIFO Level, Read-Only

This register returns the number of bytes in the TX_FIFO. It can be used for software debugging, or during recovery from a transmitter underrun condition in one of the high-speed infrared modes.

**FIGURE 88. Transmit FIFO Level**

**B5–0 TFL [5–0] – Number of bytes in TX_FIFO.**
**B7–6 Reserved.**
Return 0's.

### 5.16.6 RXFLV – RX_FIFO Level, Read-Only

This register returns the number of bytes in the RX_FIFO. It can be used for software debugging.

**FIGURE 88. Receive FIFO Level**

**B5–0 RFL [5–0] – Number of bytes in RX_FIFO.**
**B7–6 Reserved.**
Return 0's.

**Note:** The contents of TXFLV and RXFLV are not frozen during CPU reads. Therefore, invalid data could be returned if the CPU reads these registers during normal transmitter and receiver operation. To obtain correct data, the software should perform three consecutive reads and then take the data from the second read, if first and second read yield the same result, or from the third read, if first and second read yield different results.

## 5.17 BANK 3

**TABLE 85. Bank 3 Register Set**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | MRID | Module Identification Register |
| 01h | SH_LCR | Shadow of LCR Register (Read Only) |
| 02h | SH_FCR | Shadow of FIFO Control Register (Read Only) |
| 03h | LCR/ BSR | Link Control Register/ Bank Select Registers |
| 04h-07h | Reserved | |

### 5.17.1 MID – Module Identification Register, Read Only

When read, it returns the module revision.

The returned value is 2Xh.

### 5.17.2 SH_LCR – Link Control Register Shadow, Read Only

This register returns the value of the LCR register.

The LCR register is written into when a byte value with bit 7 set to 0 is written to the LCR/BSR registers location (at offset 3) from any bank.

### 5.17.3 SH_FCR – FIFO Control Register Shadow, Read-Only

This register returns the value written into the FCR register in bank 0.

### 5.17.4 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

## 5.18 BANK 4

**TABLE 86. Bank 4 Register Set**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | TMR(L) | Timer Register (Low Byte) |
| 01h | TMR(H) | Timer Register (High Byte) |
| 02h | IRCR1 | Infrared Control Register 1 |
| 03h | LCR/ BSR | Link Control/ Bank Select Registers |
| 04h | TFRL(L)/ TFRCC(L) | Transmit Frame Length/ Current Count (Low Byte) |
| 05h | TFRL(H)/ TFRCC(H) | Transmit Frame Length/ Current Count (High Byte) |
| 06h | RFRML(L)/ RFRCC(L) | Receive Frame Maximum Length/ Current Count (Low Byte) |
| 07h | RFRML(H)/ RFRCC(H) | Receive Frame Maximum Length/ Current Count (High Byte) |

### 5.18.1 TMR – Timer Register

This register is used to program the reload value for the internal down-counter as well as to read the current counter value. TMR is 12 bits wide and is split into two independently accessible parts occupying consecutive address locations. TMR(L) is located at the lower address and accesses the least significant 8 bits, whereas TMR(H) is located at the higher address and accesses the most significant 4 bits. Values from 1 to $2^{12}$ –1 can be used. The zero value is reserved and must not be used. The upper 4 bits of TMR(H) are reserved and must be written with 0's. The timer resolution is 125 µs, providing a maximum time-out interval of approximately 0.5 seconds. To properly program the timer, the CPU must always write the lower value into TMR(L) first, and then the upper value into TMR(H). Writing into TMR(H) causes the counter to be loaded. A read of TMR returns the current counter value if the CTEST bit is 0, or the programmed reload value if CTEST is 1. In order for a read access to return an accurate value, the CPU should always read TMR(L) first, and then TMR(H). This is because a read of TMR(H) returns the content of an internal latch that is loaded with the 4 most significant bits of the current counter value when TMR(L) is read. After reset, the content of this register is indeterminate.

### 5.18.2 IRCR1 – Infrared Control Register 1

Used to control the timer and counters as well as enable the Sharp-IR or SIR infrared mode in the non-extended mode of operation.

Upon reset, all bits are set to 0.

.

**FIGURE 88. Infrared Control Register 1**

**B0 TMR_EN – Timer Enable, Extended Mode Only.**

When this bit is 1, the timer is enabled.

When it is 0, the timer is frozen.

**B1 CTEST – Counters Test.**

When this bit is set to 1, the TMR register reload value, as well as the TFRL and RFRML register contents are returned during CPU reads.

**B3–2 IR_SL [1–0] – SIR or Sharp-IR Select, Non-Extended Mode Only.**

These bits are used to select the appropriate infrared mode when the module is in non-extended mode.

They are ignored when extended mode is selected.

| Bits 3-2 | Selected Mode |
|---|---|
| 00 | UART |
| 01 | Reserved |
| 10 | Sharp-IR |
| 11 | SIR |

**B7–4 Reserved**.

Write as 0's.

### 5.18.3 LCR/BSR – Link Control/Bank Select Registers

These Registers are the same as in bank 0.

### 5.18.4 TFRL/TFRCC – Transmitter Frame-Length/Current-Count

These registers share the same addresses. TFRL is always accessed during write cycles and is used to program the frame length, in bytes, for the frames to be transmitted. The frame length value does not include any appended CRC bytes. TFRL is accessed during read cycles if the CTEST bit is set to 1, and returns the previously programmed value. Values from 1 to $2^{13}$ –1 can be used. The zero value is reserved and must not be used. TFRCC is loaded with the content of TFRL when transmission of a frame begins, and decrements after each byte is transmitted. It is read-only and is accessed during CPU read cycles when the CTEST bit is 0. It returns the number of currently remaining bytes of the frame being transmitted. These registers are 13 bits wide and are split into two independently accessible parts occupying consecutive address locations. TFRL(L) and TFRCC(L) are located at the lower address and access the least significant 8 bits, whereas TFRL(H) and TFRCC(H) are located at the higher address and access the most significant 5 bits. To properly program TFRL, the CPU must always write the lower value into TFRL(L) first, and then the upper value into TFRL (H). The upper 3 bits of TFRL(H) are reserved and must be written with 0's. In order for a read access of TFRCC to return an accurate value, the CPU should always read TFRCC(L) first, and then TFRCC(H). After reset, the content of the TFRL register is 800h.

### 5.18.5 RFRML/RFRCC – Receiver Frame Maximum-Length/Current-Count

These registers share the same addresses. RFRML is always accessed during write cycles and is used to program the maximum frame length, in bytes, for the frames to be received. The maximum frame length value includes the CRC bytes. RFRML is accessed during read cycles if the CTEST bit is set to 1, and returns the previously programmed value.

Values from 4 to $2^{13}$ –1 can be used. The values from 0 to 3 are reserved and must not be used. RFRCC holds the current byte count of the incoming frame, and increments after each byte is received. It is read-only and is accessed during CPU read cycles when the CTEST bit is 0. These registers are 13 bits wide and are split into two independently accessible parts occupying consecutive address locations. RFRML(L) and RFRCC(L) are located at the lower address and access the least significant 8 bits, whereas RFRML(H) and RFRCC(H) are located at the higher address and access the most significant 5 bits. To properly program RFRML, the CPU must always write the lower value into RFRML(L) first, and then the upper value into RFRML(H). The upper 3 bits of RFRML(H) are reserved and must be written with 0's. In order for a read access of RFRCC to return an accurate value, the CPU should always read RFRCC(L) first, and then RFRCC(H). After reset, the content of the RFRML register is 800h.

**Note:** TFRCC and RFRCC are intended for testing purposes only. Use of these registers for any other purpose is not recommended.

## 5.19 BANK 5

**TABLE 87. Bank 5 Register**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | P_BGD(L) | Pipelined Baud Generator Divisor Set Register |
| 01h | P_BGD(H) | Pipelined Baud Generator Divisor Set Register |
| 02h | P_MDR | Pipeline Mode Register |
| 03h | LCR/ BSR | Link Control/ Bank Select Registers |
| 04h | IRCR2 | Infrared Control Register 2 |
| 05h | FRM_ST | Frame Status |
| 06h | RFRL(L)/ LSTFRC | Received Frame Length (Low Byte)/Lost Frame Count |
| 07h | RFRL(H) | Received Frame Length (High Byte) |

### 5.19.1 P_BGD – Pipelined Baud Generator Divisor Register

This register holds the value that determines the new baud rate following a pipeline operation. It is a 16-bit wide register and is split into two 8-bit parts, P_BGD(L) and P_BGD(H), occupying consecutive address locations. The value written into these registers will be loaded into the least and most significant parts of the baud generator divisor register when the transmitter becomes empty and both the MD_PEN and BR_PEN bits in the P_MDR register are set to 1. Upon reset, the content of this register is indeterminate.

### 5.19.2 P_MDR – Pipelined Mode Register

This register can be read or written in any mode. However, a pipeline operation will only take place if the presently selected mode and the target mode are both IrDA modes.

Furthermore, SIR must be selected in extended mode and the TX_FIFO1 must be enabled.

When a pipeline operation takes place, the following occurs:

1. If the target mode is MIR or FIR, the transmitter is halted for 250 s.
2. If the target mode is SIR, the transmitter is halted for 250 µs or a character time (at the newly selected baud rate), whichever is greater.
3. Bits 7, 6, 5 and 2 will be loaded into the corresponding bit positions in the MCR register in bank 0, bit 3 will be loaded into bit position 3 of EXCR1.

Upon reset, all bits are set to 0.

**FIGURE 88. Pipelined Mode Register**

**B0 MD_PEN – Mode Bits Pipelining Enable.**
When this bit is set to 1 and the transmitter becomes empty, a pipeline load operation takes place.
This bit is automatically cleared after the load has occurred.

**B1 BR_PEN – Baud Rate Pipelining Enable.**
This bit is effective only when the MDPEN bit is set to 1.
When it is set to 1 and a pipeline load operation takes place, the PBGD register will be loaded into the baud generator divisor register.

**B2 P_DMA_EN – Pipelined DMA Enable Bit**

**B3 P_DMASWP – Pipelined DMA Swap Bit**

**B4 Reserved.**
Write 0.

**B7–5 P_MDSL [2–0] – Pipelined Mode Select Bits**

### 5.19.3 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

### 5.19.4 IRCR2 – Infrared Control Register 2

Upon reset, the content of this register is 02h.

**FIGURE 88. IInfrared Control Register 2**

**B0 IR_FDPLX – Infrared Full Duplex Mode.**
When set to 1, the infrared receiver is not masked during transmission.

**B1 IRMSSL – MSR Register Function Select in Infrared Mode.**
This bit selects the behavior of the modem status register/interrupt when any infrared mode is selected. When UART mode is selected, the modem status register and interrupt function normally, and this bit is ignored.
0 → MSR register and modem status interrupt work as in UART mode.
1 → MSR register returns 30h and the modem status interrupt is disabled.

**B2 MDRS – MIR Data Rate Select.**
This bit determines the data rate in MIR mode.
0 → 1.152 Mbps
1 → 0.576 Mbps

**B3 TX_MS – Transmitter Mode Select.**
This bit is used in MIR and FIR modes only. When it is set to 1, transmitter frame-end stop mode is selected. In this case the transmitter stops after transmission of a frame is complete, if the end-of-frame condition was generated by the TFRCC counter reaching 0. The transmitter can be restarted by clearing the TXHFE bit in the ASCR register.

**B4 AUX_IRRX – Auxiliary Infrared Input Select.**
When set to 1, the infrared signal is received from the auxiliary input. See Table 97.

**B5 FEND_MD – Frame End Control.**
This bit selects whether a terminal-count condition from the
TFRCC register will generate an EOF in PIO mode or DMA mode.
0 → TFRCC terminal count effective in PIO mode.

1 → TFRCC terminal count effective in DMA mode.

**B6 SFTSL – ST_FIFO Threshold Select.**

An interrupt request is generated when the ST_FIFO level reaches the threshold or when an ST_FIFO time-out occurs.

| Bit Value | Threshold Level |
|---|---|
| 0 | 2 |
| 1 | 4 |

**B7 Reserved.**

Read/write 0.

### 5.19.5 ST_FIFO – Status FIFO

The ST_FIFO is used in MIR and FIR Modes.

It is an 8-level FIFO and is intended to support back-to-back incoming frames in DMA mode, when an 8237-type DMA controller is used. Each ST_FIFO entry contains either status information and frame length for a single frame, or the number of lost frames.

The bottom entry spans three address locations, and is accessed via the FRMST, RFRL(L)/LSTFRC and RFRL(H) registers. The ST_FIFO is flushed when

a hardware reset occurs or when the receiver is soft reset.

**Note:** The status and length information of received frames is loaded into the ST_FIFO whenever the DMA_EN bit in the extended-mode MCR register is set to 1 and an 8237 type DMA controller is used, regardless of whether the CPU or the DMA controller is transferring the data from the RX_FIFO to memory. This implies that, during testing, if full duplex is enabled and a DMA channel is servicing the transmitter while the CPU is servicing the receiver, the CPU must still read the ST_FIFO. Otherwise, it fills up and incoming frames will be rejected.

#### FRMST – Frame Status Byte at ST_FIFO Bottom, Read-Only

This register returns the status byte at the bottom of the ST_FIFO. If the LOSTFR bit is 0, bits 0 to 4 indicate if any error condition occurred during reception of the corresponding frame. Error conditions will also affect the error flags in the LSR register.

**FIGURE 88. Frame Status Byte Register**

**B0 OVR2 – Overrun Error 2.**

This bit is set to 1 when incoming characters or entire frames have been discarded due to the ST_FIFO being full.

**B1 OVR1 – Overrun Error 1.**

This bit is set to 1 when incoming characters or entire frames have been discarded due to the RX_FIFO being full.

**B2 BAD_CRC – CRC Error.**

Set to 1 when a mismatch between the received CRC and the receiver-generated CRC is detected.

**B3 PHY_ERR – Physical Layer Error.**

Set to 1 when an encoding error or the sequence BOF-data-BOF is detected in FIR mode, or an abort condition is detected in MIR mode.

**B4 MAX_LEN – Maximum Frame Length Exceeded.**

Set to 1 when a frame exceeding the maximum length has been received.

**B5 Reserved.**

Returned data is indeterminate.

**B6 LOST_FR – Lost Frame Indicator Flag.**

Indicates the type of information provided by this ST_FIFO entry.

0 → Entry provides status information and length for a received frame.

1 → Entry provides overrun indications and number of lost frames.

**B7 VLD – ST_FIFO Entry Valid.**

When set to 1, the bottom ST_FIFO entry contains valid data.

#### RFRL(L)/LSTFRC – Received Frame Length /Lost-Frame-Count at ST_FIFO Bottom, Read-Only

This register should be read only when the VLD bit in FRMST is 1. The information returned depends on the setting of the LOST_FR bit. Upon reset, all bits are set to 0.

LOST_FR = 0 Least significant 8 bits of the received frame length.

LOST_FR = 1 Number of lost frames

### RFRL(H) – Received-Frame-Length at ST_FIFO Bottom, Read-Only

This register should be read only when the VLD bit in FRMST is 1. The information returned depends on the setting of the LOST_FR bit. Upon reset, all bits are set to 0.

LOST_FR = 0 Most significant 5 bits of the received frame length.

LOST_FR = 1 All 0's Reading this register removes the bottom ST_FIFO entry.

## 5.20 BANK 6

**TABLE 88. Bank 6 Register Set**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | IRCR3 | Infrared Control Register 3 |
| 01h | MIR_PW | MIR Pulse Width |
| 02h | SIR_PW | SIR Pulse Width Register |
| 03h | LCR/ BSR | Link Control/ Bank Select Register |
| 04h | BFPL | Beginning Flags/ Preamble Length Register |
| 05h - 07h | Reserved | |

### 5.20.1 IRCR3 – Infrared Control Register 3

Used to select the operating mode of the infrared interface.

Upon reset, the content of this register is 20h.

**FIGURE 88. Infrared Control Register 3**

**B0 Reserved.**
Write 0.

**B1 TXCRC_DS – Disable Transmitter CRC.**
When set to 1, a CRC is not transmitted.

**B2 TXCRC_INV – Invert Transmitter CRC.**
When set to 1, an inverted CRC is transmitted.This bit can be used to force a bad CRC for testing purposes.

**B3 Reserved.**
Write 0.

**B4 MIR_CRC – MIR Mode CRC Select.**
Determines the length of the CRC in MIR mode.
0 → 16-bit CRC
1 → 32-bit CRC

**B5 FIR_CRC – FIR Mode CRC Select.**
Determines the length of the CRC in FIR mode.
0 → 16-bit CRC
1 → 32-bit CRC

**B6 SHMD_DS – Sharp-IR Modulation Disable.**
When set to 1, internal 500 kHz transmitter modulation is disabled.

**B7 SHDM_DS – Sharp-IR Demodulation Disable.**
When set to 1, internal 500 kHz receiver demodulation is disabled.

### 5.20.2 MIRPW – MIR Pulse Width Register

This register is used to program the width of the transmitted MIR infrared pulses in increments of either 20.833 ns or 41.666 ns depending on the setting of the MDSR bit in the IRCR2 register. The programmed value has no effect on the MIR receiver. After reset, the content of this register is 0Ah.

**FIGURE 88. MIR Pulse Width Register**

**B3-0 MPW [3–0] – MIR Signal Pulse Width**

**TABLE 89. MIR Pulse Width Settings**

| ENCODING | Pulse Width MDRS = 0 | Pulse Width MDRS = 1 |
|---|---|---|
| 00XX | Reserved | Reserved |
| 0100 | 83.33 ns | 166.66 ns |
| 0101 | 104.16 ns | 208.33 ns |
| 0110 | 125 ns | 250 ns |
| 0111 | 145.83 ns | 291.66 ns |
| 1000 | 166.66 ns | 333.33 ns |
| 1001 | 187.50 ns | 374.99 ns |
| 1010 | 208.33 ns | 416.66 ns |
| 1011 | 229.16 ns | 458.33 |
| 1100 | 250 ns | 500 ns |
| 1101 | 270.83 ns | 541.66 ns |
| 1110 | 291.66 ns | 583.32 ns |
| 1111 | 312.5 ns | 625 ns |

**B7-4 Reserved.**

Write 0's.

### 5.20.3 SIR_PW – SIR Pulse Width Register

This register determines the width of the transmitted SIR infrared pulses.

The programmed value has no effect on the SIR receiver. After reset, the content of this register is 0.

**FIGURE 88. SIR Pulse Width Register**

**B3-0 SPW [3-0] – SIR Signal Pulse Width.**

| Encoding | Pulse Width |
|---|---|
| 0000 | 3/16 of bit time |
| 1101 | 1.6 µs |

Other encodings are reserved and will select a pulse width of 1.6 µs.

**B7-4 Reserved.**

Write 0's.

### 5.20.4 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

### 5.20.5 BFPL – Beginning Flags/Preamble Length Register

Used to program the number of beginning flags and preamble symbols for MIR and FIR modes respectively.

After reset, the content of this register is 2Ah, selecting 2 beginning flags and 16 preamble symbols.

**FIGURE 88. Beginning Flags/Preamble Length Register**

**B3–0 FPL [3–0] – FIR Preamble Length.**

Selects the number of preamble symbols for FIR frames.

**TABLE 90. FIR Preamble Length**

| ENCODING | Preamble Length |
|---|---|
| 0000 | Reserved |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 8 |
| 1000 | 10 |
| 1001 | 12 |
| 1010 | 16 (Default) |
| 1011 | 20 |
| 1100 | 24 |
| 1101 | 28 |
| 1110 | 32 |
| 1111 | Reserved |

**B7–4 MBF [3–0] – MIR Beginning Flags.**

Selects the number of beginning flags for MIR frames.

**TABLE 91. MIR Beginning Flags**

| ENCODING | Beginning Flags |
|---|---|
| 0000 | Reserved |
| 0001 | 1 |
| 0010 | 2 (Default) |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 8 |
| 1000 | 10 |
| 1001 | 12 |
| 1010 | 16 |
| 1011 | 20 |
| 1100 | 24 |
| 1101 | 28 |
| 1110 | 32 |
| 1111 | Reserved |

## 5.21 BANK 7

**TABLE 92. Bank 7 Register Set**

| Address Offset | Register Name | Description |
|---|---|---|
| 00h | IRRXDC | Infrared Receiver Demodulator Control |
| 01h | IRTXMC | Infrared Transmitter Modulator Control |
| 02h | RCCFG | CEIR Configuration Register |
| 03h | LCR/BSR | Link Control/ Bank Select Registers |
| 04h | IRCFG1 | Infrared Interface Configuration Register 1 |
| 05h | IRCFG2 | Infrared Interface Configuration Register 2 |
| 06h | IRCFG3 | Infrared Interface Configuration Register 3 |
| 07h | IRCFG4 | Infrared Interface Configuration Register 4 |

### 5.21.1 IRRXDC – Infrared Receiver Demodulator Control Register

After reset, the content of this register is 29h, selecting a frequency range from 34.61 kHz to 38.26 kHz for the CEIR mode, and from 480.0 kHz to 533.3 kHz for Sharp-IR mode. The value of this register is ignored if receiver demodulation for both Sharp-IR and CEIR mode is disabled. The available frequency ranges for CEIR and Sharp-IR modes are given in Table 93 through Table 95.

**FIGURE 88. Intrared Receiver Demodulator Control Register**

**B4–0 DFR [4–0] – Demodulator Frequency.**

These bits determine the subcarrier's center frequency for the CEIR mode.

**B7–5 DBW [2–0] – Demodulator Bandwidth.**

These bits determine the demodulator bandwidth within which the subcarrier signal frequency has to fall in order for the signal to be accepted.

Used for both Sharp-IR and CEIR modes.

**TABLE 93. CEIR, Low Speed Demodulator (RXHSC = 0) (Frequency Ranges in kHz)þ**

| | BBW [2-0] Bits | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DFR [4-0] | 001 | | 010 | | 011 | | 100 | | 101 | | 110 | |
| | min | max | min | max | min | max | min | max | min | max | min | max |
| 00011 | 28.6 | 31.6 | 27.3 | 33.3 | 26.1 | 35.3 | 25.0 | 37.5 | 24.0 | 40.0 | 23.1 | 42.9 |
| 00100 | 29.3 | 32.4 | 28.0 | 34.2 | 26.7 | 36.2 | 25.6 | 38.4 | 24.6 | 41.0 | 23.7 | 43.9 |
| 00101 | 30.1 | 33.2 | 28.7 | 35.1 | 27.4 | 37.1 | 26.3 | 39.4 | 25.2 | 42.1 | 24.3 | 45.1 |
| 00110 | 31.7 | 35.1 | 30.3 | 37.0 | 29.0 | 39.2 | 27.8 | 41.7 | 26.7 | 44.4 | 25.6 | 47.6 |
| 00111 | 32.6 | 36.0 | 31.1 | 38.1 | 29.8 | 40.3 | 28.5 | 42.8 | 27.4 | 45.7 | 26.3 | 48.9 |
| 01000 | 33.6 | 37.1 | 32.0 | 39.2 | 30.7 | 41.5 | 29.4 | 44.1 | 28.2 | 47.0 | 27.1 | 50.4 |
| 01001 | 34.6 | 38.3 | 33.0 | 40.4 | 31.6 | 42.8 | 30.3 | 45.4 | 29.1 | 48.5 | 28.0 | 51.9 |
| 01011 | 35.7 | 39.5 | 34.1 | 41.7 | 32.6 | 44.1 | 31.3 | 46.9 | 30.0 | 50.0 | 28.8 | 53.6 |
| 01100 | 36.9 | 40.7 | 35.2 | 43.0 | 33.7 | 45.5 | 32.3 | 48.4 | 31.0 | 51.6 | 29.8 | 55.3 |
| 01101 | 38.1 | 42.1 | 36.4 | 44.4 | 34.8 | 47.1 | 33.3 | 50.0 | 32.0 | 53.3 | 30.8 | 57.1 |
| 01111 | 39.4 | 43.6 | 37.6 | 45.9 | 36.0 | 48.6 | 34.5 | 51.7 | 33.1 | 55.1 | 31.8 | 59.1 |
| 10000 | 40.8 | 45.1 | 39.0 | 47.6 | 37.3 | 50.4 | 35.7 | 53.6 | 34.3 | 57.1 | 33.0 | 61.2 |
| 10010 | 42.3 | 46.8 | 40.4 | 49.4 | 38.6 | 52.3 | 37.0 | 55.6 | 35.6 | 59.3 | 34.2 | 63.5 |
| 10011 | 44.0 | 48.6 | 42.0 | 51.3 | 40.1 | 54.3 | 38.5 | 57.7 | 36.9 | 61.5 | 35.5 | 65.9 |
| 10101 | 45.7 | 50.5 | 43.6 | 53.3 | 41.7 | 56.5 | 40.0 | 60.0 | 38.4 | 64.0 | 36.9 | 68.6 |
| 10111 | 47.6 | 52.6 | 45.5 | 55.6 | 43.5 | 58.8 | 41.7 | 62.5 | 40.0 | 66.7 | 38.5 | 71.4 |
| 11010 | 49.7 | 54.9 | 47.4 | 57.9 | 45.3 | 61.4 | 43.5 | 65.2 | 41.7 | 69.5 | 40.1 | 74.5 |
| 11011 | 51.9 | 57.4 | 49.5 | 60.6 | 47.4 | 64.1 | 45.4 | 68.1 | 43.6 | 72.7 | 41.9 | 77.9 |
| 11101 | 54.4 | 60.1 | 51.9 | 63.4 | 49.7 | 67.2 | 47.6 | 71.4 | 45.7 | 76.1 | 43.9 | 81.6 |

**TABLE 94. Consumer IR High Speed Demodulator Frequency Ranges in kHz (RXHSC = 1)**

| | BBW [2-0] Bits | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DFR [4-0] | 001 | | 010 | | 011 | | 100 | | 101 | | 110 | |
| | min | max | min | max | min | max | min | max | min | max | min | max |
| 00011 | 381.0 | 421.1 | 363.6 | 444.4 | 347.8 | 470.6 | 333.3 | 500.0 | 320.0 | 533.3 | 307.7 | 571.4 |
| 01000 | 436.4 | 480.0 | 417.4 | 505.3 | 400.0 | 533.3 | 384.0 | 564.7 | 369.2 | 600.0 | 355.6 | 640.0 |
| 01011 | 457.7 | 505.3 | 436.4 | 533.3 | 417.4 | 564.7 | 400.0 | 600.0 | 384.0 | 640.0 | 369.9 | 685.6 |

**TABLE 95. Sharp-IR Demodulator Frequency Ranges in kHz**

| | BBW [2-0] Bits | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DFR [4-0] | 001 | | 010 | | 011 | | 100 | | 101 | | 110 | |
| | min | max | min | max | min | max | min | max | min | max | min | max |
| xxxxx | 480.0 | 533.3 | 457.1 | 564.7 | 436.4 | 600.0 | 417.4 | 640.0 | 400.0 | 685.6 | 384.0 | 738.5 |

### 5.21.2 IRTXMC – Infrared Transmitter Modulator Control Register

Used to select the modulation subcarrier parameters for CEIR and Sharp-IR modes. For Sharp-IR, only the subcarrier pulse width is controlled by this register, the subcarrier frequency is fixed at 500 kHz.

After reset, the content of this register is 69h, selecting a subcarrier frequency of 36 kHz and a pulse width of 7 µs for CEIR, or a pulse width of 0.8 µs for Sharp-IR.

**FIGURE 88. Intrared Transmitter Modulator Control Register**

**B4–0 MCFR [4–0] – Modulation Subcarrier Frequency.**

Selects the frequency for the CEIR modulation subcarrier.

**TABLE 96. CEIR Carrier Frequency Encoding**

| Encoding | Low Frequency, TXHSC = 0 | High Frequency, TXHSC = 1 |
|---|---|---|
| 00000 | Reserved | Reserved |
| 00001 | Reserved | Reserved |
| 00010 | Reserved | Reserved |
| 00011 | 30 kHz | 400 kHz |
| 00100 | 31 kHz | Reserved |
| 00101 | 32 kHz | Reserved |
| 00110 | 33 kHz | Reserved |
| 00111 | 34 kHz | Reserved |
| 01000 | 35 kHz | 450 kHz |
| 01001 | 36 kHz | Reserved |
| 01010 | 37 kHz | Reserved |
| 01011 | 38 kHz | 480 kHz |
| 01100 | 39 kHz | Reserved |
| 01101 | 40 kHz | Reserved |
| 01110 | 41 kHz | Reserved |
| 01111 | 42 kHz | Reserved |
| 10000 | 43 kHz | Reserved |
| 10001 | 44 kHz | Reserved |
| 10010 | 45 kHz | Reserved |
| 10011 | 46 kHz | Reserved |
| 10100 | 47 kHz | Reserved |
| 10101 | 48 kHz | Reserved |
| 10110 | 49 kHz | Reserved |
| 10111 | 50 kHz | Reserved |
| 11000 | 51 kHz | Reserved |
| 11001 | 52 kHz | Reserved |
| 11010 | 53 kHz | Reserved |
| 11011 | 54 kHz | Reserved |
| 11100 | 55 kHz | Reserved |
| 11101 | 56 kHz | Reserved |
| 11110 | 56.9 kHz | Reserved |
| 11111 | Reserved | Reserved |

**B7–5 MCPW [2–0] – Modulation Subcarrier Pulse Width.**

| Encoding | Low Frequency, TXHSC = 0 (CEIR only) | High Frequency, TXHSC = 1 (CEIR or Sharp-IR) |
|---|---|---|
| 000 | Reserved | Reserved |
| 001 | Reserved | Reserved |
| 010 | 6 µs | 0.7 µs |
| 011 | 7 µs | 0.8 µs |
| 100 | 9 µs | 0.9 µs |
| 101 | 10.6 µs | Reserved |
| 110 | Reserved | Reserved |
| 111 | Reserved | Reserved |

### 5.21.3 RCCFG – CEIR Configuration Register

This register controls the basic operation of the CEIR mode.

After reset, all bits are set to 0.

**FIGURE 88. CEIR Configuration Register**

**B1–0 RC_MMD [1–0] – Transmitter Modulation Mode.**

Determines how infrared pulses are generated from the transmitted bit string.

00 → C_PLS Modulation Mode.Pulses are generated continuously for the entire logic 0 bit time.

01 → 8_PLS Modulation Mode.8 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit.

10 → 6_PLS Modulation Mode.6 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit.

11 → Reserved.Result is indeterminate.

**B2 TXHSC – Transmitter Subcarrier Frequency Select.**

Selects the frequency range for the modulation subcarrier.

0 → 30–56.9 kHz

1 → 400–480 kHz

**B3 Reserved.**

Write 0.

**B4 RCDM_DS – Receiver Demodulation Disable.**

When this bit is 1, the internal demodulator is disabled. The internal demodulator, when enabled, performs subcarrier frequency checking and envelope generation.

It must be disabled when demodulation is done externally, or when oversampling mode is used to determine the subcarrier frequency.

**B5 RXHSC – Receiver Subcarrier Frequency Select.**

Selects the frequency range for the receiver demodulator.

0 → 30–56.9 kHz

1 → 400–480 kHz

**B6 T_0V – Receiver Sampling Mode.**

0 → Programmed-T-period sampling.

1 → Oversampling Mode.

**B7 R_LEN – Run-Length Control.**

When set to 1, run-length encoding/decoding is enabled.

The format of a run-length code is YXXXXXXX, where:

**Y** - Bit value

**XXXXXXX—** Number of bits minus 1. (Selects 1 to 128 bits).

### 5.21.4 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

### 5.21.5 IRCFG [1–4] – Infrared Interface Configuration Registers

Four registers are provided to configure the infrared interface. These registers are used to select the infrared receiver inputs as well as the transceiver operational mode. Selection of the transceiver mode is accomplished by up to three special output signals (ID/IRSL [2–0]). When these signals are programmed as outputs, they will be forced low when automatic configuration is enabled (AMCFG bit set to 1) and UART mode is selected.

## IRCFG1 – Infrared Interface Configuration Register 1

This register holds the transceiver configuration data for Sharp-IR and SIR Modes.

When automatic configuration is not enabled, it is used to directly control the transceiver operational mode. The least significant four bits are also used to read the identification data of a Plug-n-Play infrared adapter.

**FIGURE 88. Infrared Configuration Register 1**

**B0 IRIC0 – Transceiver Identification/Control.**

The function of this bit depends on whether the ID0/IRSL0/IRRX2 pin is programmed as an input or as an output.

ID0/IRSL0/IRRX2 Pin Programmed as Input (IRSL0_DS = 0).

Upon read, this bit returns the logic level of the pin.

Data written into this bit position is ignored.

ID0/IRSL0/IRRX2 Pin Programmed as Output (IRSL0_DS = 1).

If AMCFG is set to 1, this bit will drive the ID0/IRSL0/IRRX2 pin when Sharp-IR Mode is selected.

If AMCFG is 0, this bit will drive the ID0/IRSL0/IRRX2 pin regardless of the selected mode.

Upon read, this bit returns the value previously written.

**B2–1 IRIC[2–1] – Transceiver Identification/Control**

The function of these bits depends on whether the ID/IRSL[2–1] pins are programmed as inputs or as outputs.

ID/IRSL[2–1] Pins Programmed as Inputs (IRSL21_DS = 0).

Upon read, these bits return the logic levels of the pins.

Data written into these bit positions is ignored.

ID/IRSL[2–1] Pins Programmed as Outputs (IRSL21_DS = 1).

If AMCFG is set to 1, these bits will drive the ID/IRSL[2–1] pins when Sharp-IR Mode is selected.

If AMCFG is 0, these bits will drive the ID/IRSL[2–1] pins regardless of the selected mode.

Upon read, these bits return the values previously written.

**B6–4 SIRC [2–0] – SIR Mode Transceiver Configuration.**

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and SIR Mode is selected.

They are unused when AMCFG is 0 or when the ID/IRSL[2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

**B7 STRV_MS – Special Transceiver Mode Select.**

This bit is used to select the operational mode in high speed optical transceiver modules. When this bit is set to 1, the IRTX output is forced high and a timer is started.

The timer times out after approximately 64 µs, at which time the bit is reset and IRTX returns low. The timer is restarted every time a 1 is written into this bit position. Therefore, the time in which IRTX is forced high can be extended beyond 64 µs.

This should be avoided, however, to prevent damage to the transmitter LED.

Writing 0 into this bit position has no effect.

## IRCFG2 – Infrared Interface Configuration Register 2

This register holds the transceiver configuration data for MIR and FIR Modes.

**FIGURE 88. Infrared Configuration Register 2**

**B2–0 MIRC [2–0] – MIR Mode Transceiver Configuration.**

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and MIR Mode is selected.

They are unused when AMCFG is 0 or when the ID/IRSL [2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

**B3 Reserved.**

Write 0.

**B6–4 FIRC [2–0] – FIR Mode Transceiver Configuration.**

These bits will drive the ID/IRSL [2–0] pins when AMCFG is 1 and FIR Mode is selected.

They are unused when AMCFG is 0 or when the ID/IRSL [2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

**B7 Reserved.**

Write 0.

## IRCFG3—Infrared Interface Configuration 3

This register holds the transceiver configuration data for Low-Speed and High-Speed CEIR Modes.

**FIGURE 88. Infrared Configuration Register 3**

**B2–0 RCLC [2–0] – CEIR Mode Transceiver Configuration, Low-Speed.**

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and CEIR Mode with 30 kHz–56 kHz receiver subcarrier frequency is selected.

They are unused when AMCFG is 0 or when the ID/IRSL[2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

**B3 Reserved.**

Write 0.

**B6–4 RCHC [2–0] – CEIR Mode Transceiver Configuration, High-Speed.**

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and CEIR Mode with 400 kHz–480 kHz receiver subcarrier frequency is selected.

They are unused when AMCFG is 0 or when the ID/IRSL[2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

**B7 Reserved.**

Write 0.

## IRCFG4 – Infrared Interface Configuration 4

This register is used to configure the receiver data path and enable the automatic selection of the configuration pins. After reset, the content of this register is 0.

**FIGURE 88. Infrared Configuration Register 4**

**B2–0 Reserved.**

Read/write 0's.

**B3 IRSL21_DS – ID/IRSL[2–1] Pins' Direction Select.**

This bit determines the direction of the ID/IRSL[2–1] pins.

0 → Pins' direction is input.

1 → Pins' direction is output.

**B4 RXINV – IRRX Signal Invert.**

This bit is provided to support optical transceivers with receive signals of opposite polarity (active high instead of active low).

When set to 1, an inverter is placed on the receiver input signal path.

**B5 IRSL0_DS – ID0/IRSL0/IRRX2 Pin Direction Select.**

This bit determines the direction of the ID0/IRSL0/IRRX2 pin.

0 → Pin's direction is input.

1 → Pin's direction is output.

**B6 IRRX_MD – IRRX Mode Select.**

Determines whether a single input or two separate inputs are used for Low-Speed and High-Speed IrDA modes.

0 → One input is used for both SIR and MIR/FIR.

1 → Separate inputs are used for SIR and MIR/FIR.

Table 97 shows the IRRXn pins used in the PC97338 for the low-speed and high-speed

infrared modes, and for the various combinations of IRSL0_DS, IRRX_MD and AUX_IRRX.

**B7 AMCFG – Automatic Module Configuration Enable.**

When set to 1, automatic infrared transceiver configuration is enabled.

**TABLE 97. Infrared Receiver Input Selection**

**(HIS_IR = 1 When Selected Mode is MIR or FIR)**

| IRSL0_DS | IRRX_MD | AUX_IRRX | HIS_IR | IRRXn |
|---|---|---|---|---|
| 0 | 0 | 0 | x | IRRX1 |
| 0 | 0 | 1 | x | IRRX2 |
| 0 | 1 | x | 0 | IRRX1 |
| 0 | 1 | x | 1 | IRRX2 |
| 1 | 0 | 0 | x | IRRX1 |
| 1 | 0 | 1 | x | Reserved |
| 1 | 1 | x | 0 | IRRX1 |
| 1 | 1 | x | 1 | Reserved |

## 5.22 SERIAL COMMUNICATION CONTROLLER2 REGISTER BITMAPS

**Extended Mode**

**Interrupt Enable Register (IER) Bank 0, Offset 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- RXHDL_IE
- TXLDL_IE
- LS_IE / TXHLT_IE
- MS_IE
- DMA_IE
- TXEMP_IE / PLD_IE
- SFIF_IE (MIR and FIR only)
- TMR_IE

**Write Cycles**

**FIFO Control Register (FCR) Bank 0, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | 0 | | | | Required |

- FIFO_EN
- RXSR
- TXSR
- Reserved
- TXFTH0
- TXFTH1
- RXFTH0
- RXFTH1

**Non-Extended Modes, Read Cycle**

**Event Identification Register (EIR) Bank 0, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Reset |
| | | 0 | 0 | | | | | Required |

- IPF - Interrupt Pending
- IPR0 - Interrupt Priority 0
- IPR1 - Interrupt Priority 1
- RXFT - RX_FIFO Time-Out
- Reserved
- Reserved
- FEN0 - FIFO Enabled
- FEN1 - FIFO Enabled

**Link Control Register (LCR) All Banks, Offset 03h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- WLS0
- WLS1
- STB
- PEN
- EPS
- STKP
- SBRK
- BKSE

**Extended Mode, Read Cycles**

**Event Identification Register (EIR) Bank 0, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Reset |
| | | | | | | | | Required |

- RXHDL_EV
- TXLDL_EV
- LS_EV / TXHLT_EV
- MS_EV
- DMA_EV
- TXEMP-EV / PLD_EV
- SFIF_EV (FIR and MIR only)
- TMR_EV

**Bank Selection Register (BSR) All Banks, Offset 03h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

Bank Selected

BKSE-Bank Selection Enable

**Non-Extended Mode**

**Modem Control Register (MCR) Bank 0, Offset 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | | | | | | Required |

- DTR
- RTS
- RILP
- ISEN / DCDLP
- LOOP
- Reserved
- Reserved
- Reserved

**Extended Mode**

**Modem Control Register (MCR) Bank 0, Offset 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- 0 → DTR
- 1 → RTS
- 2 → DMA_EN
- 3 → TX_DFR
- 4 → IR_PLS
- 5 → MDSL0
- 6 → MDSL1
- 7 → MDSL2

**Extended Modes**

**Auxiliary Status Register (ASCR) Bank 0, Offset 07h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | 0 | | | | Required |

- 0 → RXF_TOUT
- 1 → FEND_INF
- 2 → S_EOT
- 3 → TXHFE (MIR / FIR only)
- 4 → LOST_FR / RXWDG
- 5 → RXBSY / RXACT
- 6 → TXUR
- 7 → PLD/CTE

**Non-Extended Mode**

**Link Status Register (LSR) Bank 0, Offset 05h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- 0 → RXDA
- 1 → OE
- 2 → PE / BAD_CRC
- 3 → FE / PHY_ERR
- 4 → BRK / MAX_LEN
- 5 → TXRDY
- 6 → TXEMP
- 7 → ER_INF / FR_END

**Legacy Baud Generator Divisor Low Byte Register (LBGD(L)) Bank 1, Offset 00h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

Least Significant Byte of Baud Rate Generator

**Modem Status Register (MSR) Bank 0, Offset 06h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | x | x | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

- 0 → DCTS
- 1 → DDSR
- 2 → TERI
- 3 → DDCD
- 4 → CTS
- 5 → DSR
- 6 → RI
- 7 → DCD

**Legacy Baud Generator Divisor High Byte Register (LBGD(H)) Bank 1, Offset 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

Most Significant Byte of Baud Rate Generator

**Non-Extended Mode**

**Scratch Register (SCR) Bank 0, Offset 07h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset |
| | | | | | | | | Required |

Scratch Data

**Baud Generator Low Byte Register (BGD(L)) Bank 2, Offset 00h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | x | x | Reset |
| | | | | | | | | Required |

Least Significant Byte of Baud Rate Generator

**Extended Control and and Status Register 2 (EXCR2) Bank 2, Offset 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | 0 | | | | | | | Required |

TF_SIZ0
TF_SIZ1
RF_SIZ0
RF_SIZ1
PRESL0
PRESL1
Reserved
LOCK

**Baud Generator High Byte Register (BGD(H)) Bank 2, Offset 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | x | x | Reset |
| | | | | | | | | Required |

Most Significant Byte of Baud Rate Generator

**IrDA or CEIR Modes**

**TX_FIFO Current Level Register (TXFLV) Bank 2, Offset 06h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | | | | | | | Required |

TFL0
TFL1
TFL2
TFL3
TFL4
TFL5
Reserved
Reserved

**Extended Control and and Status Register 1 (EXCR1) Bank 2, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | 1 | | | | | | | Required |

EXT_SL
DMANF
DMATH
DMASWP
LOOP
ETDLBK
Reserved
BTEST

**IrDA or CEIR Modes**

**RX_FIFO Current Level Register (RXFLV) Bank 2, Offset 07h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | | | | | | | Required |

RFL0
RFL1
RFL2
RFL3
RFL4
RFL5
Reserved
Reserved

**Module Revision ID Register (MRID) Bank 3 Offset 00h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | x | x | x | x | Reset |
| | | | | | | | | Required |

Revision ID(RID 3-0)

Module ID(MID 7-4)

**Shadow of Link Control Register (SH_LCR) Bank 3, Offset 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

WLS0
WLS1
STB
PEN
EPS
STKP
SBRK
BKSE

**Infrared Control Register1 (IRCR1) Bank 4, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | 0 | | | | | Required |

TMR_EN
CTEST
IR_SL0
IR_SL1
Reserved

**Shadow of FIFO Control Register (SH_FCR) Bank 3, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

FIFO_EN
RXFR
TXFR
Reserved
TXFTH0
TXFHT1
RXFTH0
RXFTH1

**Transmission Frame Length or Current Count Least Significant Bits (TFRL(L) or TFRCC(L)) Register Bank 4, Offset 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

Least Significant Bits of Transmission Frame Length or Current Count

**Timer Register Low Byte Register (TMR(L)) Bank 4, Offset 00h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | x | x | Reset |
| | | | | | | | | Required |

Least Significant Bits of Interval Timer

**Transmission Frame Length or Current Count Most Significant Bits (TFRL(H) or TFRCC(H)) Register Bank 4, Offset 05h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | | | | | | Required |

Most Significant Bits of Transmission Frame Length or Current Count
Reserved

**Timer Register High Byte Register (TMR(H)) Bank 4, Offset 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | x | x | x | x | Reset |
| 0 | 0 | 0 | 0 | | | | | Required |

Most Significant Bits of Interval Timer
Reserved

**Reception Frame Maximum Length LSB or Current Count LSB (RFRML(L) or RFRCC(L)) Register Bank 4, Offset 06h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

Least Significant Bits of Reception Frame Length or Current Count

**Pipeline Mode Register (P_MDR) Bank 5, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

MD_PEN
BR_PEN
P_DMA_EN
P_DMASWP
Reserved
P_MDSL0
P_MDSL1
P_MDSL2

**Reception Frame Maximum Length MSB or Current Count MSB (RFRML(H) or RFRCC(H)) Register Bank 4, Offset 07h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | | | | | | Required |

Most Significant Bits of Reception Frame Length or Current Count

Reserved

**Infrared Control Register 2 (IRCR2) Bank 5, Offset 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Reset |
| 0 | | | | | | | | Required |

IR_FDPLX
IRMSSL
MDRS
TX_MS
AUX_IRRX
FEND_MD
SFTSL
Reserved

**Pipeline Baud Rate Generator Divisor Low sand High Byte (P_LBGD(L) and P_BGD(H)) Bank 5, and P_BGD(H)) Offsets 00h,01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | x | x | Reset |
| | | | | | | | | Required |

High/Low Divisor Byte

**Frame Status at FIFO Bottom Register (FRM_ST) Bank 5, Offset 05h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | | | | Required |

OVR2
OVR1
BAD_CRC
PHY_ERR
MAX_LEN
Reserved
LOST_FR
VLD

**Reception Frame Length FIFO Bottom LSB Register (RFRL(L)) or Lost Frame Count LSB Register (LSTFRC) Bank 5, Offset 06h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | x | x | Reset |
| | | | | | | | | Required |

Least Significant Bits of Received Frame Length FIFO Bottom or of the Lost Frame Count

**Reception Frame Length FIFO Bottom MSB Register (RFRL(H)) Bank 5, Offset 07h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | | | | | | Required |

Least Significant Bits of Received Frame Length FIFO Bottom or of the Lost Frame Count

Reserved

**Beginning Flags and Preamble Length Register (BFPL) Bank 6, Offset 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Reset |
| | | | | | | | | Required |

FPL(3-0)

MBF(7-4)

**Infrared Control Register 3 (IRCR3) Bank 6, Offset 00h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | 0 | | | 0 | Required |

Reserved

TXCRC_DS

TXCRC_INV

Reserved

MIR_CRC

FIR_CRC

SHMD_DS

SHDM_DS

**Infrared Receiver Demodulation Control Register (IRRXDC) Bank 7, Offset 00h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Reset |
| | | | | | | | | Required |

DFR0

DFR1

DFR2

DFR3

DFR4

DBW0

DBW1

DBW2

**MIR Pulse Width Register (MIR_PW) Bank 6, Offset 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Reset |
| 0 | 0 | 0 | 0 | | | | | Required |

MPW(3-0)

Reserved

**Infrared Transmitter Modulation Control Register (IRTXMC) Bank 7, Offset 01h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | Reset |
| | | | | | | | | Required |

MCFR(4-0)

MCPW(2-0)

**SIR Pulse Width Register (SIR_PW) Bank 6, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | 0 | | | | | Required |

SPW(3-0)

Reserved

**Configuration Register (RCCFG) Bank 7, Offset 02h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | 0 | | | | Required |

RC_MMD0

RC_MMD1

TXHSC

Reserved

RCDM_DS

RXHSC

T_OV

R_LEN

**Infrared Configuration Register 1 (IRCFG1) Bank 7, Offset 04h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | Reset |
| | | | | 0 | | | | Required |

IRIC(2-0)

Reserved

SIRC(2-0)

STRV_MS

**Infrared Configuration Register 2 (IRCFG2) Bank 7, Offset 05h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | | | | 0 | | | | Required |

MIRC(2-0)

Reserved

FIRC(2-0)

Reserved

**Infrared Configuration Register 3 (IRCFG3) Bank 7, Offset 06h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | | | | 0 | | | | Required |

RCLC(2-0)

Reserved

RCHC(2-0)

Reserved

**Infrared Configuration Register 4 (IRCFG4) Bank 7, Offset 07h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| | | | | | 0 | 0 | 0 | Required |

Reserved

IRSL21_DS

RXINV

IRSL0_DS

IRRX_MD

AMCFG

# 6.0 DMA and Interrupt Mapping

The Chip provides Plug and Play support.

## 6.1 DMA SUPPORT

### 6.1.1 Legacy Mode

Table 98 shows the conditions under which DMA request signals are put in TRI-STATE, in legacy mode. For each DMA signal to be put in TRI-STATE, every column must have one true condition. If no condition is true in any one column, the signal is not put in TRI-STATE.

### 6.1.2 Plug and Play Mode

The Chip allows the Floppy Disk Controller (FDC), the parallel port and SCC2 to be connected to three 8-bit DMA channels.

It is illegal to configure a pair of DMA signals to more than one DMA source.

A pair of DMA signals may be configured to a specific device only when the device is disabled.

Upon reset, DRQ2 and $\overline{\text{DACK2}}$ are used by the FDC.

A DRQ line is in TRI-STATE and the $\overline{\text{DACK}}$ line input is blocked to 1, when any of the following conditions is true:

- When no device is mapped to the DMA channel.
- When the device mapped to the DMA channel is inactive.

  In Plug and Play mode, this condition is true for all devices.

  In Legacy mode, this condition is true only for SCC2 and the parallel port, controlled by bit 2 of the FER register and bit 2 of the PCR register, respectively.
- When the device mapped to the DMA channel floats its DRQ line.

Table 99 shows the conditions that put DMA request signals in TRI-STATE, in Plug and Play mode. For each DMA signal to be put in TRI-STATE, every column must have one true condition. If no condition is true in any one column, the signal is not put in TRI-STATE.

**TABLE 98. DMA Support in Legacy Mode**

| DMA Signal | Conditions for DRQx[a] to be in TRI-STATE | | |
|---|---|---|---|
| | Parallel Port | FDC | SCC2 |
| DRQx[a] | DRQx[a] not selected<br>or<br>bit 2 of PCR = 0<br>or<br>bit 2 of PCR = 1<br>and bit 3 of ECR =0 | DRQx[a] not selected<br>or<br>bit 3 of DOR = 0<br>and bit 7 of ASC = 1 | DRQx[a] not selected<br>or<br>bit 2 of FER. = 0 |

a. x = 0, 1 or 2

**TABLE 99. DMA Support in Plug and Play Mode**

| DMA Signal | Conditions for DRQx[a] to be in TRI-STATE | | |
|---|---|---|---|
| | Parallel Port | FDC | SCC2 |
| DRQx[a] | DRQx[a] not selected<br>or<br>bit 0 of FER = 0<br>or<br>bit 2 of PCR = 0<br>or<br>bit 2 of PCR = 1<br>and bit 3 of ECR =0 | DRQx[a] not selected<br>or<br>bit 3 of FER = 0<br>or<br>bit 3 of DOR = 0<br>and bit 7 of ASC = 1 | DRQx[a] not selected<br>or<br>bit 2 of FER = 0 |

a. x = 0, 1 or 2

## 6.2 INTERRUPT SUPPORT

### 6.2.1 Legacy Mode

Tables 100 and 101 describe the possible interrupt source for each IRQ, in legacy mode. A plus sign (+) means this is a possible interrupt source and a minus sign (–) means it is not.

Table 101 also indicates the conditions that must be true to enable IRQ 5, 12 and 15. All conditions in the row (horizontally) must be true to enable the interrupt. An x indicates the value does not matter.

It is illegal to configure two or more devices to the same ISA interrupt, with the exception of SCC1 and SCC2 which can be configured to the same ISA interrupt. An ISA interrupt may be configured to a specific device only when the device is disabled.

Table 102 describes the conditions under which each interrupt is put in TRI-STATE, in Legacy mode.

For each interrupt to be put in TRI-STATE, every column must have one true condition. If no condition is true in any one column, the signal will not be put in TRI-STATE.

**TABLE 100. Interrupt Support in Legacy Mode for IRQ3, 4, 6, 7, 9 10 and 11**

| Interrupt | Possible Interrupt Source | | | | |
|---|---|---|---|---|---|
| | SCC1 | SCC2 | Parallel Port | FDC | SIRQIn[a] |
| IRQ3,4 | + | + | – | – | + |
| IRQ6 | – | – | – | + | + |
| IRQ7 | – | – | + | – | + |
| IRQx[b] | – | – | – | – | + |

a. n = 1, 2 or 3
b. x = 9, 10 or 11

**TABLE 101. Interrupt Support in Legacy Mode for IRQ 5, 12 and 15**

| Interrupt | Conditions | | | | Possible Interrupt Source | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Bit 0 of ASC | Bit 3 of SCF3 | Bits 7,6 of SIRQI1 | Reset Value of CFG0 | SCC1 | SCC2 | Parallel Port | FDC | SIRQI1 | SIRQI2 | SIRQI3 |
| IRQ5 | 0 | x | x | x | – | – | + | – | + | + | + |
| | 1 | x | x | x | – | – | – | – | – | – | – |
| IRQ12 | x | 0 | x | 0 | – | – | – | – | + | + | + |
| | x | 1 | x | 0 | – | – | – | – | – | – | – |
| | x | x | x | 1 | – | – | – | – | – | – | – |
| IRQ15 | x | x | 0 0 | x | – | – | – | – | – | + | + |
| | x | x | 0 1 | x | – | – | – | – | – | – | – |
| | x | x | 1 x | x | – | – | – | – | – | – | – |

**TABLE 102. TRI-STATE Condition for Interrupts in Legacy Mode**

| Interrupt | TRI-STATE Condition | | | | |
|---|---|---|---|---|---|
| | SCC1 | SCC2 | Parallel Port | FDC | SIRQIn[a] |
| IRQ3,4 | As described in Section 5. | As described in Section 5. | NA | NA | IRQ3 or 4 not selected |
| IRQ5,7 | NA | NA | As described in Section 4. | NA | IRQ5 or 7 not selected |
| IRQ6 | NA | NA | NA | As described in Section 3. | IRQ6 not selected |
| IRQx[b] | NA | NA | NA | NA | IRQx[b] not selected |

a. n = 1, 2 or 3
b. x = 9, 10, 11, 12 or 15

### 6.2.2 Plug and Play Mode

In Plug and Play mode, software can configure the interrupts of the Chip on the ISA interrupts.

It is illegal to configure two or more devices to the same ISA interrupt, with the exception of SCC1 and SCC2 which can be configured to the same ISA interrupt.

An interrupt should be configured to a specific device only when the device is disabled.

Tables 103 and 104 describe the possible interrupt source for each IRQ. A plus sign (+) means this is a possible interrupt source and a minus sign (–) means it is not.

Table 104 also indicates the conditions that must be true to enable IRQ 5, 12 and 15. All conditions in the row (horizontally) must be true to enable the interrupt. An x indicates the value does not matter.

Table 105 describes the conditions under which each interrupt is put in TRI-STATE, in Plug and Play mode.

For each interrupt to be put in TRI-STATE, every column must have one true condition. If no condition is true in any one column, the signal will not be put in TRI-STATE.

An IRQ signal is in TRI-STATE when any of the following conditions is true:

- When no device is mapped to the IRQ line.
- When the device mapped to the IRQ line is inactive.
- When the device mapped to the IRQ line floats its IRQ line.

**TABLE 103. Interrupt Support in Plug and Play Mode for IRQ3, 4, 6, 7, 9, 10 or 11**

| Interrupt | Source | | | | |
|---|---|---|---|---|---|
| | SCC1 | SCC2 | Parallel Port | FDC | SIRQIn[a] |
| IRQx[b] | + | + | + | + | + |

a. n = 1, 2 or 3
b. x = 3, 4, 6, 7, 9, 10 or 11

**TABLE 104. Interrupt Support in Plug and Play Mode for IRQ 5, 12 or 15**

| Interrupt | Conditions | | | | Possible Interrupt Source | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Bit 0 of ASC | Bit 3 of SCF3 | Bits 7,6 of SIRQI1 | Reset Value of CFG0 | SCC1 | SCC2 | Parallel Port | FDC | SIRQI1 | SIRQI2 | SIRQI3 |
| IRQ5 | 0 | x | x | x | + | + | + | + | + | + | + |
| | 1 | x | x | x | – | – | – | – | – | – | – |
| IRQ12 | x | 0 | x | 0 | + | + | + | + | + | + | + |
| | x | 1 | x | 0 | – | – | – | – | – | – | – |
| | x | x | x | 1 | – | – | – | – | – | – | – |
| IRQ15 | x | x | 00 | x | + | + | + | + | – | + | + |
| | x | x | 01 | x | – | – | – | – | – | – | – |
| | x | x | 1x | x | – | – | – | – | – | – | – |

**TABLE 105. TRI-STATE Conditions for Interrupts in Plug and Play Mode**

| IRQ | Conditions for IRQx[b] to be in TRI-STATE | | | | |
|---|---|---|---|---|---|
| | SCC1 | SCC2 | PP | FDC | SIRQIn[a] |
| IRQx[b] | IRQx[b] not selected<br>or<br>bit 1 of FER = 0<br>or<br>bit 3 of MCR1 = 0<br>or<br>bit 4 of MCR1 = 1 | IRQx[b] not selected<br>or<br>bit 2 of FER = 0<br>or<br>bit 3 of MCR2 = 0<br>or<br>bit 4 of MCR2 = 1 | IRQx[b] not selected<br>or<br>bit 0 of FER = 0<br>or<br>bit 4 of CTR = 0<br>or<br>bit 2 of PCR = 0 | IRQx[b] not selected<br>or<br>bit 3 of FER = 0<br>or<br>bit 3 of DOR = 0<br>or<br>bit 7 of ASC = 1 | IRQx[b] not selected |

a. n = 1, 2 or 3
b. x = 3, 4, 5, 6, 7, 9, 10, 11, 12 or 15

# 7.0 Power Management

The chip places special emphasis on power management. Power management is implemented in the two major states of the chip: Power-Down and Power-Up.

## 7.1 POWER-DOWN STATE

Power-down can be divided into two major groups:

Group 1:
Full power-down - the entire chip is powered-down/disabled.

Group 2:
Specific function power-down - specific SuperI/O modules (FDC, SCC1, SCC2, ECP, Parallel Port) are powered-down/disabled.

All power-down modes are enhanced by a new feature which allows TRI-STATE of the output pins associated with a specific function (FDC, SCC1, SCC2, Parallel Port), and reduces current leakage by blocking their inputs.

Four modules in the chip are operated by the internal clock - FDC, SCC1, SCC2 and ECP. These modules can be powered-down/disabled by stopping their associated internal clocks. In addition, all four modules can be powered-down/disabled by stopping the external crystal oscillator.

Modules which do not use a clock; e.g., Parallel Port (SPP/EPP), can be powered-down/disabled by simply blocking access to them.

All the above power-down modes can be achieved using the power-down methods from Group 1 or Group 2, as described below.

### 7.1.1 Recommended Power-Down Methods - Group 1

Use the power-down methods in Group 1 to place the chip in following modes:

#### Mode 1

The entire chip is powered-down, the oscillator is stopped, pins are TRI-STATE, and the inputs are blocked.

In this mode the maximum current saving can be achieved.

#### Mode 2

The entire chip is powered-down and the oscillator is stopped. Pins are driven.

There are five ways to reach the above two operating modes. See Table 106.

**TABLE 106. Group 1 Power-Down**

| Method | PTR bit 0 | FER bits 3210 | PCR bit 2 | PMC bits 621 | SCF0 bit 3 | Mode | Typical Current Consumption (5v $V_{CC}$) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | xxxx | x | 111 | 1 | #1 | 600 µA |
| 2 | x | 0000 | 0 | 111 | 1 | | |
| 3 | 1 | xxxx | x | 000 | 0 | #2 | 1.5 mA |
| 4 | x | 0000 | 0 | 000 | 0 | | |
| 5 | x | 1xxx | x | 000 | 0 | | |

**Notes:**

1. The chip can also be placed in Mode 2 by using method #5, and entering FDC Low Power by executing Mode Command or by setting bit 6 of DSR to high.
2. The Current Consumption values are measured under the following conditions:
   — No load on output signals
   — Input signals are stable

— $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$

— $V_{DD} = 3.3V$

— FCR bit 0 of SCC1 and SCC2 are 1 (16550 mode - FIFO enabled)

3. When PCR bit 3 is 1, and the ECP is enabled (bit 2 of PCR is 1) the clock multiplier and the ECP clock are not stopped.

### 7.1.2 Recommended Power-Down Methods - Group 2

Use the power-down methods in Group 2 to place the chip in any desired combination of the following power-down modes:

Mode 1:Parallel Port (SPP/EPP/ECP) is powered-down, providing a possible saving of up to 5 mA.

Mode 2: SCCs are powered-down, providing a possible saving of up to 5 mA.

Mode 3:FDC is powered-down, providing a possible saving of up to 4 mA.

### 7.1.3 Special Power-Down Cases

The FDC can be powered down by executing the MODE command or by setting bit 6 of DSR to high. This is equivalent to the Mode 2 described in the previous section. See Sections 3.3.7 and 3.6.7.

When the parallel port is enabled in Extended Capability Port (ECP) mode (bit 2 of the Printer Control configuration Register (PCR) is 1), powering down by setting bit 2 of the Power and Test configuration Register (PTR) will not stop the clock of the ECP. Bit 3 of PCR must also be 0 before the internal clock multiplier to the ECP can stop. See Sections 2.3.4 and 2.3.6.

## 7.2 POWER-UP

The chip powers up with all modules disabled, as described in Mode 2, above.

### 7.2.1 The Clock Multiplier

The source of all internal clocks in the chip can be either an external 48 MHz clock on the X1 pin, or the on-chip clock multiplier.

The on-chip clock multiplier is fed by applying either a 14.31818 MHz or a 24 MHz clock on the same X1 pin. It generates two internal clocks: 24 MHz and 48 MHz. The 24 MHz clock is needed for SCC1, the FDC and the Parallel Port. The 48 MHz clock is needed for SCC2 and the FDC when it supports 2Mbps data rates, as set by bit 1 of the Tape, SCCs and Parallel Port (TUP) register. See Section 2.3.8.

After power-up or reset, the clock multiplier is disabled.

#### Clock Multiplier Functionality

The on-chip clock multiplier starts working, when it is enabled via the clock multiplier enable bit (bit 2 of the CLK register, at index 51), i.e., when it changes from 0 to 1. This bit can also disable the on-chip clock multiplier and its output clock after the multiplier is enabled.

Once enabled, the output clock is frozen to a steady logic level until the multiplier can provide a stable output clock that meets all requirements; then it starts toggling.

On power-on, when $V_{DD}$ is applied, the chip wakes-up with the on-chip clock multiplier disabled. The input and output clocks of the on-chip clock multiplier may toggle regardless of the state of the Master Reset (MR) pin (they can toggle while MR is active). The on-chip clock multiplier must have a toggling input clock. If the input clock is not toggling, the on-chip clock multiplier waits until this input clock starts toggling.

Bit 3 of the CLK register is the Valid Clock Multiplier status bit. It is read only. While stabilizing, the output clock is frozen to a steady logic level, and the status bit is cleared to 0 to indicate a frozen clock. When the on-chip clock multiplier is stable, the output clock starts toggling and the status bit is set to 1. The status bit tells the software, when the clock multiplier is ready. The software should poll this status bit and activate (enable) the FDC, Parallel Port, SCCs and infrared interface only if it is 1.

When the multiplier is enabled for the first time after power-on, more time is required until this status bit is set to 1.

The on-chip clock multiplier and its output clock do not consume power, when they are disabled.

#### Clock Multiplier Specifications

Wake-up time, from valid $V_{DD}$ (2.1V minimum) toggling input clock and multiplier enabled, until clock is stable is 2.6 msec (maximum).

Tolerance (long term deviation) of the multiplier output clock, relative to input clock is ±110 ppm.

Total tolerance is therefore ± (input clock tolerance + 110 ppm).

Cycle by cycle variance is 0.4 nsec (maximum).

### 7.2.2 Chip Power-Up Procedure

To ensure proper operation, do the following, after power-up:

1. Set bits 2,1 and 0 of the Clock Control configuration (CLK) register at index 51, according to the external clock source used. See Table 107.

   Bits 2,1 and 0 may be written in a single write cycle.

**TABLE 107. Clock Multiplier Encoding Options**

| External Clock on Pin X1 (MHz) | CLK Register (Index 51h) | | | |
|---|---|---|---|---|
| | Valid Clock Multiplier Status | Clock Multiplier Enable | Chip Clock Source | |
| | 3 | 2 | 1 | 0 |
| 14.31818 | 0 = Reset<br>1 = Stable | 1 | 0 | 0 |
| 24 | | 1 | 0 | 1 |
| 48 | Always 0 | 0 | 1 | 0 |
| Reserved | x | x | 1 | 1 |

From this point on, bits 1 and 0 of the CLK register are read-only. The value of the clock source can not be changed, except by a total power-off and power-on cycle. However, the on-chip clock multiplier can be disabled at any time.

2. If the external clock source is 14.31818 MHz or 24 MHz:
   — Enable the on-chip clock multiplier.
   — Poll bit 3 of the CLK register while the clock multiplier is stabilizing.
   — When bit 3 of CLK is set to 1, go to step 3.

   If the external clock source is 48 MHz, do not enable the clock multiplier.
3. Enable any module of the chip.

### 7.2.3 SCC1 and SCC2 Power-Up

The clock signal to the SCCs is controlled by the FER and PTR configuration registers.

To restore the clock signal to one or both SCCs, the following must both be true:

- The appropriate enable bits, bits 2 and 1 of FER for SCC2 and SCC1, respectively must be set to 1.
- The power-down bit, bit 0 of PTR, must be 0.

If the on-chip clock multiplier stopped, allow time (maximum 2.4 msec) for multiplier stabilization before sending any data or signaling that the receiver channel is ready. The stabilization period can be sensed by reading the Main Status Register in the FDC, if the FDC is being powered up. (The Request for Master bit (RQM) is not set for approximately 2.4 msec). If the FDC is not powered up but, either one of the SCCs is being powered up, then, software must generate a delay of 2.4 msec. Stabilization of multiplier can also be sensed by putting any of the enabled SCCs into local loopback mode and sending bytes until they are received correctly.

### 7.2.4 FDC Power-Up

The clock signal to the FDC is controlled by the configuration registers, the FDC MODE command and the Data Rate Select Register (DSR).

To restore the clock signal to the FDC, both of the following conditions must be true:

- Bit 3 of FER must be set to 1.
- The power-down bit, bit 0 of PTR, must be 0.

In addition to these conditions, do one of the following to initiate the recovery from power-down mode:

- Read the Main Status Register (MSR) until the RQM bit, bit 7, is set to 1.
- Set the software reset bit, bit 7 or the Data Rate Select Register (DSR), to 1.
- Write the following to the reset bit, bit 2 or the Digital Output Register (DOR):
  — Set it to 1.
  — Clear it to 0.
- Read the Data Register and the Main Status Register until the RQM bit is set to 1.

# 8.0 Device Description

## 8.1 GENERAL ELECTRICAL CHARACTERISTICS

### 8.1.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | -0.5V to + 7.0V |
| Input Voltage ($V_I$) | -0.5 to $V_{DD}$ + 0.5V |
| Output Voltage ($V_O$) | -0.5 to $V_{DD}$ + 0.5V |
| Storage Temperature ($T_{STG}$) | -65°C to + 165°C |
| Power Dissipation ($P_D$) | 1W |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | +260°C |
| ESD Tolerance (Note 2) | *2000V min.* |
| $C_{ZAP}$ | 100 pF |
| $R_{ZAP}$ | 1.5 kΩ |

**Note 1:** Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.

**Note 2:** Value Based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

**Note 3:** Unless otherwise specified all voltages are referenced to ground.

### 8.1.2 Capacitance

**TABLE 108. Capacitance: $T_A$ 0°C to 70°C, $V_{DD}$ = 5V +/- 10% or 3.3V +/- 10%, $V_{SS}$ = 0V**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Pin Capacitance | | | 5 | 7 | pF |
| $C_{ICLK}$ | Clock Input Capacitance | | | 8 | 10 | pF |
| $C_{IO}$ | I/O Pin Capacitance | f = 1 MHz | | 10 | 12 | pF |
| $C_O$ | Output Pin Capacitance | f = 1 MHz | | 6 | 8 | pF |

### 8.1.3 Electrical Characteristics

**TABLE 109. Power Consumption**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | VDD Average Supply Current | VDD = 5V, VIL = 0.5V, VIH = 2.4V, No Load | | 20 | 50 | mA |
| | | VDD = 3.3V, VIL = 0.5V, VIH = 2.4V, No Load | | 12 | 35 | mA |
| $I_{CCSB}$ | VDD Quiescent Supply Current in Low Power Mode | VDD = 5V, VIL = 0.5V, VIH = 2.4V, No Load | | 400 | | µA |
| | | VDD = 3.3V, VIL = 0.5V, VIH = 2.4V, No Load | | 200 | | µA |

## 8.2 DC CHARACTERISTICS OF PINS, BY GROUP

The following tables list the DC characteristics of all device pins described in Section 1.2 on page 22. The pin list preceding each table lists the device pins to which the table applies.

### 8.2.1 Group 1

**PIN LIST:**

A15-0, AEN, BADDR1,0, $\overline{\text{CTS2,1}}$, $\overline{\text{DACK3-1}}$, $\overline{\text{DCD2,1}}$, $\overline{\text{DSR2,1}}$, ID2-0, IRRX2,1, MR, PD7-0, PNF, $\overline{\text{RD}}$, $\overline{\text{RI2,1}}$, SIN2,1, SIRQ31, TC, $\overline{\text{WAIT}}$, $\overline{\text{WR}}$

**TABLE 110. DC Characteristics of Group 1 Pins**

| Parameter | Symbol | Conditions | 5V | | | 3.3V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | Min | Typical | Max | |
| Input high voltage | $V_{IH}$ | | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Input low voltage | $V_{IL}$ | | -0.5 | | 0.8 | -0.5 | | 0.8 | V |
| Input leakage current | $I_{LKG}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | | 10<br>–10 | | | 10<br>-10 | µA<br>µA |
| Input hysteresis | $V_H$ | On PNF | | 250 | | | 200 | | mV |
| Input Hysteresis | $V_H$ | On SIRQI3 | | | 250 | | | 200 | mV |

### 8.2.2 Group 2

**PIN LIST:**

BUSY, PE, SLCT

**TABLE 111. DC Characteristics of Group 2 Pins**

| Parameter | Symbol | Conditions | 5V | | 3.3V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Input high voltage | $V_{IH}$ | | 2.0 | 5.5 | 2.0 | 5.5 | V |
| Input low voltage | $V_{IL}$ | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| Input leakage current | $I_{LKG}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | 100<br>–200 | | 100<br>-140 | µA<br>µA |

### 8.2.3 Group 3

**PIN LIST:**

$\overline{\text{ACK}}$, $\overline{\text{ERR}}$

**TABLE 112. DC Characteristics of Group 3 Pins**

| Parameter | Symbol | Conditions | 5V | | 3.3V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Input high voltage | $V_{IH}$ | | 2.0 | 5.5 | 2.0 | 5.5 | V |
| Input low voltage | $V_{IL}$ | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| Input leakage current | $I_{IL}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | 10<br>–200 | | 10<br>-140 | µA<br>µA |

### 8.2.4 Group 4

**PIN LIST:**

$\overline{DRV2}$, $\overline{DSCKCHG}$, $\overline{INDEX}$, MSEN1,0, $\overline{RDATA}$, $\overline{TRK0}$, $\overline{WP}$

**TABLE 113. DC Characteristics of Group 4 Pins**

| Parameter | Symbol | Conditions | 5V | | | 3.3V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typical | Max | Min | Typical | Max | |
| Input high voltage | $V_{IH}$ | | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Input low voltage | $V_{IL}$ | | -0.5 | | 0.8 | -0.5 | | 0.8 | V |
| Input leakage current | $I_{LKG}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | | 10<br>–10 | | | 10<br>-10 | µA<br>µA |
| Input hysteresis | $V_H$ | All pins (but $\overline{DRV2}$) | | 250 | | | 250 | | mV |
| Input Hysteresis | $V_H$ | On $\overline{DRV2}$ | | 250 | | | 200 | | mV |

### 8.2.5 Group 5

**PIN LIST:**

X1

**TABLE 114. DC Characteristics of Group 5 Pins**

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| XTAL1 input high voltage | $V_{IH}$ | | 2.0 | | V |
| XTAL1 input low voltage | $V_{IL}$ | | | 0.4 | V |
| XTAL1 leakage | $I_{XLKG}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | 400<br>-400 | µA |

### 8.2.6 Group 6

**PIN LIST:**

D7-0, DRQ3-0, IRQ15, IRQ12-9, IRQ7-3

**TABLE 115. DC Characteristics of Group 6 Input Pins**

| Parameter | Symbol | Conditions | 5V | | 3.3V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Input high voltage | $V_{IH}$ | | 2.0 | 5.5 | 2.0 | 5.5 | V |
| Input low voltage | $V_{IL}$ | | -0.5 | 0.8 | -0.5 | 0.8 | V |

**TABLE 116. DC Characteristics of Group 6 Output Pins**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | 5V | 3.3V | | | |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –15 mA | $I_{OH}$ = –7.5 mA | 2.4 | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 24 mA | $I_{OL}$ = 12 mA | | 0.4 | V |
| Input TRI-STATE leakage current | $I_{OZ}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | 50<br>-50 | µA<br>µA |

### 8.2.7 Group 7

**PIN LIST:**

BOUT2,1, $\overline{\text{DTR2,1}}$, $\overline{\text{RTS2,1}}$, SOUT2,1

**TABLE 117. DC Characteristics of Group 7 Pins**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | 5V | 3.3V | | | |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6 mA | $I_{OH}$ = –3 mA | 2.4 | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 12 mA | $I_{OL}$ = 6 mA | | 0.4 | V |

### 8.2.8 Group 8

**PIN LIST:**

$\overline{\text{CS1,0}}$, DRATE1,0

**TABLE 118. DC Characteristics of Group 8 Pins**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | 5V | 3.3V | | | |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6 mA | $I_{OH}$ = –3 mA | 2.4 | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6 mA | $I_{OL}$ = 3 mA | | 0.4 | V |

### 8.2.9 Group 9

These parameters apply only during reset. After reset, the pins in parentheses apply. See Group 7.

**PIN LIST:**

BADDR0 ($\overline{RTS1}$), BADDR1 (SOUT1), CFG0 (SOUT2)

**TABLE 119. DC Characteristics of Group 9 Pins**

| Parameter | Symbol | Conditions | 5V | | 3.3V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Input leakage current during reset | $I_{LKG}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | 150<br>-160 | | 150<br>-110 | µA<br>µA |
| Input high voltage | $V_{IH}$ | | 2.5 | 5.5 | 2.5 | 5.5 | |
| Input low voltage | $V_{IL}$ | | -0.5 | 0.8 | -0.5 | 0.8 | |

### 8.2.10 Group 10

**PIN LIST:**

ADRATE1,0, DENSEL, $\overline{DIR}$, $\overline{DR1,0}$, $\overline{DR23}$, $\overline{HDSEL}$, IDLE, $\overline{MRT1,0}$, PD, $\overline{STEP}$, $\overline{WDATA}$, $\overline{WGATE}$

**TABLE 120. DC Characteristics of Group 10 Pins**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | 5V | 3.3V | | | |
| High output voltage1 | $V_{OH}$ | $I_{OH}$ = –4 mA | $I_{OH}$ = –2 mA | 2.4 | | V |
| Low output voltage | $V_{OL}$ | $I_{OL}$ = 40 mA | $I_{OL}$ = 20mA | | 0.4 | V |
| High output leakage current [1] | $I_{LKG}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | 10<br>–10 | µA<br>µA |

Note 1. $V_{OH}$ for the floppy disk interface pins is valid for CMOS buffered output signals only.

### 8.2.11 Group 11

**PIN LIST:**

$\overline{AFD}$, $\overline{ASTRB}$, $\overline{DSTRB}$, $\overline{INIT}$, PD7-0, $\overline{SLIN}$, $\overline{STB}$, $\overline{WRITE}$

**TABLE 121. DC Characteristics of Group 11 Pins**

| Parameter | Symbol | Conditions | 5V | | 3.3V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| High level output current1 | $I_{OH}$ | $V_{OH}$ = 2.4 V | -14 | | -14 | | mA |
| Low level output current | $I_{OL}$ | $V_{OL}$ = 0.4 V | 14 | | 14 | | mA |

Note 1. When the Compatible or Extended modes, or EPP 1.7, or ECP mode 0, or ECP mode 2 and bit 1 of PCR is 0 for the parallel port are selected, pins $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$, and $\overline{STB}$ are open-drain support pins. 4.7 KΩ resistors should be used.

### 8.2.12 Group 12

**PIN LIST:**

IRSL2-0, IRTX

**TABLE 122. DC Characteristics of Group 12 Pins**

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = – 6 mA | 2.4 | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6 mA | | 0.4 | V |
| Output high current | $I_{OH}$ | $V_{OH} = V_{CC} - 0.2$ V | | –100 | µA |
| Output low current | $I_{OL}$ | $V_{OL}$ = 0.2 V | | 100 | µA |

### 8.2.13 Group 13

**PIN LIST:**

IOCHRDY, $\overline{ZWS}$

**TABLE 123. DC Characteristics of Group 13 Pins**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | 5V | 3.3V | | | |
| Output high voltage | $V_{OH}$ | TRI-STATE | TRI-STATE | | | |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 24 mA | $I_{OL}$ = 12 mA | | 0.4 | V |
| Input TRI-STATE leakage current | $I_{OZ}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | | 50<br>-50 | µA<br>µA |

## 8.3 AC ELECTRICAL CHARACTERISTICS

### 8.3.1 AC Test Conditions $T_A$ = 0° C to 70° C, $V_{DD}$ = 5.0 V ± 10%, 3.3 V ± 10%

- $C_L$ = 100 pF, includes jig and scope capacitance.
- $S_1$ = Open for push-pull output signals.
  $S_1 = V_{DD}$ for high impedance to active low and active low to high impedance measurements.
  $S_1$ = GND for high impedance to active high and active high to high impedance measurements.
  $R_L$ = 1.0 K¾ for uP interface pins.
- For the FDC open drive interface pins, $S_1 = V_{DD}$ and $R_L$ = 150¾.
- For 3V operation, it is recommended to connect all reset strap pins to CMOS input.

**FIGURE 89. Load Circuit**

## 8.4 SWITCHING CHARACTERISTICS

All the timing specifications given in this section refer to 0.8V and 2.0V on all the signals as illustrated in Figure 90, unless specifically stated otherwise.

**FIGURE 90. Testing Specification Standard**

### 8.4.1 Timing Table

$T_A$ = 0°C to 70°C, $V_{DD}$ = 5V +/- 10% or 3.3V +/- 10%, $V_{SS}$ = 0V

| Symbol | Figure | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **CLOCK TIMING** | | | | | | |
| $C_{FREQ}$ | | Clock Frequency | 14.318 MHz Nominal | 14.318 - 100 ppm | 14.318 + 100 ppm | MHz |
| | | | 24 MHz Nominal | 24 -100 ppm | 24+100 ppm | MHz |
| | | | 48 MHz Nominal | 48 -100 ppm | 48+100 ppm | MHz |
| $t_{CH}$ | Figure 91 | Clock High Pulse Width | 14.318 MHz Nominal | 26 | | ns |
| | | | 24 MHz Nominal | 16 | | ns |
| | | | 48 MHz Nominal | 16 | | ns |
| $t_{CL}$ | Figure 91 | Clock Low Pulse Width | 14.318 MHz Nominal | 8 | | ns |
| | | | 24 MHz Nominal | 8 | | ns |
| | | | 48 MHz Nominal | 8 | | ns |
| **CPU ACCESS TIMING** | | | | | | |
| $t_{AR}$ | Figure 92 | Address Valid to Read Active | | 15 | | ns |
| $t_{AW}$ | Figure 93 | Address Valid to Write Active | | 15 | | ns |
| $t_{AES}$ | Figures 92, 93 | AEN Signal Setup | | 15 | | ns |
| $t_{AEH}$ | Figures 92, 93 | AEN Signal Hold | | 5 | | ns |
| $t_{DH}$ | Figure 93 | Data Hold | | 2 | | ns |
| $t_{DS}$ | Figure 93 | Data Setup | | 18 | | ns |
| $t_{HZ}$ | Figure 92 | Data Bus Floating From Read Inactive | | | 25 | ns |
| $t_{RA}$ | Figure 92 | Address Hold from Read Inactive | | 1 | | ns |
| $t_{RRV}$ | Figure 92 | Read Cycle Recovery | | 45 | | ns |
| $t_{RD}$ | Figure 92 | Read Strobe Width | | 60 | 1000 | ns |
| $t_{RDH}$ | Figure 92 | Read Data Hold | | 10 | | ns |
| $t_{RDV}$ | Figure 92 | Data Valid From Read Active | | | 55 | ns |
| $t_{WA}$ | Figure 93 | Address Hold from Write Inactive | | 1 | | ns |
| $t_{WRV}$ | Figure 93 | Write Cycle Recovery | | 45 | | ns |
| $t_{WR}$ | Figure 93 | Write Strobe Width | | 60 | 1000 | ns |
| $t_{RI}$ | Figure 92 | IRQn Reset Delay from Read Inactive | | | 60 | ns |
| $t_{WI}$ | Figure 93 | IRQn Reset Delay from Write Inactive | | | 60 | ns |
| RC | Figure 92 | Read Cycle Time (RC > $t_{AR}$ + $t_{RD}$ + $t_{RRV}$) | | 123 | | ns |
| WR | Figure 93 | Write Cycle Time (WR > $t_{AW}$ + $t_{WR}$+ $t_{WRV}$) | | 123 | | ns |

| Symbol | Figure | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **DMA ACCESS TIMING** | | | | | | |
| $t_{DSW}$ | Figure 94 | Read or Write Signal Width | | 60 | 1000 | ns |
| $t_{DSQ}$ | Figure 94 | DRQ Inactive from Read or Write Active | | | 60 | ns |
| $t_{DKS}$ | Figure 94 | $\overline{DACK}$ Signal Setup | | 15 | | ns |
| $t_{DKH}$ | Figure 94 | $\overline{DACK}$ Signal Hold | | 0 | | ns |
| $t_{TCS}$ | Figure 94 | TC Signal Setup | | 60 | | ns |
| $t_{TCH}$ | Figure 94 | TC Signal Hold from Read or Write Inactive | | 2 | | ns |
| **UART AND INFRARED INTERFACE TIMING** | | | | | | |
| $t_{CMW}$ | Figure 95 | Modulation Signal Pulse Width in Sharp-IR and CEIR | Transmitter | $t_{CWN}$ -25ns (Note 1) | $t_{CWN}$ +25ns | |
| | | | Receiver | 500 | | ns |
| $t_{CMP}$ | Figure 95 | Modulation Signal Period in Sharp-IR and CEIR | Transmitter | $t_{CPN}$ -25 ns (Note 2) | $t_{CPN}$ +25 ns | |
| | | | Receiver | $t_{MMIN}$ (Note 3) | $t_{MMAX}$ | |
| $t_{BT}$ | Figure 95 | Single Bit Time in UART and Sharp-IR | Transmitter | $t_{BTN}$ - 25 ns (Note 4) | $t_{BTN}$ + 25 ns | |
| | | | Receiver | $t_{BTN}$ - 2% | $t_{BTN}$ + 2% | |
| $S_{DRT}$ | — | SIR Data Rate Tolerance. Percent of Nominal Data Rate. | Transmitter | | +/- 0.87% | |
| | | | Receiver | | +/- 2.0% | |
| $t_{SJT}$ | — | SIR Leading Edge Jitter. Percent of Nominal Bit Duration. | Transmitter | | +/- 2.5% | |
| | | | Receiver | | +/- 6.0% | |
| $t_{SPW}$ | Figure 96 | SIR Pulse Width | Transmitter, Variable Width | (3/16) x $t_{BTN}$ -15 ns (Note 4) | (3/16) x $t_{BTN}$ +15 ns | |
| | | | Transmitter, Fixed Width | 1.48 | 1.78 | µs |
| | | | Receiver | 1 µs | (1/2) x $t_{BTN}$ | |
| $M_{DRT}$ | — | MIR Data Rate Tolerance. Percent of Nominal Data Rate. | Transmitter | | +/- 0.1% | |
| | | | Receiver | | +/- 0.15% | |
| $t_{MJT}$ | — | MIR Leading Edge Jitter. Percent of Nominal Bit Duration. | Transmitter | | +/- 2.9% | |
| | | | Receiver | | +/- 6.0% | |
| $t_{MPW}$ | Figure 96 | MIR Pulse Width | Transmitter | $t_{MWN}$ - 15ns (Note 5) | $t_{MWN}$ + 15 ns | |
| | | | Receiver | 60 ns | (1/2) x $t_{BTN}$ (Note 4) | |

| Symbol | Figure | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{DRT}$ | — | FIR Data Rate Tolerance. Percent of Nominal Data Rate. | Transmitter | | +/- 0.01% | |
| | | | Receiver | | +/- 0.01% | |
| $t_{FJT}$ | — | FIR Leading Edge Jitter. Percent of Nominal Chip Duration. | Transmitter | | +/- 4.0% | |
| | | | Receiver | | +/- 25.0% | |
| $t_{FPW}$ | Figure 96 | FIR Single Pulse Width (Note 6) | Transmitter | 115 | 135 | ns |
| | | | Receiver, Leading Edge Jitter = 0 ns | 80 | 175 | ns |
| | | | Receiver, Leading Edge Jitter = +/- 25 ns | 90 | 150 | ns |
| $t_{DPW}$ | Figure 96 | FIR Double Pulse Width (Note 6) | Transmitter | 115 | 135 | ns |
| | | | Receiver, Leading Edge Jitter = 0 ns | 205 | 300 | ns |
| | | | Receiver, Leading Edge Jitter = +/- 25 ns | 215 | 310 | ns |
| $t_{WOD}$ | Figure 97 | $\overline{RTS}$, $\overline{DTR}$ and IRSLn Output Delay From Write Inactive | | | 40 | ns |
| $t_{MDO}$ | Figure 98 | Delay from $\overline{WR}$ ($\overline{WR}$ MCR) to output. | | | 40 | ns |
| $t_{HL}$ | Figure 98 | $\overline{RI2, 1}$ High-to-Low Transition | | 10 | | ns |
| $t_{RIM}$ | Figure 98 | Delay to Reset IRQ From $\overline{RD}$ (MSR) | | | 78 | ns |
| $t_{SIM}$ | Figure 98 | Delay to Reset IRQ From Modem Input | | | 40 | ns |
| **FLOPPY DISK CONTROLLER TIMING** | | | | | | |
| $t_{HDS}$ | Figure 99 | $\overline{HDSEL}$ Signal Setup | | | 100 | µs |
| $t_{HDH}$ | Figure 99 | $\overline{HDSEL}$ Signal Hold | | | 750 | µs |
| $t_{WDW}$ | Figure 99 | | 1 Mbps | 250 | | ns |
| | | | 500 kbps | 250 | | ns |
| | | | 300 kbps | 375 | | ns |
| | | | 250 kbps | 500 | | ns |
| $t_{DRV}$ | Figure 101 | DR3-0, MTR3-0 Signals Delay from WR Inactive | | | 110 | ns |
| $t_{DST}$ | Figure 101 | DIR Signal Setup to $\overline{STEP}$ Active | | 6 | | µs |
| $t_{IW}$ | Figure 101 | Index Pulse Width | | 100 | | ns |
| $t_{STR}$ | Figure 101 | $\overline{STEP}$ Signal Rate Time (See Table 3-2) | | 1 | | ms |
| $t_{STP}$ | Figure 101 | $\overline{STEP}$ Signal Pulse Width | | 8 | | µs |
| $t_{STD}$ | Figure 101 | $\overline{DIR}$ Signal Hold From $\overline{STEP}$ Inactive | | tSTR | | ms |
| $t_{RDW}$ | Figure 100 | Read Data Signal Pulse Width | | 50 | | ns |
| **PARALLEL PORT TIMING ( COMPATIBLE AND EXTENDED MODES)** | | | | | | |
| $t_{PIB}$ | Figure 103 | Parallel Port Interrupt Active | | 33 | | ns |
| $t_{PIE}$ | Figure 103 | Parallel Port Interrupt Inactive | | 33 | | ns |
| $t_{BLSL}$ | Figure 104 | BUSY Signal Low to $\overline{STB}$ Low | | 0 | | ns |

| Symbol | Figure | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{DSSL}$ | Figure 104 | Data Stable to $\overline{STB}$ Low | 750 | | ns |
| $t_{STBW}$ | Figure 104 | $\overline{STB}$ Signal Width | 750 | 500,000 | ns |
| $t_{SHDC}$ | Figure 104 | $\overline{STB}$ Signal High to Data Change | 750 | | ns |
| $t_{SLBH}$ | Figure 104 | $\overline{STB}$ Signal Low to BUSY High | | 500 | ns |
| $t_{SHNL}$ | Figure 104 | $\overline{STB}$ Signal High to ACK Low | 0 | | ns |
| $t_{ACKW}$ | Figure 104 | $\overline{ACK}$ Signal Width | 500 | 10,000 | ns |
| $t_{AHBL}$ | Figure 104 | $\overline{ACK}$ Signal High to BUSY Low | 0 | | ns |
| $t_{AHSL}$ | Figure 104 | $\overline{ACK}$ Signal High to $\overline{STB}$ Low | 0 | | ns |
| **PARALLEL PORT TIMING ( EPP 1.7 AND EPP 1.9 MODES)** | | | | | |
| $t_{WW}$ | Figures 105, 106 | $\overline{WRITE}$ Signal Delay After WR | | 45 | ns |
| $t_{WST}$ | Figures 105, 106 | $\overline{DSTRB}$ or $\overline{ASTRB}$ Delay After WR or RD (Note 7) | | 45 | ns |
| $t_{WST7}$ | Figures 105, 106 | $\overline{DSTRB}$ or $\overline{ASTRB}$ Active After WRITE Active | 0 | | ns |
| $t_{WPD7}h$ | Figures 105, 106 | PD7-0 Hold After $\overline{WRITE}$ Inactive | 50 | | ns |
| $t_{HRW}$ | Figures 105, 106 | IOCHRDY Signal Delay After $\overline{WR}$, $\overline{RD}$ or $\overline{WAIT}$ | | 40 | ns |
| $t_{WPDS}$ | Figures 105, 106 | PD7-0 Valid After $\overline{WRITE}$ Active (Note 8) | | 15 | ns |
| $t_{EPDW}$ | Figures 105, 106 | PD7-0 Valid Time | 80 | | ns |
| $t_{EPDh}$ | Figures 105, 106 | PD7-0 Hold After $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive | 0 | | ns |
| $t_{ZWSa}$ | Figures 105, 106 | $\overline{ZWS}$ Valid After $\overline{WR}$ or $\overline{RD}$ Active | | 45 | ns |
| $t_{ZWSh}$ | Figures 105, 106 | $\overline{ZWS}$ Hold After $\overline{WR}$ or $\overline{RD}$ Inactive | 0 | | ns |
| $t_{WWa}$ | Figures 105, 106 | $\overline{WRITE}$ Active From $\overline{WR}$ Active or $\overline{WAIT}$ Low | | 45 | ns |
| $t_{WWia}$ | Figures 105, 106 | $\overline{WRITE}$ Inactive From $\overline{WAIT}$ Low | | 45 | ns |
| $t_{WSTa}$ | Figures 105, 106 | $\overline{DSTRB}$ or $\overline{ASTRB}$ Active From $\overline{WR}$ or $\overline{RD}$ Active or WAIT Low (Notes 7, 9) | | 65 | ns |
| $t_{WSTia}$ | Figures 105, 106 | $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive From WR or RD High | | 45 | ns |
| $t_{WEST}$ | Figures 105, 106 | $\overline{DSTRB}$ or $\overline{ASTRB}$ Active After $\overline{WRITE}$ Active | 10 | | ns |
| $t_{WPDh}$ | Figures 105, 106 | PD7-0 Hold After $\overline{WRITE}$ Inactive | 0 | | ns |
| **PARALLEL PORT TIMING (ECP MODE)** | | | | | |
| $t_{ECDS}$ | Figures 107, 108 | PD7-0, $\overline{AFD}$ or BUSY Setup | 0 | | ns |
| $t_{ECDH}$ | Figures 107, 108 | PD7-0, $\overline{AFD}$ or BUSY Hold | 0 | | ns |
| $t_{ECLH}$ | Figures 107, 108 | BUSY or $\overline{AFD}$ Delay After $\overline{STB}$ or $\overline{ACK}$ Active | 75 | | ns |
| $t_{ECHH}$ | Figures 107, 108 | $\overline{STB}$ or $\overline{ACK}$ Active After $\overline{BUSY}$ or $\overline{AFD}$ Rising Edge | 0 | 1 | s |

| Symbol | Figure | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{ECHL}$ | Figures 107, 108 | BUSY or $\overline{AFD}$ Delay After $\overline{STB}$ or $\overline{ACK}$ Inactive | 0 | 35 | ms |
| $t_{ECLL}$ | Figures 107, 108 | $\overline{STB}$ or $\overline{ACK}$ Active After BUSY or $\overline{AFD}$ Falling Edge | 0 | | ns |
| **MISCELLANEOUS TIMING** | | | | | |
| $t_{ISS}$ | Figure 109 | IRQn Signal Delay From SIRQI1,2,3 | | 25 | ns |
| $t_{CSD}$ | Figure 110 | CS1-0 Signals Delay From A15-0, $\overline{WR}$ and $\overline{RD}$ | | 25 | ns |
| $t_{MRW}$ | Figure 111 | Master Reset Pulse Width | 22 | | µs |
| $t_{MRF}$ | Figure 111 | Output Signals Floating From Reset Active | | 700 | ns |
| $t_{MRCia}$ | Figure 111 | Output Signals Inactive From Reset Active | | 300 | ns |

**Note 1:** $t_{CWN}$ is the nominal pulse width of the modulation signal for Sharp-IR and CEIR modes. It is determined by the MCPW [2-0] and TXHSC bits in the IRTXMC and RCCFG registers.

**Note 2:** $t_{CPN}$ is the nominal period of the modulation signal for Sharp-IR and CEIR modes. It is determined by the MCFR [4-0] and TXHSC bits in the IRTXMC and RCCFG registers.

**Note 3:** $t_{MMIN}$ and $t_{MMAX}$ define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the content of register IRRXDC and the setting of bit RXHSC in the RCCFG register.

**Note 4:** $t_{BTN}$ is the nominal bit time in UART, Sharp-IR, SIR, MIR and CEIR modes.

**Note 5:** $t_{MWN}$ is the nominal pulse width for MIR mode. It is determined by the MPW [3-0] and MDRS bits in the MIR_PW and IRCR2 registers.

**Note 6:** The receiver pulse width requirements for various jitter values can be obtained by assuming a linear pulse-width/jitter relationship. For example, if the jitter is +/- 10 ns, the width of a single pulse must fall between 84 and 165 ns.

**Note 7:** The $\overline{WRITE}$ Signal will not change from low to high before $\overline{DSTRB}$ or $\overline{ASTRB}$ changes from low to high.

**Note 8:** D7-0 is assumed to be valid 15 ns or more before WR becomes active.

**Note 9:** When $\overline{WAIT}$ is low, $t_{WSTa}$ and $t_{WWa}$ are measured from the high-to-low transition of $\overline{WR}$ or $\overline{RD}$; otherwise they are measured from the high-to-low transition of $\overline{WAIT}$.

## 8.4.2 Timing Diagrams

**FIGURE 91. Clock Timing**

**FIGURE 92. CPU Read Timing**

**FIGURE 93. CPU Write Timing**

**FIGURE 94. DMA Access Timing**

**FIGURE 95. UART, Sharp-IR and CEIR Timing**

**Note**: The signals shown here represent the infrared signals at the IRTX output. The infrared signals at the IRRXn inputs have opposite polarity.

**FIGURE 96. SIR, MIR and FIR Timing**

**FIGURE 97. IRSLn Write Timing**

Notes
1. See write cycle timing, Figure 8-5
2. See read cycle timing, Figure 8-4

**FIGURE 98. Modem Control Timing**

**FIGURE 99. FDC Write Data Timing**

**FIGURE 100. FDC Read Data Timing**

**FIGURE 101. FDC Control Signals Timing**

**FIGURE 102. Parallel Port Interrupt Timing (Compatible Mode)**

**FIGURE 103. Parallel Port Interrupt Timing (Extended Mode)**

**FIGURE 104. Parallel Port Data Transfer Timing (Compatible Mode)**

**FIGURE 105. Parallel Port Data Transfer Timing (EPP 1.7 Mode)**

**FIGURE 106. Parallel Port Data Transfer Timing (EPP 1.9 Mode)**

**FIGURE 107. Parallel Port Forward Transfer Timing (ECP Mode)**

**FIGURE 108. Parallel Port Reverse Transfer Timing (ECP Mode)**

**FIGURE 109. System Interrupts Timing**

**FIGURE 110. CS1-0 Signals Timing**

**FIGURE 111. Reset Timing**

## Appendix A

## Comparison of PC87338 and PC97338

| Module | PC87338 | PC97338 |
|---|---|---|
| Configuration | Updating a Configuration Register requires two consecutive write accesses to the Data Register, and the CPU interrupts must be disabled during the write cycle. | Updating a Configuration Register requires a single write to the Data Register, and the CPU interrupts do not need to be disabled. |
| | The MIDI baud rate (pre-scale of 12 instead of 13) is configured by TUP3 as follows:<br>TUP3: 0 - Pre-scale divides the clock by 13<br>TUP3: 1 - Pre-scale divides the clock by 12 (for MIDI) | TUP3 is reserved. Programming the UART to MIDI baud rate is accomplished by programming the pre-scale to 1, and the baud rate divisor to a number that is 12 times its value in the PC87338. |
| | SuperI/O Chip Configuration Register 2 (SCF2) bit 4 is reserved:<br>Bit 4: Reserved | SuperI/O Chip Configuration Register 2 (SCF2) bit 4 value is:<br>Bit 4: SCC1 Bank Select Enable |
| | No Manufacturing Test Register. | Includes a new register, the Manufacturing Test Register (MTEST), Index 52h. |
| FDC | No FM mode support. | Supports FM mode. |
| NPP | The output of the control signals are at level 2 (push-pull) in:<br>- EPP1.9 mode<br>- ECP mode 011<br>- ECP mode 010 and PCR[1]=1 | The output of the control signal are at level 2 (push-pull) in:<br>- EPP mode<br>- All ECP modes except 000 |
| | DCR5 is a read only bit (return 0) in ECP modes 000 and 010. In all other ECP modes, DCR5 is a read/write bit. | DCR5 is a read/write bit in all ECP modes. |
| | CTR2 is 0 after reset (activate $\overline{\text{INIT}}$ signal to initialize the printer). | CTR2 is 1 after reset, so the printer remains in ECP mode if it was programmed to this mode and not initialized to SPP mode. |
| UART** and IR | The baud rate generator is not initialized on power-up. | MR signal resets the baud rate generator register on power-up. |
| | In loopback mode, the data is not projected on SOUT1,2 pins. | In loopback mode, the data is projected on SOUT1,2 pins. |
| | No ID pin. | IRSL0-2 is multiplexed with ID0-2 |

** In the PC87338 and PC97338, BOUT1 is multiplexed with SOUT1; BOUT2 is multiplexed with DRT2.

## Glossary

**11-bit address mode**

In this mode, the Chip decodes address lines A0-A10, A11-A15 are masked to 1, and UART2 is a fully featured 16550 UART. The mode is configured during reset, via the CFG0 strap pin.

**16-bit address mode**

In this mode, the Chip decodes address lines A0-A15 and SCC2 is a 16550 UART with SIN2/SOUT2 interface signals only. The mode is configured during reset, via the CFG0 strap pin.

**AFIFO**

Address FIFO for the parallel port in Extended Capabilities Port mode.

**ASC**

The register that configures the Advanced Super I/O chip, i.e., the PC87338/VLJ or the PC87338VJG.

**ASK-IR**

Amplitude Shift Keying Infrared.

**BGD(H) and BGD(L)**

Baud Generator Divisor Ports (High and Low bytes) for the SCCs.

**BSR**

Bank Selection Register for the SCCs.

**CCR**

Configuration Control Register of the Floppy Disk Controller (FDC).

**CFIFO**

Parallel port data FIFO in Extended Capabilities Port (ECP) mode.

**CNFGA and CNFGB**

Configuration registers A and B for the parallel port in Extended Capabilities Port mode.

**CEIR Mode**

This IR mode supports all four protocols currently used in remote-controlled home entertainment equipment. Also called TV-Remote mode.

**CS0HA**

The Chip Select 0 High Address register.

**CS0LA**

The Chip Select 0 Low Address register.

**CS1CF**

The Chip Select 1 Configuration register.

**CS1HA**

The Chip Select 1 High Address register.

**CS1LA**

The Chip Select 1 Low Address register.

**CTR**

Control Register of the parallel port.

**DASK-IR**

Digital Amplitude Shift Keying Infrared.

**Data**

The Data register contains the data in the register indicated by the corresponding Index register.

**DATAR**

Data Register for the parallel port in Extended Capability Port mode.

**DCR**

Data Control Register for the parallel port in Extended Capabilities Port mode.

**Device**

Any circuit that performs a specific function, such as a parallel port.

**DIR**

Digital Input Register of the Floppy Disk Controller (FDC).

**DOR**

Digital Output Register of the Floppy Disk Controller (FDC).

**DSR**

Data rate Select Register of the Floppy Disk Controller (FDC) and the data Status Register in Extended Capabilities Port mode.

**DTR**

Data Register of the parallel port.

**EAR**

Extended Auxiliary Register of the parallel port in Extended Capabilities Port (ECP) modes.

**ECP**

Extended Capabilities Port.

**ECR**

Extended Control Register for the parallel port in Extended Capabilities Port mode.

**EDR**

Extended Data Register for the parallel port in extended Capabilities Port (ECP) modes.

**EIR**

Two expressions:

Extended Index Register of the parallel port Extended Capabilities Port (ECP) modes.

Event Identification Register for SCC1 and SCC2 for read cycles.

**EPP**

Enhanced Parallel Port.

**FAR**

The Function Address configuration Register.

**FBAH**

The register that holds the High byte of the Base Address of the Floppy Disc Controller (FDC).

**FBAL**

The register that holds the Low byte of the Base Address of the Floppy Disk Controller (FDC).

**FCR**

The Function Control configuration Register or the FIFO Control Register for SCCs.

**FDC**

Floppy Disk Controller.

**FER**

The Function Enable configuration Register.

**FIFO**

Data register (FIFO queue) of the Floppy Disk Controller (FDC)

**IER**

The Interrupt Enable Register for the SCCs.

**Index**

The Index register is a pointer that is used to address other registers.

**IR**

Infrared.

**IRCFG1, IRCFG3 and IRCFG4**

Infrared module Configuration registers for the SCC2.

**IRCR1, IRCR2 and IRCR3**

Infrared Module Control Registers 1, 2 and 3 for the SCC2.

**IrDA**

Infrared Data Association.

**IrDA mode**

In this mode, the Chip provides the Infrared Data Association standard compliant interface.

**IRQ**

Interrupt Request.

**IRRXDC**

Infrared Receiver Demodulator Control register for the SCC2.

**IRTXMC**

Infrared Transmitter Modulator Control register for the SCC2.

**ISA**

Industry Standard Architecture.

**LBGD(H) and LBGD(L)**

Legacy Baud rate Generator Divisor port (High and Low bytes) for the SCC2.

**LCR**

Line Control Register for SCCs.

**Legacy**

A colloquial description usually referring to older devices or systems that are not Plug and Play compatible.

**Legacy mode**

In this mode, the interrupts and the base addresses of the FDC, SCC1, SCC2 and the parallel port of the Chip are configured as in earlier SuperI/O chips. This mode is configured via bit 3 of Plug and Play configuration register 0 (PNP0).

**LFSR**

The Linear Feedback Shift Register. In Plug and Play mode, this register is used to prepare the chip for operation in Plug and Play (PnP) mode.

**LSR**

Line Status Register for SCCs.

**MCR**

Modem Control Register for SCCs.

**MRID**

Module Revision ID register for the SCC2.

**MSR**

Main Status Register of the Floppy Disk Controller (FDC) or Modem Status Register for SCCs.

**Non-Extended UART Operation Modes**

These UART operation modes support only UART operations that are standard for 15450 or 16550A devices.

**PBAH**

The register that holds the High byte of the Base Address of the Parallel port.

**PBAL**

The register that holds the Low byte of the Base Address of the Parallel port.

**PCR**

The Parallel port Control configuration Register.

**Plug and Play (PnP)**

A design philosophy and a set of specifications that describe hardware and software changes to the PC and its peripherals that automatically identify and arbitrate resource requirements among all devices and buses on the system.

**PMC**

The Power Management Control configuration register.

**PnP**

Plug and Play.

**PnP mode**

In this mode, the interrupts, the DMA channels and the base address of the FDC, SCC1, SCC2 and the Parallel Port of the Chip are fully plug and play. This mode is configured via bit 3 of Plug and Play configuration register 0 (PNP0).

**PNP0, PNP1 and PNP2**

Plug and Play configuration registers 0 through 2.

**P_MDR**

Pipeline Mode Register for SCCs.

**PIO**

Programmable Input/Output.

**ppm**

Parts per million.

**PPM**

Parallel Port Multiplexor or Multiplexed.

**PPM mode**

In this mode, the Parallel Port pins of the chip serve as FDC pins.

**Precompensation**

Also called write precompensation, is a way of preconditioning the $\overline{\text{WDATA}}$ output signal to adjust for the effects of bit shift on the data as it is written to the disk surface.

**PTR**

The Power and Test configuration Register.

**RSR**

The Receiver Shift Register for SCCs. This register if for internal use only.

**SBAH**

The register that holds the High byte of the Base Address, of the Super I/O chip.

**SBAL**

The register that holds the Low byte of the Base Address, of the Super I/O chip.

**SCCs**

Serial Communciation Controllers.

**SCF0, SCF1 and SCF2**

The Configuration registers that configure the Super I/O chip.

**SCR**

Scratch Register for SCCs.

**SH_LCR**

Shadow of the Line Control Register (LCR) for the SCC2 for read operations.

**SHARP-IR**

SHARP Infrared.

**SHARP-IR mode**

In this mode, the Chip provides SHARP Infrared interface. This mode is configured via the IRC register.

**SID**

Super I/O ID, the configuration register that holds the identity of the Super I/O chip.

**SIO**

Super I/O, sometimes used to refer to a chip that has Super I/O capabilities.

**SIR**

Serial Infrared.

**SIR_PW**

SIR Pulse Width control for the SCC2.

**SIRQ1, SIRQ2 and SIRQ3**

These configuration registers describe the SIRQI1, SIRQI2 and SIRQI3 functions, which determine how Interrupt Requests are handled.

**SPP**

The Standard Parallel Port configuration of the Parallel Port device supports the Compatible SPP mode and the Extended PP mode.

**SRA and SRB**

Status Registers A and B of the Floppy Disk Controller (FDC).

**ST0, ST1, ST2 and ST3**

Status registers 0, 1, 2 and 3 of the Floppy Disk Controller (FDC).

**STR**

Status Register of the parallel port.

**TDR**

Tape Drive Register of the Floppy Disk Controller (FDC).

**TFIFO**

Test FIFO for the parallel port in Extended Capabilities Port mode.

**TXDR**

The Transmitter Data Register for SCCs.

**TUP**

The Tape drive, SCCs, Parallel port configuration register.

**S1BAH**

The configuration register that holds the High byte of the Base Address of SCC1.

**S1BAL**

The configuration register that holds the Low byte of the Base Address of SCC1.

**S2BAH**

The configuration register that holds the High byte of the Base Address of SCC2.

**S2BAL**

The configuration register that holds the Low byte of the Base Address of SCC2.

**UART**

Universal Asynchronous Receiver Transmitter.

## Physical Dimensions millimeters

Plastic Quad Flatpack (PQFP), EIAJ
Order Number PC87338/PC97338(VLJ)
NS Package Number VLJ100A

## Physical Dimensions millimeters

Thin Quad Flatpack (TQFP), JEDEC)
Order Number PC87338/PC97338(VJG)
NS Package Number VJG100A

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