National Semiconductor

PRELIMINARY
May 1995

PC87332VLJ (3.3V/5V) and PC87332VLJ-5 (5V) (SuperI/O™ III Premium Green) Floppy Disk Controller, Dual UARTs, IEEE1284 Parallel Port, and IDE Interface

General Description

The PC87332VLJ and PC87332VLJ-5 are single chip solutions for most commonly used I/O peripherals in ISA, EISA and MicroChannel® based computers. It incorporates a Floppy Disk Controller (FDC), two full featured UARTs, an IEEE 1284 compatible parallel port and all the necessary control logic for an IDE interface. Standard PC-AT® address decoding for all the peripherals and a set of configuration registers are also implemented in this highly integrated member of the SuperI/O family. Advanced power management features and mixed voltage operation in the VLJ version make the PC87332 chips an ideal for low-power and/or portable personal computer applications.

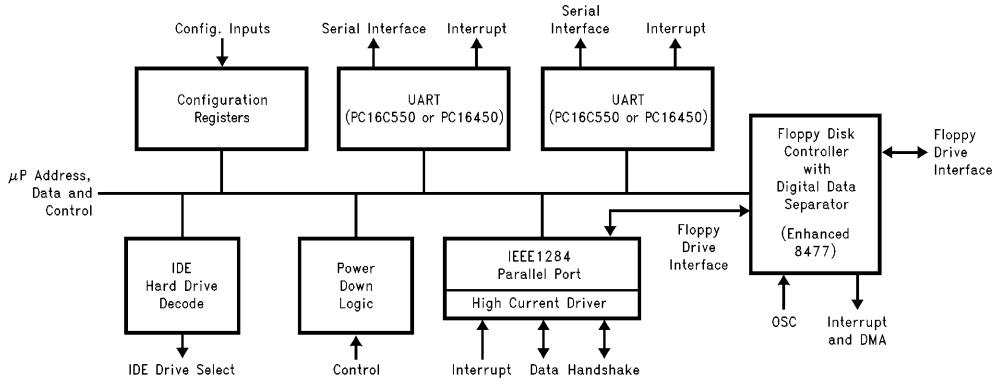
The PC87332 FDC uses a high performance digital data separator eliminating the need for any external filter components. It is fully compatible with the PC8477 and incorporates a superset of DP8473, NEC μPD765 and N82077 floppy disk controller functions. All popular 5.25″ and 3.5″ floppy drives, including the 2.88 MB 3.5″ floppy drive, are supported. In addition, automatic media sense and 2 Mbps tape drive support are provided by the FDC.

The two UARTs are fully NS16450 and NS16550 compatible. Both ports support MIDI baud rates. (Continued)

Features

- Floppy Disk Controller:
  - — Software compatible with the DP8473, the 765A and the N82077
  - — 16-byte FIFO (disabled by default)
  - — Burst and Non-Burst modes
  - — Perpendicular Recording drive support
  - — New high-performance internal digital data separator (no external filter components required)
  - — Low-power CMOS with enhanced power-down mode
  - — Automatic media-sense support
  - — Supports fast 2 Mbps and standard 1 Mbps/ 500 kbps/250 kbps tape drives
- Bidirectional Parallel Port:
  - — Enhanced Parallel Port (EPP) compatible
  - — Extended Capabilities Port (ECP) compatible, including level 2 support
  - — Bidirectional under either software or hardware control
  - — Ability to multiplex FDC signals on parallel port pins allows use of an external Floppy Disk Drive (FDD)
  - — Includes protection circuit to prevent damage to the parallel port when a connected printer is powered up or is operated at a higher voltage (Continued)

Block Diagram



TL/C/11930–1

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
SuperI/O™ is a trademark of National Semiconductor Corporation.
IBM®, MicroChannel®, PC-AT® and PS/2® are registered trademarks of International Business Machines Corporation.

©1995 National Semiconductor Corporation TL/C/11930

RRD-B30M65/Printed in U. S. A.

General Description (Continued)

The parallel port is fully IEEE 1284 level 2 compatible. The SPP (Standard Parallel Port) is fully compatible with ISA, EISA and MicroChannel parallel ports. In addition to the SPP, EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port) modes are supported by the parallel port.

All IDE control signals are provided by the PC87332. Only external signal buffers are required to implement a complete IDE interface.

A set of eight configuration registers are provided to control various functions of the PC87332. These registers are accessed using two 8-bit wide index and data registers. The ISA I/O address of the register pair can be relocated using a power-up strapping option.

When idle, advanced power management features allows the PC87332 to enter extremely low power modes under hardware or software control. The PC87332VLJ can operate from a 5V or a 3.3V power supply. An unique I/O cell structure allows the PC87332VLJ to interface directly with 5V external components while operating from a 3.3V power supply.

Features (Continued)

- UARTs:
  - — Software compatible with the PC16550A and PC16450
  - — MIDI baud rate support
- IDE Control Logic:
  - — All IDE control signals. Only external signal buffers required to implement full IDE interface
- Address Decoder:
  - — Provides selection of all primary and secondary ISA addresses including COM1–4 and LPTA–C
- Enhanced Power Management:
  - — Special configuration registers for power-down
  - — Enhanced programmable power-down FDC command
  - — Auto power-down and wake-up modes
  - — 3 special pins for power management
  - — Typical current consumption during power-down is less than 10 μA
  - — Reduced pin leakage current
- Mixed Voltage Support:
  - — Supports standard 5V operation
  - — Supports 3.3V operation
  - — Supports mixed internal 3.3V operation with 3.3V/5V external configuration
- General:
  - — 100% compatible with ISA, EISA, and MicroChannel architectures
  - — 100-Pin PQFP package is pin compatible with the PC87312 and PC87322VF

Table of Contents

1.0 PIN DESCRIPTION

2.0 CONFIGURATION REGISTERS

2.1 Overview
2.2 Software Configuration
2.3 Hardware Configuration
2.4 Index and Data Registers
2.5 Base Configuration Registers
2.5.1 Function Enable Register (FER)
2.5.2 Function Address Register (FAR)
2.5.3 Power and Test Register (PTR)
2.5.4 Function Control Register (FCR)
2.5.5 Printer Control Register (PCR)
2.5.6 Power Management Control Register (PMC)
2.5.7 Tape, UARTs and Parallel Port Configuration Register (TUP)
2.5.8 SIO Identification Register (SID)
2.6 Power-Down Options
2.6.1 Recommended Power-Down Methods—Group 1
2.6.2 Recommended Power-Down Methods—Group 2
2.7 Power-Up Procedure and Considerations
2.7.1 Crystal Stabilization
2.7.2 UART Power-Up
2.7.3 FDC Power-Up

3.0 FDC REGISTER DESCRIPTION

3.1 FDC Control Registers
3.1.1 Status Registger A (SRA) Read Only
3.1.2 Status Register B (SRB) Read Only
3.1.3 Digital Output Register (DOR) Read/Write
3.1.4 Tape Drive Register (TDR) Read/Write
3.1.5 Main Status Register (MSR) Read Only
3.1.6 Data Rate Select Register (DSR) Write Only
3.1.7 Data Register (FIFO) Read/Write
3.1.8 Digital Input Register (DIR) Read Only
3.1.9 Configuration Control Register (CCR) Write Only
3.2 Result Phase Status Registers
3.2.1 Status Register 0 (ST0)
3.2.2 Status Register 1 (ST1)
3.2.3 Status Register 2 (ST2)
3.2.4 Status Register 3 (ST3)

4.0 FDC COMMAND SET DESCRIPTION

4.1 Command Description
4.1.1 Configure Command
4.1.2 Dumpreg Command
4.1.3 Format Track Command
4.1.4 Invalid Command
4.1.5 Lock Command
4.1.6 Mode Command
4.1.7 NSC Command
4.1.8 Perpendicular Mode Command
4.1.9 Read Data Command
4.1.10 Read Deleted Data Command
4.1.11 Read ID Command
4.1.12 Read A Track Command
4.1.13 Recalibrate Command
4.1.14 Relative Seek Command
4.1.15 Scan Commands
4.1.16 Seek Command
4.1.17 Sense Drive Status Command
4.1.18 Sense Interrupt Command
4.1.19 Set Track Command
4.1.20 Specify Command
4.1.21 Verify Command
4.1.22 Version Command
4.1.23 Write Data Command
4.1.24 Write Deleted Data
4.2 Command Set Summary
4.3 Mnemonic Definitons for FDC Commands

5.0 FDC FUNCTIONAL DESCRIPTION

5.1 Microprocessor Interface
5.2 Modes of Operation
5.3 Controller Phases
5.3.1 Command Phase
5.3.2 Execution Phase
5.3.2.1 DMA Mode—FIFO Disabled
5.3.2.2 DMA Mode—FIFO Enabled
5.3.2.3 Interrupt Mode—FIFO Disabled
5.3.2.4 Interrupt Mode—FIFO Enabled
5.3.2.5 Software Polling
5.3.3 Result Phase
5.3.4 Idle Phase
5.3.5 Drive Polling Phase
5.4 Data Separator
5.5 Crystal Oscillator
5.6 Perpendicular Recording Mode
5.7 Data Rate Selection
5.8 Write Precompensation
5.9 FDC Low Power Mode Logic
5.10 Reset Operation

Table of Contents (Continued)

6.0 SERIAL PORTS

6.1 Serial Port Registers
6.2 Line Control Register (LCR)
6.3 Programmable Baud Rate Generator
6.4 Line Status Register (LSR)
6.5 FIFO Control Register
6.6 Interrupt Identification Register (IIR)
6.7 Interrupt Enable Register (IER)
6.8 MODEM Control Register (MCR)
6.9 MODEM Status Register (MSR)
6.10 Scratchpad Register (SCR)

7.0 PARALLEL PORT

7.1 Introduction
7.2 Data Register (DTR)
7.3 Status Register (STR)
7.4 Control Register (CTR)
7.5 Enhanced Parallel Port Operation
7.6 Extended Capabilities Parallel Port (ECP)
7.6.1 Introduction
7.6.2 Software Operation
7.7 Register Definitions
7.8 Software Controlled Data Transfer (Modes 000 and 001)
7.9 Automatic Data Transfer (Modes 010 and 011)
7.9.1 Forward Direction (Bit 5 of DCR = 0)
7.9.2 ECP (Forward) Write Cycle
7.9.3 Backward Direction (bit 5 of DCR is 1)
7.9.4 ECP (Backward) Read Cycle
7.10 FIFO Test Access (Mode 110)
7.11 Configuration Registers Access (Mode 111)
7.12 Interrupt Generation

8.0 INTEGRATED DEVICE ELECTRONICS INTERFACE (IDE)

8.1 Introduction
8.2 IDE Signals

9.0 ELECTRICAL CHARACTERISTICS

9.1 DC Electrical Characteristics
9.2 DC Electrical Characteristics
9.3 AC Electrical Characteristics
9.3.1 AC Test Conditions
9.3.2 Clock Timing
9.3.3 Microprocessor Interface Timing
9.3.4 Baud Out Timing
9.3.5 Transmitter Timing
9.3.6 Receiver Timing
9.3.7 MODEM Control Timing
9.3.8 DMA Timing
9.3.9 Reset Timing
9.3.10 Write Data Timing
9.3.11 Drive Control Timing
9.3.12 Read Data Timing
9.3.13 IDE Timing
9.3.14 Parallel Port Timing
9.3.15 Enhanced Parallel Port Timing
9.3.16 Extended Capabilities Port Timing

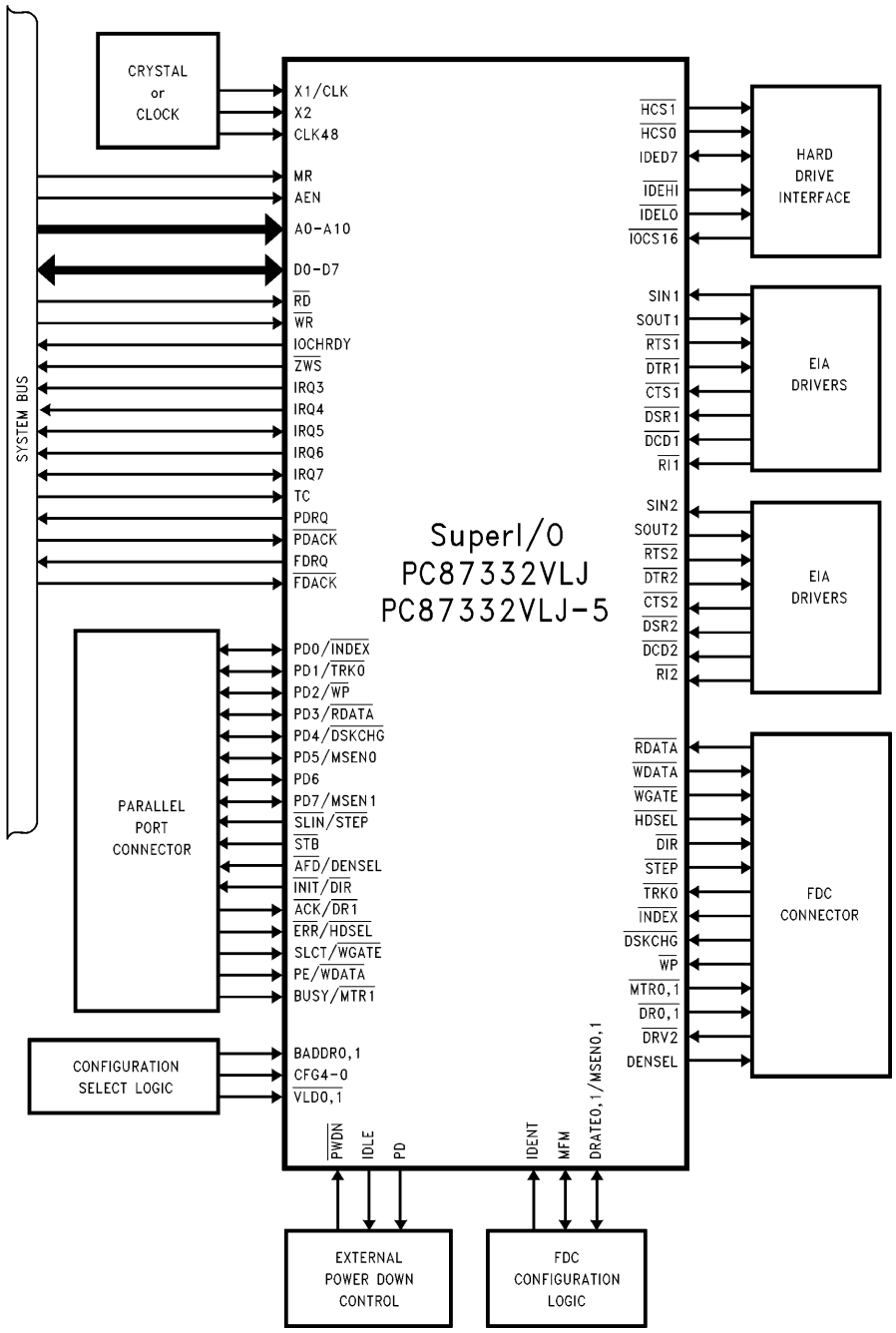
List of Figures

FIGURE 2-1 PC87332VLJ/PC87332VLJ-5 Configuration Registers
FIGURE 2-2 PC87332 Four Floppy Drive Circuit Example
FIGURE 3-1 FDC Functional Block Diagram
FIGURE 4-1 FDC Command Structure
FIGURE 4-2 IBM, Perpendicular, and ISO Formats Supported by the Format Command
FIGURE 5-1 PC87332 Dynamic Window Margin Performance
FIGURE 5-2 Read Data Algorithm—State Diagram
FIGURE 5-3 Perpendicular Recording Drive R/W Head and Pre-Erase Head
FIGURE 6-1 PC87332 Composite Serial Data
FIGURE 6-2 Reciever FIFO Trigger Level
FIGURE 7-1 EPP 1.7 Address Write
FIGURE 7-2 EPP 1.7 Address Read
FIGURE 7-3 EPP Write with ZWS
FIGURE 7-4 EPP 1.9 Address Write
FIGURE 7-5 EPP 1.9 Address Read
FIGURE 7-6 ECP (Forward) Write Cycle
FIGURE 7-7 ECP (Backward) Read Cycle
FIGURE 8-1 IDE Interface Signal Equations (Non-DMA)
FIGURE 9-1 Clock Timing
FIGURE 9-2 Microprocessor Read Timing
FIGURE 9-3 Microprocessor Write Timing
FIGURE 9-4 Baud Out Timing
FIGURE 9-5 Transmitter Timing
FIGURE 9-6a Sample Clock Timing
FIGURE 9-6b Receiver Timing
FIGURE 9-6c Mode Receiver Timing
FIGURE 9-6d Timeout Receiver Timing
FIGURE 9-7 MODEM Control Timing
FIGURE 9-8 DMA Timing
FIGURE 9-9 Reset Timing
FIGURE 9-10 Write Data Timing
FIGURE 9-11 Drive Control Timing
FIGURE 9-12 Read Data Timing
FIGURE 9-13 IDE Timing
FIGURE 9-14 Compatible Mode Parallel Port Interrupt Timing
FIGURE 9-15 Extended Mode Parallel Port Interrupt Timing
FIGURE 9-16 Typical Parallel Port Data Exchange
FIGURE 9-17 Enhanced Parallel Port Timing
FIGURE 9-18 ECP Parallel Port Forward Timing Diagram
FIGURE 9-19 ECP Parallel Port Backward Timing Diagram

List of Tables

TABLE 1-1 Pin Descriptions (Alphabetical)
TABLE 2-1 Default Configurations Controlled by Hardware
TABLE 2-2 Index and Data Register Optional Locations
TABLE 2-3 Encoded Drive and Motor Pin Information
TABLE 2-4 Primary and Secondary Drive Address Selection
TABLE 2-5 Parallel Port Addresses
TABLE 2-6 COM Port Selection for UART1
TABLE 2-7 COM Port Selection for UART2
TABLE 2-8 Address Selection for COM3 and COM4
TABLE 2-9 Logical Drive Exchange
TABLE 2-10 Parallel Port Mode
TABLE 2-11 Methods to Achieve Group 1 Power-Down Modes
TABLE 3-1 Register Description and Addresses
TABLE 3-2 Drive Enable Values
TABLE 3-3 Media ID Bit Functions
TABLE 3-4 Tape Drive Assignment Values
TABLE 3-5 Write Precompensation Delays
TABLE 3-6 Default Precompensation Delays
TABLE 3-7 Data Rate Select Encoding
TABLE 4-1 Typical Format Gap Length Values
TABLE 4-2 Typical Format GAP3 Length Values Based on PC Compatible Diskette Media
TABLE 4-3 DENSEL Default Encoding
TABLE 4-4 DENSEL Encoding
TABLE 4-5 Head Settle Time Calculation
TABLE 4-6 Effect of Drive Mode and Data Rate on Format and Write Commands
TABLE 4-7 Effect of GAP and WG on Format and Write Commands
TABLE 4-8 Sector Size Selection
TABLE 4-9 SK Effect on the Read Data Command
TABLE 4-10 Result Phase Termination Values with No Error
TABLE 4-11 SK Effect on the Read Deleted Data Command
TABLE 4-12 Maximum Recalibrate Step Pulses Based on R255 and ETR
TABLE 4-13 Scan Command Termination Values
TABLE 4-14 Status Register 0 Termination Codes
TABLE 4-15 Set Track Register Address
TABLE 4-16 Step Rate Time (SRT) Values
TABLE 4-17 Motor Off Time (MFT) Values
TABLE 4-18 Motor On Time (MNT) Values
TABLE 4-19 Verify Command Result Phase
TABLE 6-1 PC87332 UART Register Addresses (AEN = 0)
TABLE 6-2 PC87332 Register Summary for an Individual UART Channel
TABLE 6-3 PC87332 UART Reset Configuration
TABLE 6-4 PC87332 UART Divisors, Baud Rates and Clock Frequencies
TABLE 6-5 PC87332 Interrupt Control Functions
TABLE 7-1 Parallel Interface Register Addresses
TABLE 7-2 Standard Parallel Port Modes Selection
TABLE 7-3 SPP Data Register Read and Write Modes
TABLE 7-4 Parallel Port Reset States
TABLE 7-5 EPP Registers
TABLE 7-6 Parallel Port Pin Out
TABLE 7-7 ECP Registers Summary
TABLE 8-1 IDE Registers and Their ISA Addresses
TABLE 9-1 Nominal t_{ICP}, t_{DRP} Values
TABLE 9-2 Minimum t_{WDW} Values

Basic Configuration

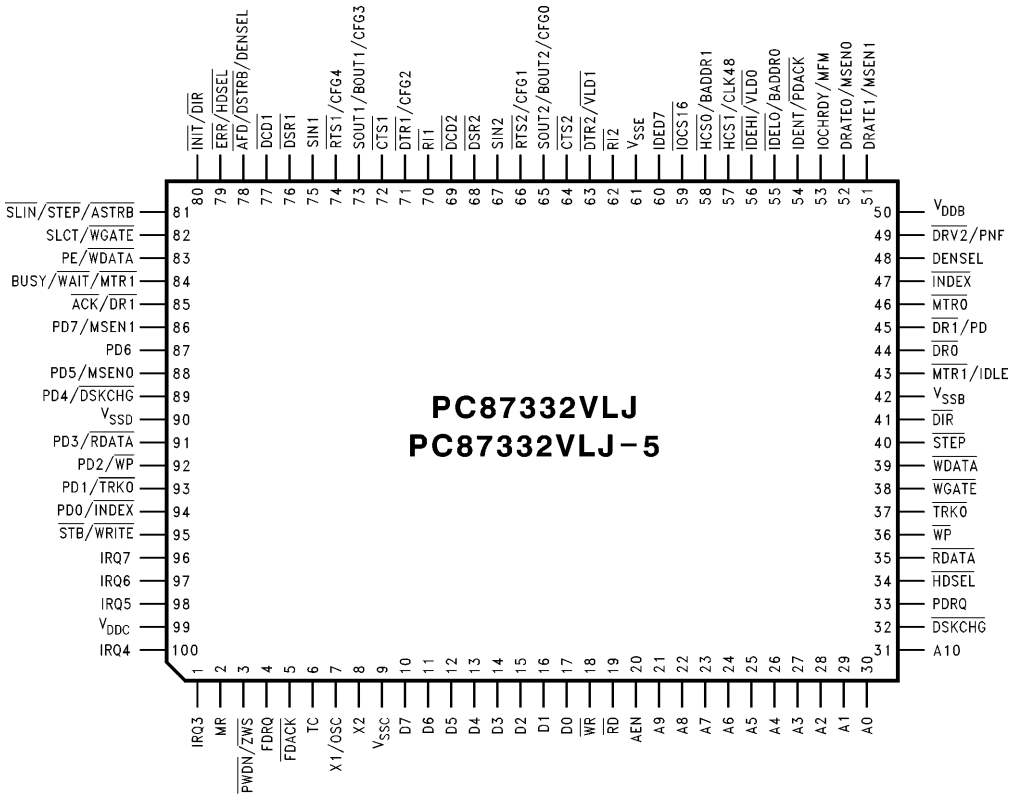


TL/C/11930–2

1.0 Pin Description

Connection Diagrams

Plastic Quad Flatpak (PQFP), EIAJ



TL/C/11930−3

Order Number PC87332VLJ or PC87332VLJ-5
See NS Package Number VLJ100A

1.0 Pin Description (Continued)

TABLE 1-1. Pin Descriptions (Alphabetical)

Symbol	Pin	I/O	Function
A10–A0	21–31	I	**Address.** These microprocessor address lines determine which internal register is accessed. A0–A10 are don't cares during a DMA transfer.
$\overline{ACK}$	85	I	**Acknowledge.** This input is pulsed low by a connected printer to indicate that it has received data from the parallel port. This pin has a nominal 25 kΩ pull-up resistor attached to it. (This pin is shared with $\overline{DR1}$. See Table 7-5 for further information.)
$\overline{AFD}$	78	I/O	**Automatic Feed XT.** When this signal is low the connected printer should automatically line feed after each line is printed. This pin is in a TRI-STATE® condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 kΩ resistor. (See $\overline{DSTRB}$ and Table 7-5 for further information.)
AEN	20	I	**Address Enable.** This input disables function selection via A10–A0 when it is high. Access during DMA transfer is NOT affected by this pin.
$\overline{ASTRB}$	81	O	**Address Strobe.** This signal is used in EPP mode as an address strobe. It is active low. (See $\overline{SLIN}$ and Table 7-5 for further information.)
BADDR0,1	55, 58	I	**Base Address.** These bits determine one of four base addresses from which the Index and Data Registers are offset (See Table 2-2). An internal pull-down resistor of 30 kΩ is present on this pin. Use a 10 kΩ resistor to pull this pin to V_{CC}.
BOUT1,2	73, 65	O	**BAUD Output.** This multi-function pin provides the associated serial channel Baud Rate generator output signal, when test mode is selected in the Power and Test Configuration Register and the DLAB bit (LCR7) is set. After Master Reset this pin provides the SOUT function. (See SOUT and CFG0–4 for further information.)
BUSY	84	I	**Busy.** This pin is set high by the printer when it cannot accept another character. It has a nominal 25 kΩ pull-down resistor attached to it. (See $\overline{WAIT}$ and Table 7-5 for further information.)
CFG0–4	65, 66, 71 73, 74	I	**Configuration on Power-up.** These CMOS inputs select 1 of 32 default configurations in which the PC87334VLJ/PC87334VJG powers-up (See Table 2-1). An internal pull-down resistor of 30 kΩ is present on each pin. Use a 10 kΩ resistor to pull these pins to V_{CC}.
CLK48	57	I	**Clock 48.** This pin is the CLK48 reset strap option. During reset the value of this pin is latched into bit 0 of TUP (CLK48 bit). A 30 kΩ internal pull-down resistor is present on this pin. Use a 10 kΩ resistor to pull it high during reset.
$\overline{CTS1,2}$	72, 64	I	**Clear to Send.** When low this indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose condition the CPU can test by reading bit 4 (CTS) of the MODEM Status Register (MSR) for the appropriate serial channel. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MSR indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MSR. $\overline{CTS}$ has no effect on the transmitter. **Note:** Whenever the DCTS bit of the MSR is set an interrupt is generated if MODEM Status interrupts are enabled.
D7–D0	10–17	I/O	**Data.** Bi-directional data lines to the microprocessor. D0 is the LSB and D7 is the MSB. These signals all have 24 mA (sink) buffered outputs.

1.0 Pin Description (Continued)

Symbol	Pin	I/O	Function
$\overline{DCD1,2}$	77, 69	I	**Data Carrier Detect.** When low this signal indicates that the MODEM or data set has detected the data carrier.The $\overline{DCD}$ signal is a MODEM status input whose condition the CPU can test by reading bit 7 (DCD) of the MODEM Status Register (MSR) for the appropriate serial channel. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MSR indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MSR. **Note:** Whenever the DDCD bit of the MSR is set, an interrupt is generated if MODEM Status interrupts are enabled.
DENSEL Normal Mode	48	O	**Density Select.** Indicates that a high FDC density data rate (500 kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 kbps or 300 kbps) is selected. DENSEL is active high for high density (5.25″ drives) when IDENT is high, and active low for high density (3.5″ drives) when IDENT is low. DENSEL is also programmable via the Mode command (see Section 4.2.6).
DENSEL PPM Mode	78	O	**Density Select.** This pin provides an additional Density Select signal in PPM Mode when PNF = 0. (See $\overline{AFD}$ and Table 7-5 for further information.)
$\overline{DIR}$ Normal Mode	41	O	**Direction.** This output determines the direction of the floppy disk drive (FDD) head movement (active = step in, inactive = step out) during a seek operation. During reads or writes, DIR is inactive.
$\overline{DIR}$ PPM Mode	80	O	**Direction.** This pin provides an additional direction signal in PPM Mode when PNF = 0. (See $\overline{INIT}$ and Table 7-5 for further information.)
$\overline{DR0,1}$ Normal Mode	44, 45	O	**Drive Select 0,1.** These are the decoded Drive Select outputs that are controlled by the Digital Output Register bits D0, D1. The Drive Select outputs are gated with DOR bits 4–7. These are active low outputs. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. (See $\overline{MTR0,1}$ for more information.) $\overline{DR0}$ exchanges logical drive values with $\overline{DR1}$ when bit 4 of Function Control Register (FCR) is set. (See Table 7-5 for further information.)
$\overline{DR1}$ PPM Mode	85	O	**Drive Select 1.** This pin provides an additional Drive Select signal in PPM Mode when PNF = 0. It is drive select 1 when bit 4 of FCR is 0. It is drive select 0 when bit 4 of FCR is 1. This signal is active low. (See $\overline{ACK}$ and Table 7-5 for further information.)
DRATE0,1	52, 51	O	**Data Rate 0,1.** These outputs reflect the currently selected FDC data rate (bits 0 and 1 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last). The pins are totem-pole buffered outputs (6 mA sink, 6 mA source).
$\overline{DRV2}$	49	I	**Drive2.** This input indicates whether a second floppy disk drive has been installed. The state of this pin is available from Status Register A in PS/2® mode. (See PNF for further information.)

1.0 Pin Description (Continued)

Symbol	Pin	I/O	Function
$\overline{\text{DSKCHG}}$ Normal Mode	32	I	**Disk Change.** This input indicates if the drive door has been opened. The state of this pin is available from the Digital Input register. This pin can also be configured as the Read Gate (RGATE) data separator diagnostic input via the Mode command (see Section 4.2.6).
$\overline{\text{DSKCHG}}$ PPM Mode	89	I	**Disk Change.** This pin provides an additional Disk Change signal in PPM Mode when PNF = 0. (See PD4 and Table 7-5 for further information.)
$\overline{\text{DSR1,2}}$	76, 68	I	**Data Set Ready.** When low this signal indicates that the data set or MODEM is ready to establish a communications link. The $\overline{\text{DSR}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 5 (DSR) of the MODEM Status Register (MSR) for the appropriate channel. Bit 5 is the complement of the $\overline{\text{DSR}}$ signal. Bit 1 (DDSR) of the MSR indicates whether the $\overline{\text{DSR}}$ input has changed states since the previous reading of the MSR. (See IRRX for further information.) **Note:** Whenever the DDSR bit of the MSR is set, an interrupt is generated If MODEM Status interrupts are enabled.
$\overline{\text{DSTRB}}$	78	O	**Data Strobe.** This signal is used in EPP mode as a data strobe. It is active low. (See $\overline{\text{AFD}}$ and Table 7-5 for further information.)
$\overline{\text{DTR1,2}}$	71, 63	O	**Data Terminal Ready.** When low, this output indicates to the MODEM or data set that the UART is ready to establish a communications link. The $\overline{\text{DTR}}$ signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state. (See CFG4−0 for further information.)
$\overline{\text{ERR}}$	79	I	**Error.** A connected printer sets this input low when it has detected an error. This pin has a nominal 25 kΩ pull-up resistor attached to it. (See $\overline{\text{HDSEL}}$ and Table 7-5 for further information.)
$\overline{\text{FDACK}}$	5	I	**DMA Acknowledge.** Active low input to acknowledge the FDC DMA request and enable the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs during a DMA transfer. When in PC-AT® or Model 30 mode, this signal is enabled by bit D3 of the Digital Output Register (DOR). When in PS/2 mode, $\overline{\text{FDACK}}$ is always enabled, and bit D3 of the DOR is reserved. $\overline{\text{FDACK}}$ should be held high during I/O accesses.
FDRQ	4	O	**DMA Request.** Active high output to signal the DMA controller that a FDC data transfer is needed. When in PC-AT or Model 30 mode, this signal is enabled by bit D3 of the DOR. When in PS/2 mode, FDRQ is always enabled, and bit D3 of the DOR is reserved.
$\overline{\text{HCS0}}$	58	O	**Hard Drive Chip Select 0.** This output is active in the AT mode when 1) the hard drive registers from 1F0−1F7h are selected and the primary address is used or 2) the hard drive registers from 170−177h are selected and the secondary address is used. This output is inactive if the IDE interface is disabled via the Configuration Register. (See BADDR1 for further information.)
$\overline{\text{HCS1}}$	57	O	**Hard Drive Chip Select 1.** This output is active in the AT mode when 1) the hard drive registers from 3F6−7 are selected and the primary address is used or 2) the hard drive registers from 376−377 are selected and the secondary address is used. This output is also inactive, if the IDE interface is disabled via the Configuration Register. (See CLK48 for further information.)
$\overline{\text{HDSEL}}$ Normal Mode	34	O	**Head Select.** This output determines which side of the FDD is accessed. When active, the head selects side 1. When inactive, the head selects side 0.
$\overline{\text{HDSEL}}$ PPM Mode	79	O	**Head Select.** This pin provides an additional Head Select signal in PPM Mode when PNF = 0. (See $\overline{\text{ERR}}$ and Table 7-5 for further information.)
IDED7	60	I/O	**IDE Bit 7.** This pin provides the data bus bit 7 signal to the IDE hard drive during accesses in the address range 1F0−1F7h, 170−177h, 3F6h and 376h. This pin is in TRI-STATE during read or write accesses to 3F7h and 377h.

1.0 Pin Description (Continued)

Symbol	Pin	I/O	Function
$\overline{\text{IDEHI}}$	56	O	**IDE High Byte.** This output enables the high byte data latch during a read or write to the hard drive if the hard drive returns $\overline{\text{IOCS16}}$. This output is inactive if the IDE interface is disabled via the Configuration Register. (See $\overline{\text{VLD0}}$ for further information.)
$\overline{\text{IDELO}}$	55	O	**IDE Low Byte.** This output enables the low byte data latch during a read or write to the hard drive. This output is inactive if the IDE interface is disabled via the Configuration Register. (See BADDR0 for further information.)
IDENT	54	I	**Identity.** During chip reset, the IDENT and MFM pins are sampled to determine the desired mode of operation according to the following table: IDENT / MFM / MODE 1 / 1 or NC / PC-AT Mode 1 / 0 / Illegal 0 / 1 or NC / PS/2 Mode 0 / 0 / Model 30 Mode **AT Mode**—The DMA enable bit in the DOR is valid. TC is active high. Status Registers A and B are disabled (TRI-STATE). **Model 30 Mode**—The DMA enable bit in the DOR is valid. TC is active high. Status Registers A and B are enabled. **PS/2 Mode**—The DMA enable bit in the DOR is a don't care, and the FDRQ and IRQ6 signals are always enabled. TC is active low. Status Registers A and B are enabled. After chip reset, the state of IDENT determines the polarity of the DENSEL output. When IDENT is a logic "1", DENSEL is active high for the 500 kbps/1 Mbps/2 Mbps data rates. When IDENT is a logic "0", DENSEL is active low for the 500 kbps/1 Mbps/2 Mbps data rates. (See Mode command for further explanation of DENSEL.)
IDLE	43	O	**IDLE.** This pin is IDLE output when bit 4 of PMC is 1. IDLE indicates that the FDC is in the IDLE state and can be powered down. Whenever the FDC is in IDLE state, or whenever the FDC is in power-down state, the pin is active high. This bit is $\overline{\text{MTR1}}$ when bit 4 of the Power Management Control Register (PMC) is 0.
$\overline{\text{INDEX}}$ Normal Mode	47	I	**Index.** This input signals the beginning of a FDD track.
$\overline{\text{INDEX}}$ PPM Mode	94	I	**Index.** This pin provides an additional Index signal in PPM Mode when PNF = 0. (See PD0 and Table 7-5 for further information.)
$\overline{\text{INIT}}$	80	I/O	**Initialize.** When this signal is low it causes the printer to be initialized. This pin is in a TRI-STATE condition 10 ns after a 1 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 kΩ resistor. (See $\overline{\text{DIR}}$ and Table 7-5 for further information.)
IOCHRDY	53	O	**I/O Channel Ready.** This is the I/O Channel Ready open drain output when bit 7 of FCR is 0. When IOCHRDY is driven low, the EPP extends the host cycle. This pin is the MFM output pin when bit 7 of FCR is 1. (See MFM pin for further information.)
$\overline{\text{IOCS16}}$	59	I	**I/O Chip Select 16-bit.** This input is driven by the peripheral device when it can accommodate a 16-bit access.
IRQ3,4	1, 100	O	**Interrupt 3 and 4.** These are active high interrupts associated with the serial ports. IRQ3 presents the signal if the serial port has been designated as COM2 or COM4. IRQ4 presents the signal if the serial port is designated as COM1 or COM3. The appropriate interrupt goes active whenever it is enabled via the Interrupt Enable Register (IER), the associated Interrupt Enable bit (Modem Control Register bit 3, MCR3), and any of the following conditions are active: Receiver Error, Receive Data available, Transmitter Holding Register Empty, or a Modem Status Flag is set. The interrupt is reset low (inactive) after the appropriate interrupt service routine is executed, after being disabled via the IER, or after a Master Reset. Either interrupt can be disabled, putting them into TRI-STATE, by setting the MCR3 bit low.

1.0 Pin Description (Continued)

Symbol	Pin	I/O	Function
IRQ5	98	I/O	**Interrupt 5.** Active high output that indicates a parallel port interrupt. When enabled this bit follows the $\overline{ACK}$ signal input. When bit 4 in the parallel port Control Register is set and the parallel port address is designated as shown in Table 2-5, this interrupt is enabled. When it is not enabled this signal is TRI-STATE. This pin is I/O only when ECP is enabled, and IRQ5 is configured. For ECP operation, refer to the interrupt ECP Section 7.11.1.
IRQ6	97	O	**Interrupt 6.** Active high output to signal the completion of the execution phase for certain FDC commands. Also used to signal when a data transfer is ready during a Non-DMA operation. When in PC-AT or Model 30 mode, this signal is enabled by bit D3 of the DOR. When in PS/2 mode, IRQ6 is always enabled, and bit D3 of the DOR is reserved.
IRQ7	96	I/O	**Interrupt 7.** Active high output that indicates a parallel port interrupt. When enabled this bit follows the $\overline{ACK}$ signal input. When bit 4 in the parallel port Control Register is set and the parallel port address is designated as shown in Table 2-5, this interrupt is enabled. When it is not enabled this signal is TRI-STATE. This pin is I/O only when ECP is enabled, and IRQ7 is configured. For ECP operation, refer to the interrupt ECP Section 7.11.1.
MR	2	I	**Master Reset.** Active high input that resets the controller to the idle state, and resets all disk interface outputs to their inactive states. The DOR, DSR, CCR, Mode command, Configure command, and Lock command parameters are cleared to their default values. The Specify command parameters are not affected. The Configuration Registers are set to their selected default values.
MFM	53	I/O	**MFM (Modified Frequency Modulation).** During a chip reset, when IDENT is low, this pin is sampled to select the PS/2 mode (MFM high), or the Model 30 mode (MFM low). An internal pull-up or external pull-down 10k resistor selects between the two PS/2 modes. When the PC-AT mode is desired (IDENT high), MFM should be left pulled high internally. MFM reflects the current data encoding format when RESET is inactive. MFM = high. Defaults to low after a chip reset. (See IOCHRDY for further information.)
$\overline{MTR0,1}$ Normal Mode	46, 43	O	**Motor Select 0,1.** These are the motor enable lines for drives 0 and 1, and they are controlled by bits D7–D4 of the Digital Output register. They are active low outputs. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. $\overline{MTR0}$ exchanges logical motor values with $\overline{MTR1}$ when bit 4 of FCR is set. (See $\overline{DR0,1}$).
$\overline{MTR1}$ PPM Mode	84	O	**Motor Select 1.** This pin provides an additional Motor Select 1 signal in PPM Mode when PNF = 0. This pin is the motor enable line for drive 1 when bit 4 of FCR is 0. It is the motor enable line for drive 0 when bit 4 of FCR is 1. This signal is active low. (See BUSY and Table 7-5 for further information.)
MSEN0,1 Normal Mode	52, 51	I	**Media Sense.** These pins are Media Sense input pins when bit 0 of FCR is 0. Each pin has a 10 kΩ internal pull-up resistor. When bit 0 of FCR is 1, these pins are Data Rate output pins, and the pull-up resistors are disabled. (See DRATE0,1 for further information.)
MSEN0,1 PPM Mode	88, 86	I	**Media Sense.** These pins provide additional Media Sense signals for PPM Mode and PNF = 0. (See PD5, 7 and Table 7-5 for further information.)
PD	45	O	**Power-Down.** This pin is PD output when bit 4 of PMC is 1. It is $\overline{DR1}$ when bit 4 of PMC is 0. PD is active high whenever the FDC is in power-down state, either via bit 6 of DSR (or bit 3 of FER, or bit 0 of PTR), or via the mode command. See $\overline{DR1}$ for further information.
PD0–7	94–91, 89–86	I/O	**Parallel Port Data.** These bidirectional pins transfer data to and from the peripheral data bus and the parallel port Data Register. These pins have high current drive capability. (See DC Electrical Characteristics.) (See MSEN0,1 $\overline{INDEX}$, $\overline{TRK0}$, $\overline{WP}$, $\overline{RDATA}$, $\overline{DSKCHG}$ and Table 7-5 for further information.)

1.0 Pin Description (Continued)

Symbol	Pin	I/O	Function
$\overline{\text{PDACK}}$	54	I	**Printer DMA Acknowledge.** Active low input to acknowledge the printer DMA request, and enable the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs during a DMA transfer. This pin is $\overline{\text{PDACK}}$ input pin when bit 3 of PMC is 1. It is IDENT when bit 3 of PMC is 0. $\overline{\text{PDACK}}$ input pin is ECP DMA acknowledge. $\overline{\text{PDACK}}$ is assumed to be 1 when bit 3 of PMC is 0. IDENT is assumed to be 1 when bit 3 of PMC is 1. This input is valid only in ECP mode.
PDRQ	33	O	**Printer DMA Request.** Active high output to signal the DMA controller that a printer data transfer is required. This pin is in TRI-STATE when ECP is disabled (bit 2 of PCR is 0), or configured with no DMA (bit 3 of PMC is 0). This output is valid only in ECP mode.
$\overline{\text{PWDN}}$	3	I	**Power Down.** This multi-function pin stops the clocks and/or the external crystal based on the selections made in the Power and Test Register bits 1-2. This pin also affects the FDC, UARTs, IDE and Parallel Port pins, when the relevant PMC register bits are set. (See $\overline{\text{ZWS}}$ for further information.)
PE	83	I	**Paper End.** This input is set high by the printer when it is out of paper. This pin has a nominal 25 kΩ pull-down resistor attached to it. (See $\overline{\text{WDATA}}$ and Table 7-5 for further information.)
PNF	49	I	**Printer Not Floppy.** PNF is the Printer Not Floppy pin when bit 2 of FCR is 1. It selects the device which is connected to the PPM pins. A parallel printer is connected when PNF = 1, and a floppy disk drive is connected when PNF = 0. This pin is the DRV2 input pin when bit 2 of FCR is 0. (See $\overline{\text{DRV2}}$ for further information.)
$\overline{\text{RD}}$	19	I	**Read.** Active low input to signal data read by the microprocessor.
$\overline{\text{RDATA}}$ Normal Mode	35	I	**Read Data.** This input is the raw serial data read from the floppy disk drive.
$\overline{\text{RDATA}}$ PPM Mode	91	I	**Read Data.** This pin provides an additional Read Data signal in PPM Mode when PNF = 0. (See PD3 and Table 7-5 for further information.)
$\overline{\text{RI1,2}}$	70, 62	I	**Ring Indicator.** When low this indicates that a telephone ring signal has been received by the MODEM. The RI signal is a MODEM status input whose condition the CPU can test by reading bit 6 (RI) of the MODEM Status Register (MSR) for the appropriate serial channel. Bit 6 is the complement of the RI signal. Bit 2 (TERI) of the MSR indicates whether the RI input has changed from low to high since the previous reading of the MSR. **Note:** When the TERI bit of the MSR is set, an interrupt is generated if MODEM Status interrupts are enabled.
$\overline{\text{RTS1,2}}$	74, 66	O	**Request to Send.** When low, this output indicates to the MODEM or data set that the UART is ready to exchange data. The $\overline{\text{RTS}}$ signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state. (See CFG0−4 for further information.)
SIN1,2	75, 67	I	**Serial Input.** This input receives composite serial data from the communications link (e.g. peripheral device, MODEM, or data set).
SLCT	82	I	**Select.** When a printer is connected, it sets this input high. This pin has a nominal 25 kΩ pull-down resistor attached to it.
$\overline{\text{SLIN}}$	81	I/O	**Select Input.** When this signal is low it selects the printer. This pin is in a TRI-STATE condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 kΩ resistor. (See $\overline{\text{ASTRB}}$, $\overline{\text{STEP}}$ and Table 7-5 for further information.)
SOUT1,2	73, 65	O	**Serial Output.** This output signal sends composite serial data to the communications link (e.g. peripheral device, MODEM, or data set). The SOUT signal is set to a marking state (logic 1) after a Master Reset operation. (See BOUT and CFG0−4 for further information.)

1.0 Pin Description (Continued)

Symbol	Pin	I/O	Function
$\overline{STB}$	95	I/O	**Data Strobe.** This output signal indicates to the printer that valid data is available at the printer port. This pin is in a TRI-STATE condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 kΩ resistor. (See $\overline{WRITE}$ for further information.)
$\overline{STEP}$ Normal Mode	40	O	**Step.** This output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{STEP}$ PPM Mode	81	O	**Step.** This pin provides an additional step signal in PPM Mode when PNF = 0. (See $\overline{SLIN}$, $\overline{ASTRB}$ and Table 7-5 for further information.)
TC	6	I	**Terminal Count.** Control signal from the DMA controller to indicate the termination of a DMA transfer. TC is accepted only when $\overline{FDACK}$ is active. TC is active high in PC-AT and Model 30 modes, and active low in PS/2 mode.
$\overline{TRK0}$ Normal Mode	37	I	**Track 0.** This input indicates to the controller that the head of the selected floppy disk drive is at track zero.
$\overline{TRK0}$ PPM Mode	93	I	**Track 0.** This pin provides an additional Track 0 signal in PPM Mode when PNF = 0. (See PD1 and Table 7-5 for further information.)
V_{DDB}, V_{DDC}	50, 99		**Power Supply.** This is the 3.3V or 5V supply voltage for the PC87332 circuitry.
$\overline{VLD0,1}$	56, 63	I	**Valid Data.** These input pins are sensed during reset, and indicate the state of bit 5 in the FDC Tape Drive Register (3F3h). They indicate whether bits 6 and 7 of this register contain valid media ID information for floppy drives 0 and 1. If $\overline{VLD0}$ is sensed low at reset, then whenever drive 0 is accessed, bit 5 of the Tape Drive Register is a 0 indicating that bits 6 and 7 contain valid media ID information. If $\overline{VLD0}$ is sensed high at reset, then whenever drive 0 is accessed, bit 5 of the Tape Drive Register is a 1 indicating that bits 6 and 7 do not contain valid media ID information. The same is true of $\overline{VLD1}$ relative to the media ID information for drive 1. If bit 0 of FCR is 1, the $\overline{VLD}$ bits have no meaning. $\overline{VLD0}$ value during reset is loaded into bit 0 of FCR (to select between media sense or DRATE). A 30 kΩ internal pull-down resistor is on each pin. Use a 10 kΩ resistor to pull these pins to high during reset.
V_{SSB}, V_{SSC}, V_{SSD}, V_{SSE}	42, 9, 90, 61		**Ground.** This is the ground for the PC87332 circuitry.
$\overline{WAIT}$	84	I	**Wait.** This signal is used, in EPP mode, by the parallel port device to extend its access cycle. It is active low. (See BUSY and Table 7-5 for further information.)
$\overline{WR}$	18	I	**Write.** Active low input signal to indicate a write from the microprocessor to the controller.
$\overline{WDATA}$ Normal Mode	39	O	**Write Data.** This output is the write precompensated serial data that is written to the selected floppy disk drive. Precompensation is software selectable.
$\overline{WDATA}$ PPM Mode	83	O	**Write Data.** This pin provides an additional Write Data signal in PPM Mode when PNF = 0. (See PE and Table 7-5 for further information.)
$\overline{WGATE}$ Normal Mode	38	O	**Write Gate.** This output signal enables the write circuitry of the selected disk drive. $\overline{WGATE}$ has been designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
$\overline{WGATE}$ PPM Mode	82	O	**Write Gate.** This pin provides an additional Write Gate signal in PPM Mode when PNF = 0. (See SLCT and Table 7-5 for further information.)

1.0 Pin Description (Continued)

Symbol	Pin	I/O	Function
$\overline{WP}$ Normal Mode	36	I	**Write Protect.** This input indicates that the floppy disk in the selected drive is write protected.
$\overline{WP}$ PPM Mode	92	I	**Write Protect.** This pin provides an additional Write Protect signal in PPM Mode when PNF = 0. (See PD2 and Table 7-5 for further information.)
$\overline{WRITE}$	95	O	**Write Strobe.** This signal is used in EPP mode as a write strobe. It is active low. (See $\overline{STB}$ and Table 7-5 for further information.)
X1/OSC	7	I	**Crystal1/Clock.** One side of an external 24 MHz/48 MHz crystal is attached here. The other side of the crystal is connected to X2. If a crystal is not used, a TTL or CMOS compatible clock is connected to this pin.
X2	8	O	**Crystal2.** One side of an external 24 MHz/48 MHz crystal is attached here. The other side of the crystal is connected to X1/OSC. This pin is left unconnected if an external clock is used.
$\overline{ZWS}$	3	O	**Zero Wait State.** This pin is the Zero Wait State open drain output pin when bit 6 of FCR is 0. $\overline{ZWS}$ is driven low when the EPP or ECP is written, and the access can be shortened. This pin is $\overline{PWDN}$ when bit 6 of FCR is 1. (See the $\overline{PWDN}$ pin for further information.)

2.0 Configuration Registers

2.1 OVERVIEW

Eight registers constitute the Base Configuration Register set, and control the PC87332 set-up. In general, these registers control the enabling of major functions (FDC, UARTs, parallel port, pin functionality, etc.), the I/O addresses of these functions, and whether they power-down via hardware control or not. These registers are the Function Enable Register (FER), Function Address Register (FAR), Power and Test Register (PTR), Function Control Register (FCR), the Printer Control Register (PCR), the Power Management Control Register (PMC), the Tape, UARTs and Parallel Port Configuration Register (TUP), and the SuperI/O (SIO) Identification Register (SID).

During reset, the PC87332 loads a set of default values selected by a hardware strapping option into the FER, FAR, and PTR Configuration Registers. The FCR, PCR, PMC, TUP and SID registers can only be accessed by software.

An index and data register pair are used to read and write the configuration registers. Each Configuration Register is pointed to the value loaded into the Index Register. The data to be written into the Configuration Register is transferred via the Data register. A Configuration Register is read in a similar way (i.e., by pointing to it via the Index Register and then reading its contents via the Data Register).

Accessing the Configuration Registers in this way requires only two system I/O addresses. Since I/O address space is shared by other devices, the Index and Data Registers can still be inadvertently accessed. To reduce the chances of an inadvertent access, a simple procedure has been developed. It is described in Section 2.2.

2.2 SOFTWARE CONFIGURATION

If the system requires access to the Configuration Registers after reset, the following procedure must be used to change data in the registers.

1. Determine the default location of the PC87332 Index Register.

   Check the four possible locations (see Table 2-1) by reading them twice. The first byte is the ID byte 88h, although read-after-write always brings the value of the written byte. The second byte read is always 00h. Compare the data read with the ID byte and then 00h. A match occurs at the correct location. Note that the ID byte is only issued from the Index Register during the first read after a reset. Subsequent reads return the value loaded into the Index Register. Bits 4-6 are reserved and always read 0.

2. Load the Configuration Registers.
   - A. Disable CPU interrupts.
   - B. Write the index of the Configuration Register (00h–0Eh) to the Index Register one time.
   - C. Write the correct data for the Configuration Register in two consecutive write accesses to the Data Register.
   - D. Enable CPU interrupts.

3. Load the Configuration Registers (read-modify-write).
   - A. Disable CPU interrupts.
   - B. Write the index of the Configuration Register (00h–0Eh) to the Index Register one time.
   - C. Read the configuration data in that register via the Data Register.
   - D. Modify the configuration data.
   - E. Write the changed data for the Configuration Register in two consecutive writes to the Data Register. The register updates on the second consecutive write.
   - F. Enable CPU interrupts.

A single read access to the Index and Data Registers can be done at any time without disabling CPU interrupts. When the Index Register is read, the last value loaded into the Index Register is returned. When the Data Register is read, the Configuration Register data pointed to by the Index Register is returned.

2.0 Configuration Registers (Continued)

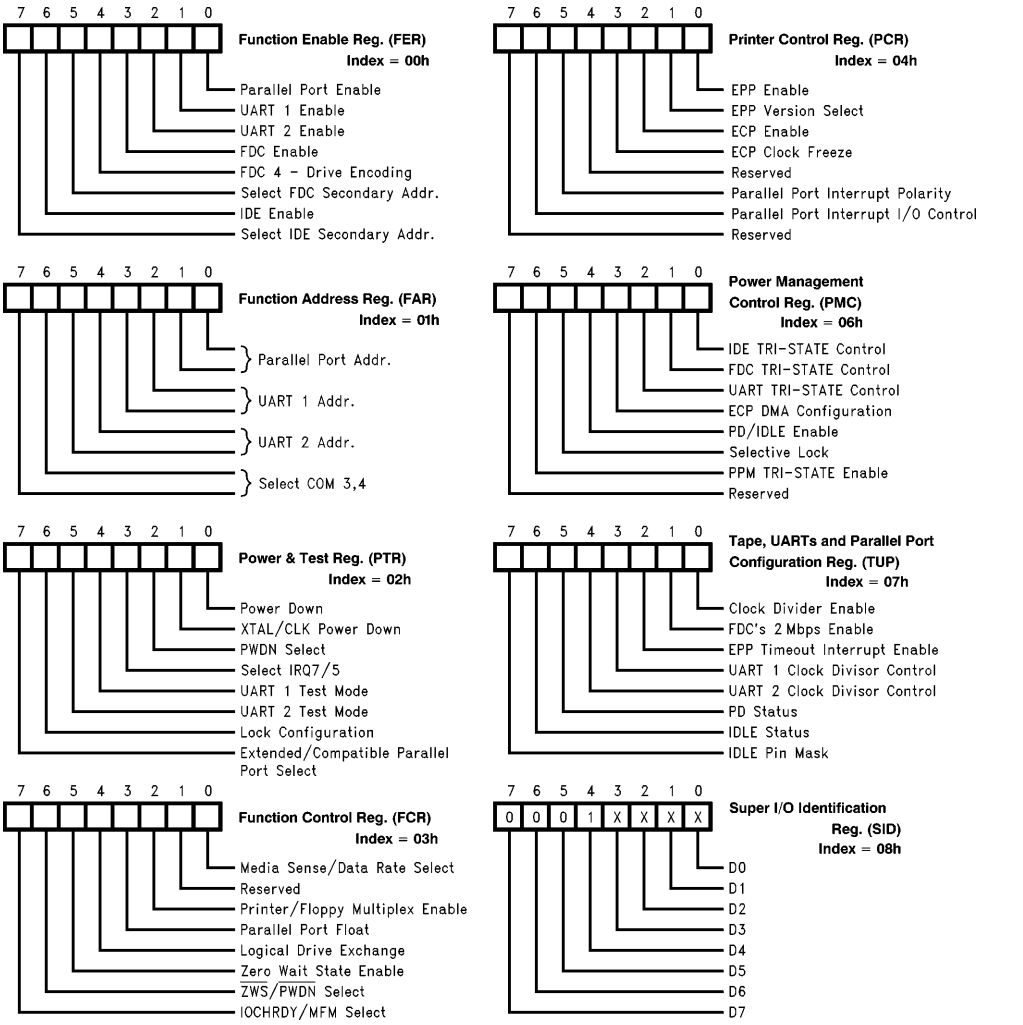


FIGURE 2-1. PC87332VLJ/PC87332VLJ-5 Configuration Registers

2.0 Configuration Registers (Continued)

2.3 HARDWARE CONFIGURATION

During reset, one of 32 possible sets of default values are loaded into the first three Configuration Registers. A strapping option on five pins (CFG0−4) selects the set of values that is loaded. This allows for automatic configuration without software intervention. Table 2-1 shows the 32 possible default configurations. The default configuration can be modified by software at any time after reset by using the access procedure described in the Software Configuration Section.

Table 2-1 is organized as follows. The logic values of the five external Configuration Pins are associated with the resulting Configuration Register Data and the activated functions. The activated functions are grouped into seven categories based on the data in the FER. In some cases the data in the FER is given as one of two options. This is because the primary or secondary IDE address is chosen via the FER.

The PTR has one value associated with the active functions in the FER. This value allows the power-down of all clocks when the $\overline{\text{PWDN}}$ pin goes active. In the last case where no functions are active after reset, activating the $\overline{\text{PWDN}}$ pin also stops the crystal.

Most of the variability available is through the FAR. Addresses controlled by the FAR are coded as follows:

PRI: is the PRImary floppy or IDE address (i.e., 3F0−7h or 1F0−7, 3F6, 7h).

SEC: is the SECondary IDE address (170−7, 376, 7h).

COM1: is the UART address at 3F8−Fh.

COM2: is the UART address at 2F8−Fh.

COM3: is the UART address at 3E8−Fh.

COM4: is the UART address at 2E8−Fh.

LPTA: is the parallel port (|| PORT) address at 3BC−3BEh.

LPTB: is the || PORT address at 378−37Fh.

The chosen addresses are given under active functions and are in the same order as the active functions with which they are associated. In other words, if the active functions are given as FDC, IDE, UART1, UART2, || PORT and the addresses are given as PRI, PRI, COM1, COM2, LPTB, then the functions and the addresses are associated as follows: FDC = PRI, IDE = PRI, UART1 = COM1, UART2 = COM2, || PORT = LPTB.

TABLE 2-1. Default Configurations Controlled by Hardware

Configuration Pins (CFGn)					Data (Hex)	Activated Functions
4	3	2	1	0		
					FER = 4F, CF	FDC, IDE, UART1, UART2, || PORT
					PTR = 00, 80	Power-Down Clocks Option
0	0	0	0	0	FAR = 10	PRI, PRI, COM1, COM2, LPTB
0	0	0	0	1	FAR = 11	PRI, PRI, COM1, COM2, LPTA
0	0	0	1	0	FAR = 11	PRI, SEC, COM1, COM2, LPTA
0	0	0	1	1	FAR = 39	PRI, PRI, COM3, COM4, LPTA
0	0	1	0	0	FAR = 24	PRI, PRI, COM2, COM3, LPTB
0	0	1	0	1	FAR = 38	PRI, SEC, COM3, COM4, LPTB
					FER = 4B, CB	FDC, IDE, UART1, || PORT
					PTR = 00, 80	Power-Down Clocks Option
0	0	1	1	0	FAR = 00	PRI, PRI, COM1, LPTB
0	0	1	1	1	FAR = 01	PRI, PRI, COM1, LPTA
0	1	0	0	0	FAR = 01	PRI, SEC, COM1, LPTA
0	1	0	0	1	FAR = 09	PRI, PRI, COM3, LPTA
0	1	0	1	0	FAR = 08	PRI, PRI, COM3, LPTB
0	1	0	1	1	FAR = 08	PRI, SEC, COM3, LPTB
					FER = 0F	FDC, UART1, UART2, || PORT
					PTR = 00, 80	Power-Down Clocks Option
0	1	1	0	0	FAR = 10	PRI, COM1, COM2, LPTB
0	1	1	0	1	FAR = 11	PRI, COM1, COM2, LPTA
0	1	1	1	0	FAR = 39	PRI, COM3, COM4, LPTA
0	1	1	1	1	FAR = 24	PRI, COM2, COM3, LPTB

2.0 Configuration Registers (Continued)

TABLE 2-1. Default Configurations Controlled by Hardware (Continued)

Configuration Pins (CFGn)					Data (Hex)	Activated Functions
4	**3**	**2**	**1**	**0**		
					FER = 49, C9	FDC, IDE, || PORT
					PTR = 00, 80	Power-Down Clocks Option
1	0	0	0	0	FAR = 00	PRI, PRI, LPTB
1	0	0	0	1	FAR = 01	PRI, PRI, LPTA
1	0	0	1	0	FAR = 01	PRI, SEC, LPTA
1	0	0	1	1	FAR = 00	PRI, SEC, LPTB
					FER = 07	UART1, UART2, || PORT
					PTR = 00, 80	Power-Down Clocks Option
1	0	1	0	0	FAR = 10	COM1, COM2, LPTB
1	0	1	0	1	FAR = 11	COM1, COM2, LPTA
1	0	1	1	0	FAR = 39	COM3, COM4, LPTA
1	0	1	1	1	FAR = 24	COM2, COM3, LPTB
					FER = 47, C7	IDE, UART1, UART2, || PORT
					PTR = 00, 80	Power-Down Clocks Option
1	1	0	0	0	FAR = 10	PRI, COM1, COM2, LPTB
1	1	0	0	1	FAR = 11	PRI, COM1, COM2, LPTA
1	1	0	1	0	FAR = 11	SEC, COM1, COM2, LPTA
1	1	0	1	1	FAR = 39	PRI, COM3, COM4, LPTA
1	1	1	0	0	FAR = 24	PRI, COM2, COM3, LPTB
1	1	1	0	1	FAR = 38	SEC, COM3, COM4, LPTB
					FER = 08	FDC
					PTR = 00, 80	Power-Down Clocks Option
1	1	1	1	0	FAR = 10	PRI
					FER = 00	None
					PTR = 02, 82	Power-Down XTAL and Clocks
1	1	1	1	1	FAR = 10	NA

2.0 Configuration Registers (Continued)

2.4 INDEX AND DATA REGISTERS

Another general aspect of the Configuration Registers is that the Index and the Data Register pair can be relocated to one of four locations. This is controlled through a hardware strapping option on pins (BADDR0,1) and it allows the registers to avoid conflicts with other adapters in the I/O address space. Table 2-2 shows the address options.

TABLE 2-2. Index and Data Register Optional Locations

BADDR1	BADDR0	Index Addr.	Data Addr.
0	0	398	399
0	1	26E	26F
1	0	15C	15D
1	1	2E	2F

2.5 BASE CONFIGURATION REGISTERS

2.5.1 Function Enable Register (FER, Index 00h)

This register enables and disables major chip functions (e.g. UARTs, parallel ports, FDC, etc.). Disabled functions have their clocks automatically powered-down, but the data in their registers remains intact. It also selects whether the FDC and the IDE controller is located at their primary or secondary address.

Bit 0 When this bit is 1 the parallel port can be accessed at the address specified in the FAR.

Bit 1 When this bit is 1, UART1 can be accessed at the address specified in the FAR. When this bit is 0, access to UART1 is blocked and it is in power-down mode. The UART1 registers retain all data in power-down mode.

Caution: Any UART1 interrupt that is enabled and active or becomes active after UART1 is disabled, asserts the associated IRQ pin. If disabling UART1 via software, clear the IRQ Enable bit (MCR3) to 0 before clearing FER 1. This is not an issue after reset because MCR3 is 0 until it is written.

Bit 2 When this bit is 1, UART2 can be accessed at the address specified in the FAR. When this bit is 0, access to UART2 is blocked and it is in power-down mode. The UART2 registers retain all data in power-down mode.

Caution: Any UART2 interrupt that is enabled and active or becomes active after UART2 is disabled asserts the associated IRQ pin. If disabling UART2 via software, clear the IRQ Enable bit (MCR3) to 0 before clearing FER 1. This is not an issue after reset because MCR3 is 0 until it is written.

Bit 3 When this bit is 1, the FDC can be accessed at the address specified in the FER bits. When this bit is 0 access to the FDC is blocked and it is in power-down mode. The FDC registers retain all data in power-down mode.

Bit 4 When this bit is 0 the PC87332 can control two floppy disk drives directly without an external decoder. When this bit is 1 the two drive select signals and two motor enable signals from the FDC are encoded so that four floppy disk drives can be controlled (see Table 2-3 and *Figure 2-2*). Controlling four FDDs requires an external decoder. The pin states shown in Table 2-3 are a direct result of the bit patterns shown. All other bit patterns produce pin states that should not be decoded to enable any drive or motor.

Bit 5 This bit selects the primary or secondary FDC address. (See Table 2-4.)

Bit 6 When this bit is a 1 the IDE drive interface can be accessed at the address specified by FER bit 7. When it is 0, access to the IDE interface is blocked, the IDE control signals (i.e., $\overline{HCS0}$, $\overline{HCS1}$, $\overline{IDELO}$, $\overline{IDEHI}$) are held in the inactive state, and the IDED7 signal is in TRI-STATE.

Bit 7 This bit selects the primary or secondary IDE address. (See Table 2-4.)

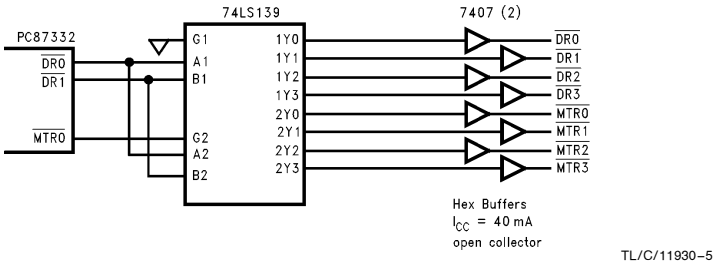


FIGURE 2-2. PC87332 Four Floppy Drive Circuit Example

TABLE 2-3. Encoded Drive and Motor Pin Information (FER 4 = 1)

Digital Output Register								Drive Control Pins				Decoded Functions
7	6	5	4	3	2	1	0	$\overline{MTR1}$	$\overline{MTR0}$	$\overline{DR1}$	$\overline{DR0}$	
X	X	X	**1**	X	X	0	0	(Note)	0	0	0	Activate Drive 0 and Motor 0
X	X	**1**	X	X	X	0	1	(Note)	0	0	1	Activate Drive 1 and Motor 1
X	**1**	X	X	X	X	1	0	(Note)	0	1	0	Activate Drive 2 and Motor 2
1	X	X	X	X	X	1	1	(Note)	0	1	1	Activate Drive 3 and Motor 3
X	X	X	**0**	X	X	0	0	(Note)	1	0	0	Activate Drive 0 and Deactivate Motor 0
X	X	**0**	X	X	X	0	1	(Note)	1	0	1	Activate Drive 1 and Deactivate Motor 1
X	**0**	X	X	X	X	1	0	(Note)	1	1	0	Activate Drive 2 and Deactivate Motor 2
0	X	X	X	X	X	1	1	(Note)	1	1	1	Activate Drive 3 and Deactivate Motor 3

Note: When FER4 = 1, $\overline{MTR1}$ presents a pulse that is the inverted image of the IOW strobe. This inverted pulse is active whenever an I/O write to address 3F2h or 372h takes place. This pulse is delayed by 25 ns–80 ns after the leading edge of IOW and its leading edge can be used to clock data into an external latch (e.g., 74LS175). Address 3F2h is used if the FDC is located at the primary address (FER5 = 0) and address 372h is used if the FDC is located at the secondary address (FER5 = 1).

TABLE 2-4. Primary and Secondary Drive Address Selection

Bit 5	Bit 7	Drive	PC-AT Mode
0	X	FDC	Primary, 3F0–7h
1	X	FDC	Secondary, 3F0–7h
X	0	IDE	Primary, 1F0–7h, 3F6–7h
X	1	IDE	Secondary 170–7h, 376–7h

2.5.2 Function Address Register (FAR, Index = 01h)

This register selects the ISA I/O address range to which each peripheral function responds.

Bits 0,1 These bits select the parallel port address as shown in Table 2-5:

TABLE 2-5. Parallel Port Addresses

Bit 1	Bit 0	Parallel Port Address	PC-AT Interrupt
0	0	LPTB (378–37F)	IRQ5 (Note)
0	1	LPTA (3BC–3BE)	IRQ7
1	0	LPTC (278–27F)	IRQ5
1	1	Reserved	TRI-STATE (CTR4 = 0)

Note: The interrupt assigned to this address can be changed to IRQ7 by setting Bit 3 of the Power and Test Register (PTR).

Bits 2–5 These bits determine which ISA I/O address range is associated with each UART (see Table 2-6 and Table 2-7).

TABLE 2-6. COM Port Selection for UART1

FAR		UART1 COM #
Bit 3	Bit 2	
0	0	1 (3F8-F)
0	1	2 (2F8-F)
1	0	3 (Table 2-8)*
1	1	4 (Table 2-8)*

TABLE 2-7. COM Port Selection for UART2

FAR		UART2 COM #
Bit 5	Bit 4	
0	0	1 (3F8-F)
0	1	2 (2F8-F)
1	0	3 (Table 2-8)*
1	1	4 (Table 2-8)*

***Note:** COM3 and COM4 addresses are determined by Bits 6 and 7.

Bits 6,7 These bits select the addresses that are used for COM3 and COM4 (see Table 2-8).

TABLE 2-8. Address Selection for COM3 and COM4

Bit 7	Bit 6	COM3 IRQ4	COM4 IRQ3
0	0	3E8–Fh	2E8–Fh
0	1	338–Fh	238–Fh
1	0	2E8–Fh	2E0–7h
1	1	220–7h	228–Fh

2.0 Configuration Registers (Continued)

2.5.3 Power and Test Register (PTR, Index = 02h)

This register determines the power-down method used when the power-down pin ($\overline{PWDN}$) is asserted (crystal and clocks vs. clocks only) and whether hardware power-down is enabled. It also provides a bit for software power-down of all enabled functions. It selects whether IRQ7 or IRQ5 is associated with LPTB. It puts the enabled UARTs into their test mode.

Independent of this register the floppy disk controller can enter low power mode via the Mode Command or the Data Rate Select Register.

Bit 0 Setting this bit causes all enabled functions to be powered-down.
If the crystal power-down option is selected (see Bit 1) the crystal is also powered-down. All register data is retained when the crystal or clocks are stopped. The FDC, UARTs, IDE and Parallel Port pins are affected by this bit when the relevant PMC register bits are set.

Note: Bits 2 and 3 of PCR can affect the function of the parallel port power-down mode.

Bit 1 When the Power-Down pin or Bit 0 is asserted this bit determines whether the enabled functions have their internal clocks stopped (Bit 1 = 0) or the external crystal (Bit 1 = 1) is stopped. Stopping the crystal is the lowest power consumption state of the part. However, if the crystal is stopped, a finite amount of time (~8 ms) is required for crystal stabilization once the Power-Down pin ($\overline{PWDN}$) or Bit 0 is deasserted. If all internal clocks are stopped, but the crystal continues to oscillate, no stabilization period is required after the Power-Down pin or Bit 0 is deasserted.

Bit 2 Reserved. This bit must be set to 0.

Bit 3 Setting this bit associates the parallel port with IRQ7 when the address for the parallel port is 378–37Fh (LPTB). This bit is a ''don't care'' when the parallel port address is 3BC–3BEh (LPTA) or 278–27Fh (LPTC).

Bit 4 Setting this bit puts UART1 into a test mode, which causes its Baud Out clock to be present on its SOUT1 pin if the Line Control Register bit 7 is set to 1.

Bit 5 Setting this bit puts UART2 into a test mode, which causes its Baud Out clock to be present on its SOUT2 pin if the Line Control Register bit 7 is set to 1.

Bit 6 Setting this bit to 1 prevents all further write accesses to the Configuration Registers. Once it is set by software it can only be cleared by a hardware reset. After the initial hardware reset it is zero.

Bit 7 When not in EPP or ECP modes, this bit selects Compatible or Extended mode operation and thus controls whether Pulse or Level interrupts are used.
Set this bit to 0 for Compatible mode, Pulse interrupt.
Set this bit to 1 for Extended mode, Level interrupt.
In EPP mode this bit selects Regular or Automatic bidirectional mode, thus determining the direction control method:
Set this bit to 0 for Automatic mode, Host $\overline{RD}$ and $\overline{WR}$ signals control the direction.
Set this bit to 1 for Regular mode, bit 5 of CTR controls the direction.
After the initial hardware reset, this bit is 0.

2.5.4 Function Control Register (FCR, Index = 03h)

This register determines several pin options:

It selects between Data Rate output and automatic media sense inputs.

It enables the Parallel Port Multiplexor (PPM), and switches between internal and external drives.
For Enhanced Parallel Port operation it enables the IOCHRDY and $\overline{ZWS}$ options, and pins.
On reset bits 2–7 of FCR are cleared.

Bit 0 Media Sense/Data Rate select bit. When this bit is 0, the MSEN0–1 pins are Media Sense inputs and bits 5–7 of TDR are valid. When this bit is 1, the DRATE0–1 pins are Data Rate outputs and bits 2–7 of TDR are TRI-STATE during read. On reset, the $\overline{VLD0}$ pin is sampled and its value placed into this bit.

Bit 1 Reserved.

Bit 2 Printer/Floppy Parallel Port Multiplexor (PPM) enable bit. When this bit is 0, the port is configured as a parallel port. When this bit is 1, the port is configured as a floppy drive port. See PNF pin description for further information. The $\overline{DRV2}$/PNF pin is read as $\overline{DRV2}$ bit, regardless of bit 2 of FCR.

Bit 3 Parallel Port Multiplexor (PPM) float control bit. When this bit is 0, the PPM pins are driven. When this bit is 1, the PPM pins are in TRI-STATE mode and the pull-ups are disconnected.

Bit 3 is functional whether or not the PPM is configured (when bit 2 of FCR is 0).

When bit 3 = 1 the PPM outputs are in TRI-STATE and the inputs are blocked to reduce their leakage current. The values of the blocked inputs are: BUSY = 1, PE = 0, SLCT = 0, $\overline{ACK}$ = 1 and $\overline{ERR}$ = 1.

Note: To avoid undefined FDC inputs the PPM can be disabled before this bit is set.

Bit 4 Logical Drive Exchange bit. This bit allows software to exchange the physical floppy-disk control signals, assigned to drives 0 and 1, thus exchanging the logical drives A and B.

This is accomplished by exchanging control of the $\overline{DR0}$ and $\overline{MTR0}$ pins with the $\overline{DR1}$ and $\overline{MTR1}$ pins. The result is undefined if four drive mode is selected (FER4 = 1). Table 2-9 shows the associations between the Configuration Register bit, the Digital Output Register bits (DRVSEL0,1 and MTR0,1) and the drive and motor control pins ($\overline{DR0,1}$ and $\overline{MTR0,1}$).

TABLE 2-9. Logical Drive Exchange

FCR Bit 4	Digital Output Register (FDC)				Asserted FDC Pins
	MTR1	MTR0	DRVSEL1	DRVSEL0	
0	0	1	0	0	$\overline{DR0}$, $\overline{MTR0}$
0	1	0	0	1	$\overline{DR1}$, $\overline{MTR1}$
1	0	1	0	0	$\overline{DR1}$, MTR1
1	1	0	0	1	$\overline{DR0}$, $\overline{MTR0}$

Bit 5 Zero Wait State enable bit. If this bit is 1, (and pin 3/1 (PQFP/TQFP) is configured as $\overline{ZWS}$) $\overline{ZWS}$ is driven low when the Enhanced Parallel Port (EPP) or the ECP can accept a short host read/write-cycle, otherwise the $\overline{ZWS}$ open drain output is not driven. EPP $\overline{ZWS}$ operation should be configured when the system is fast enough to support it.

Bit 6 $\overline{ZWS}$/$\overline{PWDN}$ select bit. When this bit is 0, the $\overline{ZWS}$ pin is Zero Wait State output.
When this bit is 1, the $\overline{PWDN}$/$\overline{CSOUT}$ pin option is selected.

Bit 7 IOCHRDY/MFM select bit. When this bit is 0, the IOCHRDY pin is the IOCHRDY open drain output that extends the host-EPP cycle when required.
When this bit is 1, the MFM pin is selected.

2.5.5 Printer Control Register (PCR, Index = 04h)

This register enables the EPP, ECP, version modes, and interrupt options. On reset all the PCR bits are cleared to 0.

The parallel port mode is software configurable as follows:

TABLE 2-10. Parallel Port Mode

Operation Mode	FER Bit 0	PTR Bit 7	PCR Bit 0	PCR Bit 2
None	0	X	X	X
Compatible	1	0	0	0
Extended	1	1	0	0
EPP	1	X	1	0
ECP	1	X	0	1

Bit 0 EPP enable bit. When this bit is 0, the EPP is disabled, and the EPP registers are not accessible (access ignored).
When this bit is 1, and bit 2 of PCR is 0, the EPP is enabled. Note that the EPP should not be configured with base address 3BCh.

Bit 1 EPP version select bit. When this bit is 0, Version 1.7 is supported.
When this bit is 1, Version 1.9 is supported (IEEE 1284).

Bit 2 ECP enable bit. When this bit is 0, the ECP is disabled and in power mode. The ECP registers are not accessible (access ignored), the ECP interrupt is inactive and the DMA request pin is in TRI-STATE. The IRQ5,7 inputs are blocked to reduce their leakage currents.

When this bit is 1, the ECP is enabled. The software should change this bit to 1 only when bits 0, 1, and 2 of the existing CTR are 1, 0, and 0 respectively.

Bit 3 ECP Clock Freeze Control Bit. In power-down modes 2 and 3: When this bit is 0, the clock provided to the ECP is stopped; and
When this bit is 1, the clock provided to the ECP is not stopped.

Note: When either this bit or the ECP enable bit is 0, there is no change in the PC87334 crystal stopping mechanism.

Bit 4 Reserved. This bit must be set to 0.

Bit 5 Parallel port interrupt (IRQ5 or IRQ7) polarity control bit.

When this bit is 0, the interrupt polarity is as already defined, and the ECP interrupt is level high or negative pulse.

When this bit is 1, the interrupt polarity is inverted.

Bit 6 Parallel port interrupt (IRQ5 or IRQ7) open drain control bit.

When this bit is 0, the configured interrupt line (IRQ5 or IRQ7) has a totem-pole TRI-STATE output.

When this bit is 1, the configured interrupt line has an open drain output (drive low or TRI-STATE, no drive high, no internal pullup).

Bit 7 Reserved. To maintain compatibility with future SuperI/O devices, this bit must not be modified when this register is written. Use read-modify-write to preserve the value of this bit.

2.5.6 Power Management Control Register (PMC, Index = 06h)

This register controls the TRI-STATE and input pins. The PMC Register is accessed through Index 06h. The PMC Register is cleared to 0 on reset.

Bit 0 IDE TRI-STATE control bit. When this bit is 1, and either the IDE is disabled or the SuperI/O is in power-down mode, $\overline{HCS0}$ and $\overline{HCS1}$ are in TRI-STATE. IDED7 input is also blocked to reduce leakage current and its value is undefined when IDE is disabled.

Bit 1 FDC TRI-STATE control bit. When this bit is 1 and the FDC is powered-down, the FDC outputs are in TRI-STATE (except IRQ6, PD, IDLE and the PPM outputs, even if the PPM is used as FDC pins), and the FDC inputs (except $\overline{DSKCHG}$) are blocked to reduce their leakage current.

Bit 2 UARTs TRI-STATE control bit. When this bit is 1, and any UART is powered-down, the outputs of that UART are in TRI-STATE (except IRQ3 and IRQ4), and the inputs are blocked to reduce their leakage current.

The values of the blocked inputs are: SIN = 1, $\overline{CTS}$ = 1, $\overline{DSR}$ = 1, $\overline{DCD}$ = 1 and $\overline{RI}$ = 1.

Bit 3 ECP DMA configuration bit. When this bit is 0, ECP DMA is not configura ble: IDENT/$\overline{PDACK}$ is assumed to be 1 and PDRQ is in TRI-STATE.

When this bit is 1, ECP DMA is configurable via an ECP control register. Pins 54 and 33 are $\overline{PDACK}$ and PDRQ respectively. IDENT is assumed to be 1.

Note: This bit must not be set when the PC87332 is assembled into a PC87312/PC87322 socket, in which pin 33 is $V_{DD}A$.

Bit 4 PD and IDLE (FDC power management output pins) enable bit.

When this bit is 0, pins 43 and 45 are $\overline{MTR1}$ and $\overline{DR1}$ respectively.

When this bit is 1, pins 43 and 45 are IDLE and PD respectively.

Bit 5 Selective Lock bit. This bit enables locking of the following configuration bits: bit 5 of PMC, bit 4 of FER, bits 0–7 of FAR, bits 2–3 of PTR, bits 6–7 of FCR, and bit 0 of TUP. Unlike bit 6 of PTR, it does not lock all the configuration bits.

Once this bit is set by software it can only be cleared by a hardware reset. This bit should be used instead of bit 6 of PTR if a configuration bit should be dynamically modified by software (like PMC bits).

2.0 Configuration Registers (Continued)

When this bit is 0, bit 6 of PTR can be used to lock all configuration registers.

When this bit is 1, the above configuration bits cannot be modified. A hardware reset clears this bit.

Bit 6 Parallel Port Multiplexor (PPM) TRI-STATE enable bit. This bit enables reduction in power consumption, (when the SuperI/O is in power-down mode or the parallel port is disabled) by placing the PPM outputs in TRI-STATE, and blocking the PPM inputs.

When this bit is 0, the parallel port pins are enabled.

When this bit is 1, and either the parallel port is disabled or the SuperI/O is in power-down mode, the outputs of the Parallel Port, pins (except IRQ5 and IRQ7) are in TRI-STATE, and the inputs are blocked to reduce their leakage currents.

The values of the blocked inputs are: BUSY = 1, PE = 0, SLCT = 0, $\overline{ACK}$ = 1 and $\overline{ERR}$ = 1.

Bit 7 Reserved. To maintain compatibility with future SuperI/O devices, this bit must not be modified when this register is written. Use read-modify-write to preserve the value of this bit.

2.5.7 Tape, UARTs and Parallel Port Configuration Register (TUP, Index = 07h)

The TUP Register is cleared to 0XX0000X on reset.

Bit 0 CLK48. Clock divider enable bit.

When a 48 MHz clock is used this bit should be 1. When a 24 MHz clock is used this bit should be 0.

When this bit is 0, the clock for all the PC87332 modules is X1/OSC (i.e., 24 MHz).

When this bit is 1, the clock of all PC87332 modules, except the FDC, is X1/OSC divided by 2 (i.e., 48/2 = 24 MHz), and the FDC clock depends on bit 1 of TUP.

During reset the value of CLK48 pin (pin 57) is latched into this bit.

This bit should not be modified by the user.

Bit 1 FDC's 2 Mbps enable bit.

When this bit is 0, a 2 Mbps data rate is not supported by the FDC, and the FDC clock is 24 MHz (X1/OSC when bit 0 of TUP is 0, or X1/OSC divided by 2 when bit 0 of TUP is 1).

When this bit is 1, 2 Mbps is supported by the FDC, and the FDC clock is 48 MHz (X1/OSC when bit 0 of TUP is 1). Bit 0 of TUP must be set to 1, and a 48 MHz clock must be used to support a 2 Mbps data rate. The operating voltage should be 5V. (See Section 5.0 FDC Functional Description.)

Bit 2 EPP Timeout Interrupt Enable bit.

When this bit is 0, the EPP timeout interrupt is masked.

When this bit is 1, the EPP timeout interrupt is generated on the selected IRQ line (IRQ5 or IRQ7), according to PCR 6.

Bit 3 UART 1 clock divisor control (MIDI baud rate configuration) bit.

When this bit is 0, the UART 1 Baud Rate Generator is fed by the master clock divided by 13.

When this bit is 1, the UART 1 Baud Rate Generator is fed by the master clock divided by 12. This bit should be set to 1 to support MIDI baud rates.

Bit 4 UART 2 clock divisor control (MIDI baud rate configuration) bit.

When this bit is 0, the UART 2 Baud Rate Generator is fed by the master clock divided by 13.

When this bit is 1, the UART 2 Baud Rate Generator is fed by the master clock divided by 12. This bit should be set to 1 to support MIDI baud rates.

Bit 5 PD status bit. This bit holds the FDC power-down state, as defined for the PD pin, even when pin 45 is not configured as PD. This bit is read only.

Bit 6 IDLE status bit. This bit holds the FDC idle state, as defined for the IDLE pin, even when pin 43 is not configured as IDLE, and when IDLE is masked by bit 7 of TUP. This bit is read only.

Bit 7 IDLE pin mask bit. This bit masks the IDLE output pin (but not the IDLE status bit). This bit is ignored when pin 43 is not configured as idle.

When this bit is 0, the IDLE output pin is unmasked. The IDLE pin drives the value of the FDC idle state.

When this bit is 1, the IDLE output pin is masked. The IDLE pin is driven low.

2.5.8 SuperI/O Identification Register (SID, Index = 08h)

The SID Register is accessed, like the other configuration registers, through the Index Register. This read-only register is used to identify the PC87332 device.

7	6	5	4	3	2	1	0	
0	0	0	1	X	X	X	X	Super I/O Identification Reg. (SID) Index = 08h

2.6 POWER-DOWN OPTIONS

The PC87332 places special emphasis on power management. Power management methods can be divided into two major groups:

Group 1: Full device power-down—the entire PC87332 SuperI/O is powered-down and thus disabled.

Group 2: Specific function power-down—specific SuperI/O modules (FDC, UART1, UART2, IDE, ECP or Parallel Port) are powered-down and thus disabled.

All power-down modes are enhanced by a new feature which allows the output pins associated with a specific function (FDC, UART1, UART2, IDE, Parallel Port) to be TRI-STATE pins, and reduces current leakage by blocking their inputs.

Four modules in the PC87332 are operated by the internal clock—FDC, UART1, UART2 and ECP. These modules can be powered-down or disabled by stopping their associated internal clocks. In addition, all four modules can be powered-down or disabled by stopping the external crystal oscillator.

Modules which do not use a clock, the IDE and Parallel Port (SPP/EPP), can be powered-down or disabled by simply blocking access to them.

All the above power-down modes can be achieved using the power-down methods from Group 1 or Group 2, as described in the following sections.

2.0 Configuration Registers (Continued)

2.6.1 Recommended Power-Down Methods—Group 1

Use the power-down methods in Group 1 to place the PC87332 in one of the following modes:

Mode 1: The entire chip is powered-down, the crystal oscillator is stopped, pins are TRI-STATE and the inputs are blocked.

In this mode the maximum current saving can be achieved.

Mode 2: The entire chip is powered-down, the crystal oscillator is stopped. Pins are driven.

Mode 3: The entire chip is powered-down, pins are TRI-STATE, and the inputs are blocked. The crystal oscillator operates, and provides fast wake-up.

Mode 4: The entire chip is powered-down. Pins are driven. The crystal oscillator operates.

There are 13 methods to reach the above four operating modes. See Table 2-11.

2.6.2 Recommended Power-Down Methods—Group 2

Use the power-down modes in Group 2 to place the PC87332 in any desired combination of the following power-down modes:

Mode 1: Parallel Port (SPP/EPP/ECP) is powered-down, providing a savings of up to 5 mA.

Mode 2: UARTs are powered-down providing a savings of up to 5 mA.

Mode 3: FDC is powered-down, providing a savings of up to 4 mA.

Mode 4: IDE is powered-down, providing a savings of up to 0.1 mA.

See also the PMC register.

2.7 POWER-UP PROCEDURE AND CONSIDERATIONS

2.7.1 Crystal Stabilization

If the crystal is stopped by putting either the FDC or both UARTs into low power mode, then a finite amount of time (~8 ms) must be allowed for crystal stabilization during subsequent power-up. The stabilization period can be sensed by reading the Main Status Register in the FDC, if the FDC is being powered up. (The Request for Master bit is not set for ~8 ms.) If either one of the UARTs are being powered up, but the FDC is not, then the software must determine the ~8 ms crystal stabilization period. Stabilization of the crystal can also be sensed by putting the UART into local loopback mode and sending bytes until they are received correctly.

2.7.2 UART Power-Up

The clock signal to the UARTs is controlled through the Configuration Registers (FER, PTR). In order to restore the clock signal to one or both UARTs the following conditions must exist:

1. The appropriate enable bit (FER1,2) for the UART(s) must be set.
2. The Power-Down bit (PTR0) must not be set.
3. If the PWDN pin option (PTR2 and FCR6) is used the $\overline{\text{CSOUT}}$/PWDN/$\overline{\text{ZWS}}$ pin must be inactive.

If the crystal has been stopped follow the guidelines in Section 2.7.1 before sending data or signaling that the receiver channel is ready.

TABLE 2-11. Methods to Achieve Group 1 Power-Down Modes

Method	PTR Bits 012	Pin 3 (Note 3)	FER Bits 01236	PCR Bit 2	PMC Bits 0126	Mode	Typical Current Consumption (Notes 4, 5)
1	11x	x	xxxxx	x	1111	#1	10 μA
2	x10	0	xxxxx	x	1111		
3	x1x	x	00000	0	1111		
4	11x	x	xxxxx	x	0000	#2	30 μA
5	x10	0	xxxxx	x	0000		
6	x1x	x	00000	0	0000		
7	x1x	x	xxx1x	x	0000	(Notes 1, 2)	
8	10x	x	xxxxx	x	1111	#3	4 mA
9	x00	0	xxxxx	x	1111		
10	x0x	x	00000	0	1111		
11	10x	x	xxxxx	x	0000	#4	4 mA
12	x00	0	xxxxx	x	0000		
13	x0x	x	00000	0	0000	(Note 1)	

Note 1: The PC87332 can also be placed in Mode 2, or Mode 4, using the strap configuration pins CFG0–4 (see Table 2-1).

Note 2: The PC87332 can also be placed in Mode 2 by using method #7, and entering FDC Low Power by executing Mode Command or by setting bit 6 of DSR to high.

Note 3: Pin #3 is PDWN input (configured when bit 2 of PTR is 0 and bit 6 of FCR is 1).

Note 4: These values are measured under the following conditions:

1. No load on outputs
2. Inputs are stable
3. $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$
4. $V_{DD} = 3.3V$
5. Using a crystal for the 24 MHz clock.

Note 5: UARTS should be in 16550 (FIFO) mode; bit 0 of FIFO Control Register should be 1.

2.0 Configuration Registers (Continued)

2.7.3 FDC Power-Up

The clock signal to the FDC is controlled through the Configuration Registers, the FDC Mode Command and the Data Rate Select Register. In order to restore the clock signal to the FDC the following conditions must exist:

1. The appropriate enable bit (FER3) must be set.
2. The Power-Down bit (PTR0) must not be set.
3. If the PWDN pin option (PTR2 and FCR 6) is used, the $\overline{PWDN}/\overline{ZWS}$ pin must be inactive.

In addition to these conditions, one of the following actions must be taken to initiate recovery from the Power-Down mode:

1. Read the Main Status Register until the RQM bit (MSR7) is set OR
2. Write to the Data Rate Select Register and set the Software Reset bit (DSR7) OR
3. Write to the Digital Output Register, clear and then set the Reset bit (DOR2) OR
4. Read the Data Register and the Main Status Register until the RQM bit is set.

If the crystal has been stopped, read the RQM bit in the Main Status Register until it is set. The RQM bit is not set until the crystal has stabilized.

3.0 FDC Register Description

The floppy disk controller (FDC) is suitable for all PC-AT, EISA, PS/2, and general purpose applications. The operational mode (PC-AT, PS/2, or Model 30) of the FDC is determined by hardware strapping of the IDENT and MFM pins. DP8473 and N82077 software compatibility is provided. Key features include a 16-byte FIFO, PS/2 diagnostic register support, perpendicular recording mode, CMOS disk interface, and a high performance digital data separator. See *Figure 3-1*.

The FDC supports fast 2 Mbps data rate drives and standard 1 Mbps, 250/500 kbps and 300/500 kbps data rate drives. The 1 Mbps data rate is used by the high performance tape and floppy disk drives. The 2 Mbps data rate is used in very high performance tape drives. The FDC also supports the perpendicular recording mode, a new format used with some high performance, high capacity disk drives at the 1 Mbps data rate.

The high performance internal digital data separator needs no external components. It improves on the window margin performance standards of the DP8473, and is compatible with the strict data separator requirements of floppy disk and floppy-tape drives.

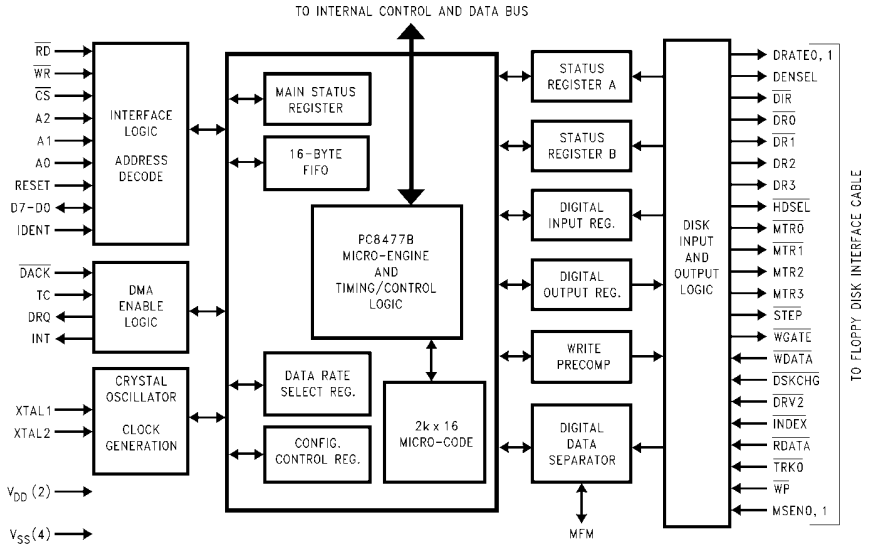
The FDC contains write precompensation circuitry that defaults to 125 ns for 250 kbps, 300 kbps, and 500 kbps, to 41.67 ns for 1 Mbps and to 20.8 ns for 2 Mbps. These values can be overridden in software to disable write precompensation or to provide levels of precompensation up to 250 ns.

The FDC has internal 24 mA data bus buffers which allow direct connection to the system bus. The internal 40 mA totem-pole disk interface buffers are compatible with both CMOS drive inputs and 150Ω resistor terminated disk drive inputs.

3.1 FDC CONTROL REGISTERS

The following FDC registers are mapped into the addresses shown in Table 3-1 and described in the following sections. The base address range is provided by the on-chip address decoder pin. For PC-AT or PS/2 applications, the diskette controller primary address range is 3F0h to 3F7h, and the secondary address range is 370h to 377h. The FDC supports three different register modes: the PC-AT mode, PS/2 mode (MicroChannel systems), and the Model 30 mode. See Section 5.2 for more details on how each register mode is enabled. When applicable, the register definition for each mode of operation is given.

If no special notes are made, then the register is valid for all three register modes.



TL/C/11930–6

FIGURE 3-1. FDC Functional Block Diagram

3.0 FDC Register Description (Continued)

TABLE 3-1. Register Description and Addresses

A2	A1	A0	IDENT	R/W	Register	
0	0	0	0	R	Status Register A*	SRA
0	0	1	0	R	Status Register B*	SRB
0	1	0	X	R/W	Digital Output Register	DOR
0	1	1	X	R/W	Tape Drive Register	TDR
1	0	0	X	R	Main Status Register	MSR
1	0	0	X	W	Data Rate Select Register	DSR
1	0	1	X	R/W	Data Register (FIFO)	FIFO
1	1	0	X	X	None (Bus TRI-STATE)	
1	1	1	X	R	Digital Input Register	DIR
1	1	1	X	W	Configuration Control Register	CCR

*Note: SRA and SRB are enabled by IDENT = 0 during a chip reset only.

3.1.1 Status Register A (SRA) Read Only

This read-only diagnostic register is part of the PS/2 floppy controller register set, and is enabled when in the PS/2 or Model 30 mode. This register monitors the state of the IRQ6 pin and some of the disk interface signals. The SRA can be read at any time when in PS/2 mode. In the PC-AT mode, D7–D0 are TRI-STATE during a μP read.

SRA—PS/2 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	IRQ6 PEND	$\overline{\text{DRV2}}$	STEP	$\overline{\text{TRK0}}$	HDSEL	$\overline{\text{INDX}}$	$\overline{\text{WP}}$	DIR
RESET COND	0	N/A	0	N/A	0	N/A	N/A	0

D7 **Interrupt Pending:** This active high bit reflects the state of the IRQ6 pin.

D6 **$\overline{\text{2nd Drive Installed}}$:** Active low status of the DRV2 disk interface input, indicating if a second drive has been installed.

D5 **Step:** Active high status of the STEP disk interface output.

D4 **$\overline{\text{Track 0}}$:** Active low status of the TRK0 disk interface input.

D3 **Head Select:** Active high status of the HDSEL disk interface output.

D2 **$\overline{\text{Index}}$:** Active low status of the INDEX disk interface input.

D1 **$\overline{\text{Write Protect}}$:** Active low status of the WP disk interface input.

D0 **Direction:** Active high status of the DIR disk interface output.

SRA— Model 30 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	IRQ6 PEND	DRQ	STEP	TRK0	$\overline{\text{HDSEL}}$	INDX	WP	$\overline{\text{DIR}}$
RESET COND	0	0	0	N/A	1	N/A	N/A	1

D7 **Interrupt Pending:** This active high bit reflects that state of the IRQ6 pin.

D6 **DMA Request:** Active high status of the DRQ signal.

D5 **Step:** Active high status of the latched STEP disk interface output. This bit is latched with the STEP output going active, and is cleared with a read from the DIR, or with a hardware or software reset.

D4 **Track 0:** Active high status of TRK0 disk interface input.

D3 **$\overline{\text{Head Select}}$:** Active low status of the HDSEL disk interface output.

D2 **Index:** Active high status of the INDEX disk interface input.

D1 **Write Protect:** Active high status of the WP disk interface input.

D0 **$\overline{\text{Direction}}$:** Active low status of the DIR disk interface output.

3.1.2 Status Register B (SRB) Read Only

This read-only diagnostic register is part of the PS/2 floppy controller register set, and is enabled when in the PS/2 or Model 30 mode. The SRB can be read at any time when in PS/2 mode. In the PC-AT mode, D7–D0 are TRI-STATE during a μP read.

SRB—PS/2 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	1	1	DR0	WDATA	RDATA	WGATE	MTR1	MTR0
RESET COND	N/A	N/A	0	0	0	0	0	0

D7 **Reserved:** Always 1.

D6 **Reserved:** Always 1.

D5 **Drive Select 0:** Reflects the status of the Drive Select 0 bit in the DOR (address 2, bit 0). It is cleared after a hardware reset, not a software reset.

D4 **Write Data:** Every inactive edge transition of the WDATA disk interface output causes this bit to change states.

D3 **Read Data:** Every inactive edge transition of the RDATA disk interface output causes this bit to change states.

D2 **Write Gate:** Active high status of the WGATE disk interface output.

D1 **Motor Enable 1:** Active high status of the MTR1 disk interface output. Low after a hardware reset, unaffected by a software reset.

D0 **Motor Enable 0:** Active high status of the MTR0 disk interface output. Low after a hardware reset, unaffected by a software reset.

SRB—Model 30 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	$\overline{\text{DRV2}}$	$\overline{\text{DR1}}$	$\overline{\text{DR0}}$	WDATA	RDATA	WGATE	$\overline{\text{DR3}}$	$\overline{\text{DR2}}$
RESET COND	N/A	1	1	0	0	0	1	1

D7 **$\overline{\text{2nd Drive Installed}}$**: Active low status of the DRV2 disk interface input.

D6 **$\overline{\text{Drive Select 1}}$:** Active low status of the DR1 disk interface output.

D5 **$\overline{\text{Drive Select 0}}$:** Active low status of the DR0 disk interface output.

3.0 FDC Register Description (Continued)

D4 **Write Data:** Active high status of latched WDATA signal. This bit is latched by the inactive going edge of WDATA and is cleared by a read from the DIR. This bit is not gated by WGATE.

D3 **Read Data:** Active high status of latched RDATA signal. It is latched by the inactive going edge of RDATA and is cleared by a read from the DIR.

D2 **Write Gate:** Active high status of latched WGATE signal. This bit is latched by the active going edge of WGATE and is cleared by a read from the DIR.

D1 **$\overline{\text{Drive Select 3}}$:** Active low status of the DR3 disk interface output.

Note: The MTR3, MTR2, DRV3, DRV2 pins are only available in four drive mode (bit 4 of FER is 1) and require external logic.

D0 **$\overline{\text{Drive Select 2}}$:** Active low status of the DR2 disk interface output.

Note: The MTR3, MTR2, DRV3, DRV2 pins are only available in four drive mode (bit 4 of FER is 1) and require external logic.

3.1.3 Digital Output Register (DOR) Read/Write

The DOR controls the drive select and motor enable disk interface outputs, enables the DMA logic, and contains a software reset bit. The contents of the DOR are set to 00h after a hardware reset, and is unaffected by a software reset. The DOR can be written to at any time.

DOR

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	MTR3	MTR2	MTR1	MTR0	DMAEN	RESET	DRIVE SEL 1	DRIVE SEL 0
RESET COND	0	0	0	0	0	0	0	0

D7 **Motor Enable 3:** This bit controls the MTR3 disk interface output. A 1 in this bit causes the MTR3 pin to go active.

D6 **Motor Enable 2:** Same function as D7 except for MTR2.

D5 **Motor Enable 1:** Same function as D7 except for MTR1. (See bit 4 of FCR for further information.)

D4 **Motor Enable 0:** Same function as D7 except for MTR0. (See bit 4 of FCR for further information.)

D3 **DMA Enable:** This bit has two modes of operation.

PC-AT mode or Model 30 mode: Writing a 1 to this bit enables the DRQ, $\overline{\text{DACK}}$, TC, and IRQ6 pins. Writing a 0 to this bit disables the $\overline{\text{DACK}}$ and TC pins and puts the DRQ and the IRQ6 pins in TRI-STATE. D3 is a 0 after a reset when in these modes.

PS/2 mode: This bit is reserved, and the DRQ, $\overline{\text{DACK}}$, TC, and IRQ6 pins are always enabled. During a reset, the DRQ, $\overline{\text{DACK}}$, TC, and IRQ6 lines remain enabled, and D3 is 0.

D2 **Reset Controller:** Writing a 0 to this bit resets the controller. It remains in the reset condition until a 1 is written to this bit. A software reset does not affect the DSR, CCR, and other bits of the DOR. A software reset affects the Configure and Mode command bits (See Section 4.0 FDC Command Set Description). The minimum time that this bit must be low is 100 ns. Thus, toggling the Reset Controller bit during consecutive writes to the DOR is an acceptable method of issuing a software reset.

D1,D0 **Drive Select:** These two bits are binary encoded for the four drive selects DR0–DR3, so that only one drive select output is active at a time. (See bit 4 of FCR for further information.)

It is common programming practice to enable both the motor enable and drive select outputs for a particular drive. Table 3-2 below shows the DOR values which enable each of the four drives.

TABLE 3-2. Drive Enable Values

Drive	DOR Value
0	1Ch
1	2Dh
2	4Eh
3	8Fh

Note: The MTR3, MTR2, DRV3, DRV2 pins are only available in four drive mode (bit 4 of FER is 1) and require external logic.

3.1.4 Tape Drive Register (TDR) Read/Write

This register is used to assign a particular drive number to the tape drive support mode of the data separator. All other logical drives can be assigned as floppy drive support. Any future reference to the assigned tape drive invokes tape drive support. The TDR is unaffected by a software reset. This register holds the media sense information of the floppy disk drive. When bit 0 of FCR is 1, bits 2–7 of TDR are TRI-STATE during read.

TDR

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	ED	HD	Valid Data	X	X	X	TAPE SEL 1	TAPE SEL 0
RESET COND	X	X	X	N/A	N/A	N/A	0	0

D7 **Extra Density:** When bit 5 is 0, this media ID bit is used with bit 6 to indicate the type of media currently in the active floppy drive. If bit 5 is 1, it is invalid. This bit holds MSEN1 pin value. When PPM is enabled and PNF is 0, it holds the PD7 pin value. See Table 3-3 for details regarding bits 5–7.

D6 **High Density;** When bit 5 is 0, this media ID bit is used with bit 7 to indicate the type of media currently in the active floppy drive. If bit 5 is 1, it is invalid. This bit holds MSEN0/DRATE0 pin value. When PPM is enabled and PNF is 0, it holds the PD5 pin value. See Table 3-3 for details regarding bits 5–7.

Note: Bits 6 and 7 of TDR are undefined when DRID0,1 pins are configured as DRATE0,1.

D5 **Valid Data:** The state of bit 5 is determined by the state of the $\overline{\text{VLD0,1}}$ pins during reset. If this bit is 0, there is valid media ID sense data in bits 7 and 6 of this register. Bit 5 holds $\overline{\text{VLD0}}$ when drive 0 is accessed, and media sense is configured. It holds $\overline{\text{VLD1}}$ when drive 1 is accessed, and media sense is configured. Otherwise, it is set to 1 to indicate that media information is not available. See Table 3-3 for details regarding bits 5–7.

3.0 FDC Register Description (Continued)

D4–2 **Reserved.** These bits are ignored.

D1, 0 **Tape Select 1,0:** These bits assign a logical drive number to a tape drive. Drive 0 is not available as a tape drive, and is reserved as the floppy disk boot drive. See Table 3-4 for the tape drive assignment values.

TABLE 3-3. Media ID Bit Functions

Bit 7	Bit 6	Bit 5	Media Type
X	X	1	Invalid Data
0	0	0	5.25″
0	1	0	2.88M
1	0	0	1.44M
1	1	0	720k

TABLE 3-4. Tape Drive Assignment Values

TAPESEL1	TAPESEL0	Drive Selected
0	0	None
0	1	1
1	0	2
1	1	3

3.1.5 Main Status Register (MSR) Read Only

The read-only Main Status Register (MSR) indicates the current status of the disk controller. The MSR is always available to be read. One of its functions is to control the flow of data to and from the Data Register (FIFO). The MSR indicates when the disk controller is ready to send or receive data through the Data Register. It should be read before each byte is transferred to or from the Data Register except during a DMA transfer. No delay is required when reading this register after a data transfer.

After a hardware or software reset, or recovery from a power-down state, the MSR is immediately available to be read by the μP. It contains a value of 00h until the oscillator circuit has stabilized, and the internal registers have been initialized. When the FDC is ready to receive a new command, it reports an 80h to the μP. The system software can poll the MSR until it is ready. The worst case time allowed for the MSR to report an 80h value (RQM set) is 2.5 μs after reset or power-up.

MSR

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	RQM	DIO	NON DMA	CMD PROG	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY
RESET COND	0	0	0	0	0	0	0	0

D7 **Request for Master:** Indicates that the controller is ready to send or receive data from the μP through the FIFO. This bit is cleared immediately after a byte transfer and is set again as soon as the disk controller is ready for the next byte. During a Non-DMA Execution phase, the RQM indicates the status of the interrupt pin.

D6 **Data I/O (Direction):** Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the Data Register.

D5 **Non-DMA Execution:** Indicates that the controller is in the Execution Phase of a byte transfer operation in the Non-DMA mode. This mode can be used for multiple byte transfers by the μP in the Execution Phase via interrupts or software polling.

D4 **Command in Progress:** This bit is set after the first byte of the Command Phase is written. This bit is cleared after the last byte of the Result Phase is read. If there is no Result Phase in a command, the bit is cleared after the last byte of the Command Phase is written.

D3 **Drive 3 Busy:** Set after the last byte of the Command Phase when a Seek or Recalibrate command is issued for drive 3. Cleared after reading the first byte in the Result Phase of the Sense Interrupt Command for this drive.

D2 **Drive 2 Busy:** Same as D3 above, but for drive 2.

D1 **Drive 1 Busy:** Same as D3 above, but for drive 1.

D0 **Drive 0 Busy:** Same as D3 above, but for drive 0.

3.1.6 Data Rate Select Register (DSR) Write Only

This write-only register is used to program the data rate, amount of write precompensation, power-down mode and software reset. The data rate is programmed via the CCR, not the DSR, for PC-AT, Model 30 and MicroChannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is determined by the most recent write to either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset sets the DSR to 02h, which corresponds to the default write precompensation setting and a 250 kbps data rate.

DSR

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	S/W RESET	LOW POWER	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE1	DRATE0
RESET COND	0	0	0	0	0	0	1	0

D7 **Software Reset:** This bit has the same function as the DOR RESET (D2, see Section 3.3) except that this software reset is self-clearing.

D6 **Low Power:** Placing a 1 in this bit puts the controller into the Manual Low Power mode. The oscillator and data separator circuits are turned off. Manual Low Power can also be accessed via the Mode command. The chip comes out of low power after a software reset, or access to the Data Register or Main Status Register.

D5 Undefined. Should be set to 0.

D4–2 Precompensation Select: These three bits select the amount of write precompensation the floppy controller uses on the WDATA disk interface output. Table 3-5 shows the amount of precompensation used for each bit pattern. In most cases, the default values (Table 3-6) can be used; however, alternate values can be chosen for specific types of drives and media. Track 0 is the default starting track number for precompensation. The starting track number can be changed in the Configure command.

TABLE 3-5. Write Precompensation Delays

Bits 4, 3, 2	Precompensation Delay	
	TUP Bit 0 = 1 24 MHz	TUP Bit 1 = 1 48 MHz
111	0.0 ns	0.0 ns
001	41.7 ns	20.8 ns
010	83.3 ns	41.7 ns
011	125.0 ns	62.5 ns
100	166.7 ns	83.3 ns
101	208.3 ns	104.2 ns
110	250.0 ns	125.0 ns
000	DEFAULT	DEFAULT

TABLE 3-6. Default Precompensation Delays

Data Rate	Precompensation Delay (24 MHz and 48 MHz)
2 Mbps	20.8 ns
1 Mbps	41.7 ns
500 kbps	125.0 ns
300 kbps	125.0 ns
250 kbps	125.0 ns

D1–0 Data Rate Select 1,0: These bits determine the data rate for the floppy controller. See Table 3-7 for the corresponding data rate for each D1,0 value pair. The data rate select bits are unaffected by a software reset, and are set to 250 kbps after a hardware reset.

TABLE 3-7. Data Rate Select Encoding

TUP Bit 1	Data Rate Select		MFM
	1	0	
0	1	1	1 Mbps
0	0	0	500 kbps
0	0	1	300 kbps
0	1	0	250 kbps
1	1	1	2 Mbps*
1	0	0	Illegal
1	0	1	Illegal
1	1	0	Illegal

*This feature is not tested.

3.1.7 Data Register (FIFO) Read/Write

The FIFO (read/write) is used to transfer all commands, data, and status between the μP and the FDC. During the Command Phase, the μP writes the command bytes into the FIFO after polling the RQM and DIO bits in the MSR. During the Result Phase, the μP reads the result bytes from the FIFO after polling the RQM and DIO bits in the MSR.

Enabling the FIFO, and setting the FIFO threshold, is done via the Configure command. If the FIFO is enabled, only the Execution Phase byte transfers use the 16-byte FIFO. The FIFO is always disabled during the Command and Result Phases of a controller operation. A software reset will not disable enabled FIFO if the Lock bit is set in the Lock Command. After a hardware reset, the FIFO is disabled to maintain compatibility with PC-AT systems.

The 16-byte FIFO can be used for DMA, Interrupt, or software polling type transfers during the execution of a read, write, format, or scan command. In addition, the FIFO can be put into a Burst or Non-Burst mode with the Mode command. In the Burst mode, DRQ or IRQ6 remains active until all of the bytes have been transferred to or from the FIFO. In the Non-Burst mode, DRQ or IRQ6 is deasserted for 350 ns to allow higher priority transfer requests to be serviced.

3.0 FDC Register Description (Continued)

The Mode command can also disable the FIFO for either reads or writes separately. The FIFO allows the system a larger latency without causing a disk overrun/underrun error. The FIFO is typically utilized with multitasking operating systems and/or when running systems at or above a 1 Mbps data rate. In its default state, the FIFO is disabled and contains a zero threshold. The default state is entered after a hardware reset.

Data Register (FIFO)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	Data [7:0]							
RESET COND	Byte Mode							

During the Execution Phase of a command involving a data transfer to/from the FIFO, the system must respond to a data transfer service request based on the following formula:

Maximum Allowable Data Transfer Service Time

$$[(\text{THRESH} + 1) \times 8 \times t_{DRP}] - (16 \times t_{ICP})$$

This formula is good for all data rates with the FIFO enabled or disabled. THRESH is a four bit value programmed in the Configure command, which sets the FIFO threshold. If the FIFO is disabled, THRESH is zero in the above formula. The last term of the formula, $(16 \times t_{ICP})$ is an inherent delay due to the microcode overhead required by the FDC. This delay is also data rate dependent. See Table 9-1 for the t_{DRP} and t_{ICP} times. See Section 9.3.2 for a description of t_{DRP} and t_{ICP}.

The programmable FIFO threshold (THRESH) is useful in adjusting the floppy controller to the speed of the system. In other words, a slow system with a sluggish DMA transfer capability uses a high value of THRESH, giving the system more time to respond to a data transfer service request (DRQ for DMA mode or IRQ6 for Interrupt mode). Conversely, a fast system with quick response to a data transfer service request uses a low value of THRESH.

3.1.8 Digital Input Register (DIR) Read Only

This diagnostic register is used to detect the state of the DSKCHG disk interface input and some diagnostic signals. The function of this register depends on its mode of operation. When in the PC-AT mode, the D6–0 are TRI-STATE to avoid conflict with the fixed disk status register at the same address. DIR is unaffected by a software reset.

DIR—PC-AT Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	DSKCHG	X	X	X	X	X	X	X
RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D7 **Disk Changed:** Active high status of DSKCHG disk interface input. During power-down this bit is invalid if it is read by the software.

D6–0 **Unused** by the FDC (at TRI-STATE). The bits are used by the Hard Disk Controller Status Register.

DIR—PS/2 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	DSKCHG	1	1	1	1	DRATE1	DRATE0	$\overline{\text{HIGH DEN}}$
RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

D7 **Disk Changed:** Active high status of DSKCHG disk interface input. During power-down this bit is invalid if it is read by the software.

D6–3 **Reserved:** Always 1.

D2–1 **Data Rate Select 1,0:** These bits indicate the status of the DRATE1–0 bits programmed through the DSR or CCR.

D0 **$\overline{\text{High Density}}$:** This bit is low when the 1 Mbps/2 Mbps or 500 kbps data rate is chosen, and high when the 300 kbps or 250 kbps data rate is chosen. This bit is independent of the IDENT value.

DIR—Model 30 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	$\overline{\text{DSKCHG}}$	0	0	0	DMAEN	NOPRE	DRATE1	DRATE0
RESET COND	N/A	0	0	0	0	0	1	0

D7 **$\overline{\text{Disk Changed}}$:** Active low status of DSKCHG disk interface input. During power-down this bit is invalid if it is read by the software.

D6–4 **Reserved:** Always 0.

D3 **DMA Enable:** Active high status of the DMAEN bit in the DOR.

D2 **No Precompensation:** Active high status of the NOPRE bit in the CCR.

D1–0 **Data Rate Select 1,0:** These bits indicate the status of the DRATE 1–0 bits programmed through the DSR or CCR.

3.1.9 Configuration Control Register (CCR) Write Only

This is the write-only data rate register commonly used in PC-AT applications. This register is not affected by a software reset and is set to 250 kbps after a hardware reset. The data rate of the floppy controller is determined by the last write to either the CCR or DSR.

CCR—PC-AT and PS/2 Modes

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	0	0	0	0	0	0	DRATE1	DRATE0
RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	1	0

D7–2 **Reserved:** Should be set to 0.

D1–0 **Data Rate Select 1,0:** These bits determine the data rate of the floppy controller. See Table 3-7 for the appropriate values.

3.0 FDC Register Description (Continued)

CCR—Model 30 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	0	0	0	0	0	NOPRE	DRATE1	DRATE0
RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	1	0

D7–3 **Reserved:** Should be set to 0.

D2 **No Precompensation:** This bit can be set by software, to indicate no precompensation. It can be read by bit D2 of the DIR when in the Model 30 register mode. This bit is unaffected by a software reset.

D1–0 **Data Rate Select 1,0:** These bits determine the data rate of the floppy controller. See Table 3-7 for the appropriate values.

3.2 RESULT PHASE STATUS REGISTERS

The Result Phase of a command contains bytes that hold status information. The format of these bytes are described below. Do not confuse these status bytes with the Main Status Register, which is a read only register that is always valid. The Result Phase status registers are read from the Data Register (FIFO) only during the Result Phase of certain commands (see Section 4.1 Command Set Summary). The status of each register bit is indicated when the bit is a 1.

3.2.1 Status Register 0 (ST0)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	IC	IC	SE	EC	0	HDS	DS1	DS0
RESET COND	0	0	0	0	0	0	0	0

D7–6 **Interrupt Code:**

00 = Normal Termination of Command.

01 = Abnormal Termination of Command. Execution of command was started, but was not successfully completed.

10 = Invalid Command Issued. Command issued was not recognized as a valid command.

11 = Internal drive ready status changed state during the drive polling mode. Only occurs after a hardware or software reset.

D5 **Seek End:** Seek, Relative Seek, or Recalibrate command completed by the controller. (Used during a Sense Interrupt command.)

D4 **Equipment Check:** After a Recalibrate command, Track 0 signal failed to occur. (Used during Sense Interrupt command.)

D3 Not Used. Always 0.

D2 **Head Select:** Indicates the active high status of the HDSEL pin at the end of the Execution Phase.

D1–0 **Drive Select 1,0:** These two binary encoded bits indicate the logical drive selected at the end of the Execution Phase.

00 = Drive 0 selected.

01 = Drive 1 selected.

10 = Drive 2 selected.

11 = Drive 3 selected.

3.2.2 Status Register 1 (ST1)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	ET	0	CE	OR	0	ND	NW	MA
RESET COND	0	0	0	0	0	0	0	0

D7 **End of Track:** Controller transferred the last byte of the last sector without the Terminal Count (TC) pin 6/4 (PQFP/TQFP) becoming active. The last sector is the End of Track sector number programmed in the Command Phase.

D6 Not Used. Always 0.

D5 **CRC Error:** If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the Address Field of the correct sector. If bit 5 of ST2 is also set, then there was a CRC error in the Data Field.

D4 **Overrun:** Controller was not serviced by the μP soon enough during a data transfer in the Execution Phase. For read operations, indicates a data overrun. For write operations, indicates a data underrun.

D3 Not Used. Always 0.

D2 **No Data:** Three possible problems:

1. Controller cannot find the sector specified in the Command Phase during the execution of a Read, Write, Scan, or Verify command. An address mark was found however, so it is not a blank disk.
2. Controller cannot read any Address Fields without a CRC error during a Read ID command.
3. Controller cannot find starting sector during execution of Read A Track command.

D1 **Not Writable:** Write Protect pin is active when a Write or Format command is issued.

D0 **Missing Address Mark:** If bit 0 of ST2 is clear then the controller cannot detect any Address Field Address Mark after two disk revolutions. If bit 0 of ST2 is set then the controller cannot detect the Data Field Address Mark after finding the correct Address Field.

3.2.3 Status Register 2 (ST2)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	0	CM	CD	WT	SEH	SNS	BT	MD
RESET COND	0	0	0	0	0	0	0	0

D7 Not Used. Always 0.

D6 **Control Mark:** Controller tried to read a sector which contained a deleted data address mark during execution of Read Data or Scan commands. Or, if a Read Deleted Data command was executed, a regular address mark was detected.

D5 **CRC Error in Data Field:** Controller detected a CRC error in the Data Field. Bit 5 of ST1 is also set.

D4 **Wrong Track:** Only set if desired sector is not found, and the track number recorded on any sector of the current track is different from the track address specified in the Command Phase.

D3 **Scan Equal Hit:** ''Equal'' condition satisfied during any Scan command.

3.0 FDC Register Description (Continued)

D2 **Scan Not Satisfied:** Controller cannot find a sector on the track which meets the desired condition during any Scan command.

D1 **Bad Track:** Only set if the desired sector is not found, the track number recorded on any sector on the track is FFh indicating a hard error in IBM® format, and is different from the track address specified in the Command Phase.

D0 **Missing Address Mark in Data Field:** Controller cannot find the Data Field Address Mark (AM) during a Read, Scan, or Verify command. Bit 0 of ST1 is also set.

3.2.4 Status Register 3 (ST3)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	0	WP	1	TK0	1	HDS	DS1	DS0
RESET COND	0	0	1	0	1	0	0	0

D7 Not Used. Always 0.

D6 **Write Protect:** Indicates active high status of the WP pin.

D5 Not Used. Always 1.

D4 **Track 0:** Indicates active high status of the TRK0 pin.

D3 Not Used. Always 1.

D2 **Head Select:** Indicates the active high status of the HD bit in the Command Phase.

D1–0 **Drive Select 1,0:** These two binary encoded bits indicate the DS1–0 bits in the Command Phase.

4.0 FDC Command Set Description

This section presents the FDC command set—full description in Section 4.1 and a working summary in Section 4.2. Each command contains a unique first command byte, the opcode byte, which tells the controller how many (0 or more) command bytes to expect. The information for each command is displayed using the structure shown in *Figure 4-1*.

If an invalid command byte is issued to the controller, it immediately enters the Result Phase and the status is 80h signifying an Invalid Command.

I/O Operation

Opcode
Command Byte 1
Command Byte 2
. . .
Command Byte n

FIGURE 4-1. FDC Command Structure

4.1 COMMAND DESCRIPTIONS

4.1.1 Configure Command

The Configure Command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power-up. These bits are set to their default values after a hardware reset. The value of each bit after a software reset is explained. The default value of each bit is denoted by a ''bullet'' to the left of each item.

Command Phase:

0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	FIFO	POLL	THRESH			
PRETRK							

Execution Phase: Internal registers written.

Result Phase: None.

EIS: Enable Implied Seeks. Default after a software reset.

- **•0** = Implied seeks disabled through Configure command. Implied seeks can still be enabled through the Mode command when EIS = 0.
- **1** = Implied seeks enabled for a read, write, scan, or verify operation. A seek and sense interrupt operation is performed prior to the execution of the read, write, scan, or verify operation. The IPS bit does not need to be set.

FIFO: Enable FIFO for Execution Phase data transfers. Default after a software reset if the LOCK bit is 0. If the LOCK bit is 1, then the FIFO bit retains its previous value after a software reset.

- **0** = FIFO enabled for both reads and writes.
- **•1** = FIFO disabled.

POLL: Disable for Drive Polling Mode. Default after a software reset.

- **•0** = Enable drive polling mode. An interrupt is generated after a reset.
- **1** = Disable drive polling mode. If the Configure command is issued within 500 μs of a hardware or software reset, then an interrupt is not generated. In addition, the use of the four Sense Interrupt commands to clear the ''Ready Changed State'' of the four logical drives is not required.

THRESH: The FIFO threshold in the Execution Phase of read and write data transfers. Programmable from 00h to 0Fh. Defaults to 00h after a software reset if the LOCK bit is 0. If the LOCK bit is 1, THRESH retains its value. A high value of THRESH is suited for slow response systems, and a low value of THRESH is better for fast response systems.

PRETRK: Starting track number for write precompensation. Programmable from track 0 (''00'') to track 255 (''FF''). Defaults to track 0 (''00'') after a software reset if the LOCK bit is 0. If the LOCK bit is 1, then PRETRK retains its value.

4.1.2 Dumpreg Command

The Dumpreg command is designed to support system runtime diagnostics, application software development and debug. This command has a one-byte command phase and a 10-byte result phase. The Result Phase returns the values of parameters set in other commands. That is, the PTR (Present Track Register) contains the least significant byte of the track the microcode has stored for each drive. The Step Rate Time, Motor Off and Motor On Times, and the DMA bit are all set in the Specify command.

The sixth byte of the result phase varies depending on what commands have been previously executed. If a format command has previously been issued, and no reads or writes have been issued since then, this byte contains the Sectors per track value. If a read or a write command has been executed more recently than a format command, this byte contains the End of Track value. The LOCK bit is set in the Lock command. The eighth result byte also contains the bits programmed in the Perpendicular Mode command. The last two bytes of the Dumpreg Result Phase are set in the Configure command. After a hardware or software reset, the parameters in the result bytes are set to their appropriate default values.

Note: Some of these parameters are unaffected by a software reset, depending on the state of the LOCK bit. See the Lock Command for further information.

Command Phase:

0	0	0	0	1	1	1	0

Execution Phase: Internal registers read.

Result Phase:

PTR Drive 0							
PTR Drive 1							
PTR Drive 2							
PTR Drive 3							
Step Rate Time				Motor Off Time			
Motor On Time							DMA
Sector per Track/End of Track (Note)							
LOCK	0	DC3	DC2	DC1	DC0	GAP	WG
0	EIS	FIFO	POLL	THRESH			
PRETRK							

Note: Sectors per Track parameter returned if last command issued was Format. End of Track parameter returned if last command issued was Read or Write.

4.1.3 Format Track Command

This command formats one track on the disk in IBM, ISO, or Perpendicular format. After the index hole is detected, data patterns are written on the disk including all gaps, Address Marks, Address Fields, and Data Fields. The exact format is determined by the following parameters:

1. The MFM bit in the Opcode (first command) byte, which determines the format of the Address Marks and the encoding scheme.
2. The IAF bit in the Mode command, which selects between IBM and ISO format.
3. The WGATE and GAP bits in the Perpendicular Mode command, which select between the conventional and Toshiba Perpendicular format.
4. The Bytes per Sector code, which determines the sector size.
5. The Sector per Track parameter, which determines how many sectors are formatted on the track.
6. The Data Pattern byte, which is used as the filler byte in the Data Field of each sector.

Command Phase:

0	MFM	0	0	1	1	0	1
X	X	X	X	X	HD	DR1	DR0
Bytes per Sector							
Sectors per Track							
Format Gap							
Data Pattern							

Execution Phase: System transfers four ID bytes (track, head, sector, bytes/sector) per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the Data Field of each sector is filled with the data pattern byte.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Undefined
Undefined
Undefined
Undefined

To allow for flexible formatting, the μP must supply the four Address Field bytes (track, head, sector, bytes per sector code) for each sector formatted during the Execution Phase. This allows for non-sequential sector interleaving. This transfer of bytes from the μP to the controller can be done in the DMA or Non-DMA mode, with the FIFO enabled or disabled.

The Format Gap byte in the Command Phase is dependent on the data rate and type of disk drive, and controls the length of GAP3. Some typical values for the programmable GAP3 are given in Table 4-1. *Figure 4-2* shows the track format for each of the formats recognized by the format command. Table 4-2 shows some typical values for the Format GAP3 based on media type. The Format command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the Result Phase are significant.

TABLE 4-1. Typical Format GAP3 Length Values based on Drive Data Rate

Mode	Sector Size (Decimal)	Sector Code (Hex)	EOT (Hex)	Sector Gap (Hex) (Note 1)	Format GAP3 (Hex) (Note 2)
250 kbps MFM	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	512	02	09	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
500 kbps MFM	256	01	1A	0E	36
	512	02	0F	1B	54
	512	02	12	1B	6C
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF

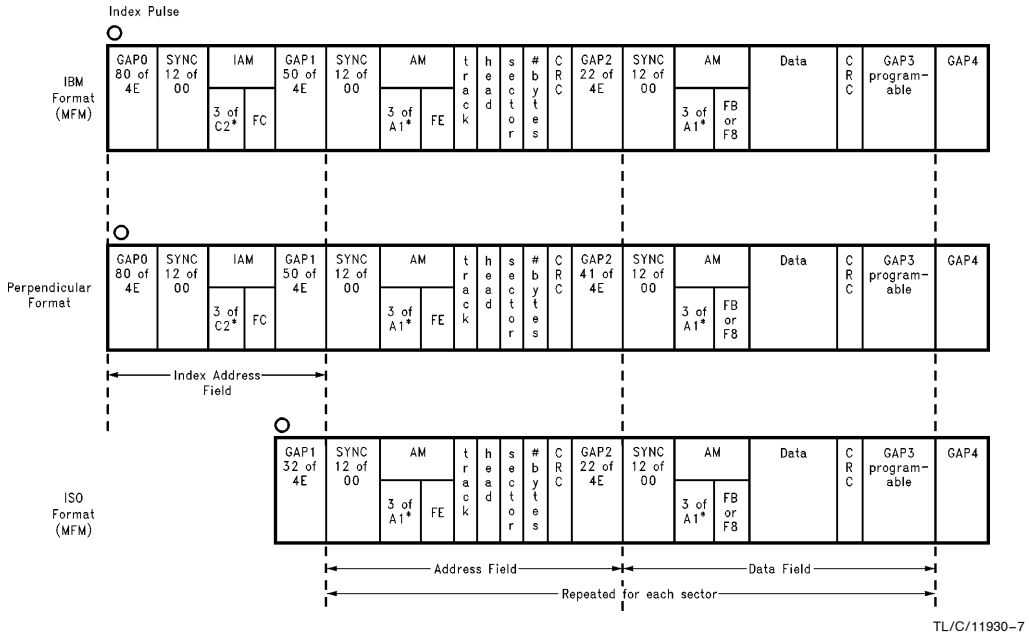
TABLE 4-2. Typical Format GAP3 Length Values Based on PC Compatible Diskette Media

Media Type	Sector Size Decimal	Sector Code Hex	EOT Hex	Sector Gap Hex	Format GAP3 Hex
360k	512	02	09	2A	50
1.2M	512	02	0F	1B	54
720k	512	02	09	1B	50
1.44M	512	02	12	1B	6C
2.88M (Note 3)	512	02	24	1B	53

Note 1: Sector Gap refers to the Intersector Gap Length parameter specified in the Command Phase of the Read, Write, Scan, and Verify commands. Although this is the recommended value, the FDC treats this byte as a don't care in the Read, Write, Scan, and Verify commands.

Note 2: Format Gap is the suggested value to use in the Format Gap parameter of the Format command. This is the programmable GAP3 as shown in *Figure 4-1*.

Note 3: The 2.88M diskette media is a Barium Ferrite media intended for use in Perpendicular Recording drives at data rates up to 1 Mbps.



Notes:

A1* = Data Pattern of A1, Clock Pattern of 0A

C2* = Data Pattern of C2, Clock Pattern of 14

All byte counts in decimal

All byte values in hex

CRC uses standard polynomial $x^{16} + x^{12} + x^5 + 1$

Perpendicular Format GAP2 = 41 bytes for 1 Mbps and 2 Mbps.

All other data rates use GAP2 = 22 bytes

FIGURE 4-2. IBM, Perpendicular, and ISO Formats Supported by the Format Command

4.1.4 Invalid Command

If an invalid command (illegal Opcode byte in the Command Phase) is received by the controller, the controller responds with ST0 in the Result Phase. The controller does not generate an interrupt during this condition. Bits 6 and 7 in the MSR are both set to a 1, indicating to the μP that the controller is in the Result Phase and the contents of ST0 must be read. The system reads an 80h value from ST0 indicating an invalid command was received.

Command Phase:

Invalid Op Codes

Execution Phase: None.

Result Phase:

Status Register 0 (80h)

4.1.5 Lock Command

The Lock command allows the user full control of the FIFO parameters after a software reset. If the LOCK bit is set to 1, then the FIFO, THRESH, and PRETRK bits in the Configure command are not affected by a software reset. In addition, the FWR, FRD, and BST bits in the Mode command are unaffected by a software reset. If the LOCK is 0 (default after a hardware reset), then the above bits are set to their default values after a software reset. This command is useful if the system designer wishes to keep the FIFO enabled and retain the other FIFO parameter values (such as THRESH) after a software reset.

After the command byte is written, the result byte must be read before continuing to the next command. The execution of the Lock command is not performed until the result byte is read by the μP. If the part is reset after the command byte is written but before the result byte is read, then the Lock command execution is not performed. This is done to prevent accidental execution of the Lock command.

Command Phase:

LOCK	0	0	1	0	1	0	0

Execution Phase: Internal Lock register is written.

Result Phase:

0	0	0	LOCK	0	0	0	0

4.1.6 Mode Command

This command is used to select the special features of the controller. The bits for the Command Phase bytes are shown in Section 4.1, Command Set Summary, and their function is described below. These bits are set to their default values after a hardware reset. The default value of each bit is denoted by a "bullet" to the left of each item. The value of each parameter after a software reset is explained.

Command Phase:

0	0	0	0	0	0	0	1
TMR	IAF	IPS	0	LOW PWR		1	ETR
FWR	FRD	BST	R255	0	0	0	0
DENSEL		BFR	WLD	Head Settle			
0	0	0	0	0	RG	0	PU

Execution Phase: Internal registers are written.

Result Phase: None.

TMR: Motor Timer mode. Default after a software reset.

- •**0** = Timers for motor on and motor off are defined for Mode 1. (See Specify command.)
- **1** = Timers for motor on and motor off are defined for Mode 2. (See Specify command.)

IAF: Index Address Format. Default after a software reset.

- •**0** = The controller formats tracks with the Index Address Field included. (IBM and Perpendicular format.)
- **1** = The controller formats tracks without including the Index Address Field. (ISO format.)

IPS: Implied Seek. Default after a software reset.

- •**0** = The implied seek bit in the command byte of a read, write, scan, or verify is ignored. Implied seeks could still be enabled by the EIS bit in the Configure command.
- **1** = The IPS bit in the command byte of a read, write, scan, or verify is enabled so that if it is set, the controller performs seek and sense interrupt operations before executing the command.

LOW PWR: Low Power mode. Default after a software reset.

- •**00** = Completely disable the low power mode.
- **01** = Automatic low power. For 500 kbps operation, go into low power mode 512 ms after the head unload timer times out. For 250 kbps operation the timeout period is doubled to 1s.
- **10** = Manual low power. Go into low power mode now.
- **11** = Not used.

ETR: Extended Track Range. Default after a software reset.

- •**0** = Track number is stored as a standard 8-bit value compatible with the IBM, ISO, and Perpendicular formats. This allows access of up to 256 tracks during a seek operation.
- **1** = Track number is stored as a 12-bit value. The upper four bits of the track value are stored in the upper four bits of the head number in the sector Address Field. This allows access of up to 4096 tracks during a seek operation. With this bit set, an extra byte is required in the Seek Command Phase and Sense Interrupt Result Phase.

FWR: FIFO Write Disable for μP write transfers to controller. Default after a software reset if LOCK is 0. If LOCK is 1, FWR retains its value after a software reset.

Note: This bit is only valid if the FIFO is enabled in the Configure command. If the FIFO is not enabled in the Configure command, then this bit is a don't care.

- •**0** = Enable FIFO. μP write transfers druing the Execution Phase use the internal FIFO.
- **1** = Disable FIFO. All write data transfers take place without the FIFO.

FRD: FIFO Read Disable for μP read transfers from controller. Default after a software reset if LOCK is 0. If LOCK is 1, FRD retains its value after a software reset.

Note: This bit is only valid if the FIFO is enabled in the Configure command. If the FIFO is not enabled in the Configure command, then this bit is a don't care.

•**0** = Enable FIFO. μP read transfers during the Execution Phase use the internal FIFO.

1 = Disable FIFO. All read data transfers take place without the FIFO.

BST: Burst Mode Disable. Default after a software reset if LOCK is 0. If LOCK is 1, BST retains its value after a software reset.

Note: This bit is only valid if the FIFO is enabled in the Configure command. If the FIFO is not enabled in the Configure command, then this bit is a don't care.

•**0** = Burst mode enabled for FIFO Execution Phase data transfers.

1 = Non-Burst mode enabled. The DRQ or IRQ6 pin is strobed once for each byte to be transferred while the FIFO is enabled.

R255: Recalibrate Step Pulses. The bit determines the maximum number of recalibrate step pulses the controller issues before terminating with an error. Default after a software reset.

•**0** = Maximum of 85 recalibrate step pulses. If ETR = 1, controller issues 3925 recalibrate step pulses maximum.

1 = Maximum of 255 recalibrate step pulses. If ETR = 1, controller issues 4095 maximum recalibrate step pulses.

DENSEL: Density Select Pin Configuration. This 2-bit value configures the Density Select output to one of three possible modes. The default mode configures the DENSEL pin according to the state of the IDENT input pin after a data rate has been selected. That is, if IDENT is high, the DENSEL pin is active high for the 500 kbps/1 Mbps/2 Mbps data rates. If IDENT is low, the DENSEL pin is active low for the 500 kbps/1 Mbps/2 Mbps data rates. See Table 4-3. In addition to these modes, the DENSEL output can be set to always low or always high, as shown in Table 4-4. This allows the user more flexibility with new drive types.

TABLE 4-3. DENSEL Default Encoding

Data Rate	DENSEL Pin Definition	
	IDENT = 1	IDENT = 0
250 kbps	Low	High
300 kbps	Low	High
500 kbps	High	Low
1 Mbps*	High	Low
2 Mbps**	High	Low

*When TUP bit 1 = 0, a Data Rate of 1 Mbps is selected.

**When TUP bit 1 = 1, a Data Rate of 2 Mbps is selected.

TABLE 4-4. DENSEL Encoding

Bit 1	Bit 0	DENSEL Pin Definition
0	0	Pin Low
0	1	Pin High
1	0	Undefined
1	1	DEFAULT

BFR: CMOS Disk Interface Buffer Enable.

•**0** = Drive output signals configured as standard 4 mA push-pull outputs (actually 40 mA sink, 4 mA source).

1 = Drive output signals configured as 40 mA open-drain outputs.

WLD: Scan Wild Card.

•**0** = An FFh from either the μP or the disk during a Scan command is interpreted as a wildcard character that always matches true.

1 = The Scan commands do not recognize FFh as a wildcard character.

Head Settle: Time allowed for read/write head to settle after a seek during an Implied Seek operation. This is controlled as shown in Table 4-5 by loading a 4-bit value for N. (The default value for N is 8.)

TABLE 4-5. Head Settle Time Calculation

Data Rate (kbits/sec)	Multiplier (4 Bit Value)	Head Settle Time (ms)
250	N × 8	0–120
300	N × 6.666	0–100
500	N × 4	0–60
1000	N × 2	0–30

RG: Read Gate Diagnostic.

•**0** = Enable DSKCHG disk interface input for normal operation.

1 = Enable DSKCHG to act as an external Read Gate input signal to the Data Separator. This is intended as a test mode to aid in evaluation of the Data Separator.

PU: PUMP Pulse Output Diagnostic.

•**0** = Enable MFM output pin for normal operation.

1 = Enable the MFM output to act as an internal serial data in signal.

4.1.7 NSC Command

The NSC command can be used to distinguish between the FDC versions and the 82077. The Result Phase byte uniquely identifies the floppy controller as a PC87334, which returns a value of 73h. The 82077 and DP8473 return a value of 80h, signifying an invalid command. The lower four bits of this result byte are subject to change by National, and reflects the particular version of the floppy disk controller part.

Command Phase:

0	0	0	1	1	0	0	0

Execution Phase: None.

Result Phase:

0	1	1	1	0	0	1	1

4.1.8 Perpendicular Mode Command

The Perpendicular Mode command is designed to support the unique Format and Write Data requirements of Perpendicular (Vertical) Recording disk drives (4 Mbyte unformatted capacity). The Perpendicular Mode command configures each of the four logical drives as a perpendicular or conventional disk drive. Configuration of the four logical disk drives is done via the D3–0 bits, or with the GAP and WG control bits. This command should be issued during the initialization of the floppy controller.

Command Phase:

0	0	0	1	0	0	1	0
OW	0	DC3	DC2	DC1	DC0	GAP	WG

Execution Phase: Internal registers are written.

Result Phase: None.

Perpendicular Recording drives operate in ''Extra High Density'' mode at 1 Mbps and 2 Mbps, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 kbps (High Density) and 250 kbps (Double Density) respectively. If perpendicular drives are present in the system, this command should be issued during initialization of the floppy controller, which configures each drive as perpendicular or conventional. Then, when a drive is accessed for a Format or Write Data command, the floppy controller adjusts the Format or Write Data parameters based on the data rate selected (see Table 4-6).

TABLE 4-6. Effect of Drive Mode and Data Rate on Format and Write Commands

Data Rate	Drive Mode	GAP2 Length Written during Format	Portion of GAP2 Re-Written by Write Data Command
250 kbps/300 kbps/500 kbps	Conventional Perpendicular	22 Bytes 22 Bytes	0 Bytes 19 Bytes
1 Mbps/2 Mbps	Conventional Perpendicular	22 Bytes 41 Bytes	0 Bytes 38 Bytes

TABLE 4-7. Effect of GAP and WG on Format and Write Commands

GAP	WG	Mode Description	GAP2 Length Written during Format	Portion of GAP2 Re-Written by Write Data Command
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps/2 Mbps)	41 Bytes	38 Bytes

Looking at the second command byte, DC3–0 corresponds to the four logical drives.

A 0 written to DCn sets drive n to conventional mode, and a 1 sets drive n to perpendicular mode. The OW (Overwrite) bit offers additional control. When OW = 1, the values of DC3–0 (drive configuration bits) are changeable. When OW = 0, the internal values of DC3–0 are unaffected, regardless of what is written to DC3–0.

The function of the DCn bits must also be qualified by setting both WG and GAP to 0. If WG and GAP are used (i.e., not set to 00), they override whatever is programmed in the DCn bits. Table 4-7 indicates the operation of the FDC based on the values of GAP and WG. Note that when GAP and WG are both 0, the DCn bits are used to configure each logical drive as conventional or perpendicular. DC3–0 is unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset. A hardware reset resets all the bits to zero (conventional mode for all drives). The Perpendicular Mode command bits may be rewritten at any time.

Note: When in the Perpendicular Mode for any drive at any data rate selected by the DC3–0 bits, write precompensation is set to zero.

Perpendicular Recording type disk drives have a Pre-Erase Head which leads the Read/Write Head by 200 μm, which translates to 38 bytes at the 1 Mbps data transfer rate (19 bytes at 500 kbps). The increased spacing between the two heads requires a larger GAP2 between the Address Field and Data Field of a sector at 1 Mbps/2 Mbps. (See Perpendicular Format in Table 4-1.) This GAP2 length of 41 bytes (at 1 Mbps/2 Mbps) ensures that the Preamble in the Data Field is completely ''pre-erased'' by the Pre-Erase Head. Also, during Write Data operations to a perpendicular drive, a portion of GAP2 must be rewritten by the controller to guarantee that the Data Field Preamble has been pre-erased (see Table 4-6).

4.1.9 Read Data Command

The Read Data command reads logical sectors containing a Normal Data Address Mark (AM) from the selected drive and makes the data available to the host μP. After the last Command Phase byte is written, the controller simulates the Motor On time for the selected drive internally. The user must turn on the drive motor directly by enabling the appropriate drive and motor select disk interface outputs with the Digital Output Register (DOR).

If Implied Seeks are enabled, the controller performs a Seek operation to the track number specified in the Command Phase. The controller also issues a Sense Interrupt for the seek and waits the Head Settle time specified in the Mode command.

The correct ID information (track, head, sector, bytes per sector) for the desired sector must be specified in the command bytes. See Table 4-8 Sector Size Selection for details on the bytes per sector code. In addition, the End of Track Sector Number (EOT) should be specified, allowing the controller to read multiple sectors. The Data Length byte is a don't care and should be set to FFh.

TABLE 4-8. Sector Size Selection

Bytes per Sector Code	Number of Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192
7	16384

The controller then starts the Data Separator and waits for the Data Separator to find the next sector Address Field. The controller compares the Address Field ID information (track, head, sector, bytes per sector) with the desired ID specified in the Command Phase. If the sector ID bytes do not match, then the controller waits for the Data Separator to find the next sector Address Field. The ID comparison process repeats until the Data Separator finds a sector Address Field ID that matches that in the command bytes, or until an error occurs. Possible errors are:

1. The μP aborted the command by writing to the FIFO. If there is no disk in the drive, the controller hangs up. The μP must then take the controller out of this hung state by writing a byte to the FIFO. This puts the controller into the Result Phase.
2. Two index pulses were detected since the search began, and no valid ID has been found. If the track address ID differs, the WT bit or BT bit (if the track address is FFh) is set in ST2. If the head, sector, or bytes per sector code did not match, the ND bit is set in ST1. If the Address Field AM was never found, the MA bit is set in ST1.
3. The Address Field was found with a CRC error. The CE bit is set in ST1.

Once the desired sector Address Field is found, the controller waits for the Data Separator to find the subsequent Data Field for that sector. If the Data Field (normal or deleted) is not found within the expected time, the controller terminates the operation and enters the Result Phase (MD is set in ST2). If a Deleted Data Mark is found and Skip Flag (SK) was set in the Opcode command byte, the controller skips this sector and searches for the next sector Address Field as described above. The effect of SK on the Read Data command is summarized in Table 4-9.

4.0 FDC Command Set Description (Continued)

Having found the Data Field, the controller then transfers data bytes from the disk drive to the host (described in Section 5.3 Controller Phases) until the bytes per sector count has been reached, or the host terminates the operation (through TC, end of track, or implicitly through overrun). The controller then generates the CRC for the sector and compares this value with the CRC at the end of the Data Field.

Having finished reading the sector, the controller continues reading the next logical sector unless one or more of the following termination conditions occurred:

1. The DMA controller asserted TC. The IC bits in ST0 are set to Normal Termination.
2. The last sector address (of side 1 if MT was set) was equal to EOT. The EOT bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. This is the expected condition during Non-DMA transfers.
3. Overrun error. The OR bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. If the μP cannot service a transfer request in time, the last correctly read byte is transferred.
4. CRC error. The CE bit in ST1 and the CD bit in ST2 are set. The IC bits in ST0 are set to Abnormal Termination.

If Multi-Track Selector (MT) was set in the Opcode command byte, and the last sector of side 0 has been transferred, the controller then continues with side 1.

Upon terminating the Execution Phase of the Read Data command, the controller asserts IRQ6, indicating the beginning of the Result Phase. The μP must then read the result bytes from the FIFO. The values that are read back in the result bytes are shown in Table 4-10. If an error occurs, the result bytes indicate the sector read when the error occurred.

Command Phase:

MT	MFM	SK	0	0	1	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

TABLE 4-9. SK Effect on the Read Data Command

SK	Data Type	Sector Read ?	CM Bit (ST2)	Description of Results
0	Normal	Y	0	Normal Termination
0	Deleted	Y	1	No Further Sectors Read
1	Normal	Y	0	Normal Termination
1	Deleted	N	1	Sector Skipped

TABLE 4-10. Result Phase Termination Values with No Error

MT	HD	Last Sector	ID Information at Result Phase			
			Track	Head	Sector	Bytes/Sector
0	0	< EOT	NC	NC	S + 1	NC
0	0	= EOT	T + 1	NC	1	NC
0	1	< EOT	NC	NC	S + 1	NC
0	1	= EOT	T + 1	NC	1	NC
1	0	< EOT	NC	NC	S + 1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S + 1	NC
1	1	= EOT	T + 1	0	1	NC

EOT = End of Track Sector Number from Command Phase
NC = No Change in Value
S = Sector Number last operated on by controller
T = Track Number programmed in Command Phase

TABLE 4-11. SK Effect on the Read Deleted Data Command

SK	Data Type	Sector Read ?	CM Bit (ST2)	Description of Results
0	Normal	Y	1	No Further Sectors Read
0	Deleted	Y	0	Normal Termination
1	Normal	N	1	Sector Skipped
1	Deleted	Y	0	Normal Termination

4.1.10 Read Deleted Data Command

The Read Deleted Data command reads logical sectors containing a Deleted Data AM from the selected drive and makes the data available to the host μP. This command is identical to the Read Data command, except for the setting of the CM bit in ST2 and the skipping of sectors. The effect of SK on the Read Deleted Data command is summarized in Table 4-11. See Table 4-10 for the state of the result bytes for a Normal Termination of the command.

Command Phase:

MT	MFM	SK	0	1	1	0	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

4.1.11 Read ID Command

The Read ID command finds the next available Address Field and returns the ID bytes (track, head, sector, bytes per sector) to the μP in the Result Phase. There is no data transfer during the Execution Phase of this command. An interrupt is generated when the Execution Phase is completed.

The controller first simulates the Motor On time for the selected drive internally. The user must turn on the drive motor directly by enabling the appropriate drive and motor select disk interface outputs with the Digital Output Register (DOR). The Read ID command does not perform an implied seek.

After waiting the Motor On time, the controller starts the Data Separator and waits for the Data Separator to find the next sector Address Field. If an error condition occurs, the IC bits in ST0 are set to Abnormal Termination, and the controller enters the Result Phase. Possible errors are:

1. The μP aborted the command by writing to the FIFO. If there is no disk in the drive, the controller hangs up. The μP must then take the controller out of this hung state by writing a byte to the FIFO. This puts the controller into the Result Phase.
2. Two index pulses were detected since the search began, and no AM has been found. If the Address Field AM was never found, the MA bit is set in ST1.

Command Phase:

0	MFM	0	0	1	0	1	0
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Controller reads first ID Field header bytes it can find and reports these bytes to the system in the result bytes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

4.1.12 Read A Track Command

The Read A Track command reads sectors in physical order from the selected drive and makes the data available to the host. This command is similar to the Read Data command with the following exceptions:

1. The controller waits for the index pulse before searching for a sector Address Field. If the μP writes to the FIFO before the index pulse, the command enters the Result Phase with the IC bits in ST0 set to Abnormal Termination.
2. A comparison of the sector Address Field ID bytes will be performed, except for the sector number. The internal sector address is set to 1, and then incremented for each successive sector read.

3. If the Address Field ID comparison fails, the controller sets ND in ST1, but continues to read the sector. If there is a CRC error in the Address Field, the controller sets CE in ST1, but continues to read the sector.
4. Multi-track and Skip operations are not allowed. SK and MT should be set to 0.
5. If there is a CRC error in the Data Field, the controller sets CE in ST1 and CD in ST2, but continues reading sectors.
6. The controller reads a maximum of EOT physical sectors. There is no support for multi-track reads.

Command Phase:

0	MFM	0	0	0	0	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or non-DMA modes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

4.1.13 Recalibrate Command

The Recalibrate command is very similar to the Seek command. The controller sets the Present Track Register (PTR) of the selected drive to zero. It then steps the head of the selected drive out until the TRK0 disk interface input signal goes active, or until the maximum number of step pulses have been issued. See Table 4-12 for the maximum recalibrate step pulse values based on the R255 and ETR bits in the Mode command. If the number of tracks on the disk drive exceeds the maximum number of recalibrate step pulses, another Recalibrate command may need to be issued.

TABLE 4-12. Maximum Recalibrate Step Pulses Based on R255 and ETR

R255	ETR	Maximum Recalibrate Step Pulses
0	0	85 (default)
1	0	255
0	1	3925
1	1	4095

After the last command byte is issued, the DRx BUSY bit is set in the MSR for the selected drive. The controller will simulate the Motor On time, and then enter the Idle Phase. The execution of the actual step pulses occur while the controller is in the Drive Polling Phase. An interrupt will be generated after the TRK0 signal is asserted, or after the maximum number of recalibrate step pulses are issued. There is no Result Phase. Recalibrates should not be issued on more than one drive at a time. This is because the drives are actually selected via the DOR, which can only select one drive at a time. No other command except the Sense Interrupt command should be issued while a Recalibrate command is in progress.

Command Phase:

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

Execution Phase: Disk drive head is stepped out to Track 0.

Result Phase: None.

4.1.14 Relative Seek Command

The Relative Seek command steps the selected drive in or out a given number of steps. This command will step the read/write head an incremental number of tracks, as opposed to comparing against the internal present track register for that drive.

Command Phase:

1	DIR	0	0	1	1	1	1
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Disk drive head stepped in or out a programmable number of tracks.

Result Phase: None.

The Relative Seek parameters are defined as follows:

DIR: Read/Write Head Step Direction Control

0 = Step Head Out

1 = Step Head In

RTN: Relative Track Number. This value will determine how many incremental tracks to step the head in or out from the current track number.

The controller will issue RTN number of step pulses and update the Present Track Register for the selected drive. The one exception to this is if the TRK0 disk input goes active, which indicates that the drive read/write head is at the outermost track. In this case, the step pulses for the Relative Seek are terminated, and the PTR value is set according to the actual number of step pulses issued. The arithmetic is done modulo 255. The DRx BUSY bit in the MSR is set for the selected drive. The controller will simulate the Motor On time before issuing the step pulses. After the Motor On time, the controller will enter the Idle Phase. The execution of the actual step pulses occurs in the Idle Phase of the controller.

After the step operation is complete, the controller will generate an interrupt. There is no Result Phase. Relative Seeks should not be issued on more than one drive at a time. This is because the drives are actually selected via the DOR, which can only select one drive at a time. No other command except the Sense Interrupt command should be issued while a Relative Seek command is in progress.

4.1.15 Scan Commands

The Scan commands allow data read from the disk to be compared against data sent from the μP, using ones complement arithmetic, sector by sector.

There are three Scan commands to choose from:

1. Scan Equal: checks to see if the scanned value of the disk data is equal to that of the μP data. The scan condition is therefore: disk data = μP data?
2. Scan Low or Equal: checks to see if the scanned value of the disk data is equal to or less than that of the μP data. The scan condition is therefore: disk data ≤ data?
3. Scan High or Equal: checks to see if the scanned value of the disk data is equal to or greater than that of the μP data. The scan condition is therefore: disk data ≥ μP data?

The results of these comparisons are indicated in the Status Register bits 3 and 2, see Table 4-13, and the structure of the three commands follows.

Each sector is compared starting with the most significant bytes first, and where the next sector is defined as the current Sector Number plus the Sector Step Size. Reading of sectors continues until either the scan condition is met, the End of Track (EOT) has been reached, or the Terminal Count (TC) is asserted.

If the Wildcard mode is enabled in the Mode command, an FFh from either the disk or the μP is used as a don't care byte that will always match equal. Read errors on the disk will have the same error conditions as the Read Data command.

Additionally, if the Skip Flag (SK) bit is set, sectors with deleted data marks will be ignored. If all sectors read are skipped, the command will terminate with bit 3 of the Status Register set (mimicking a Scan Equal Hit).

TABLE 4-13. Scan Command Termination Values

Command	Comparison Condition	Status		Condition Met?	Indicated Result
		D3	D2		
Scan Equal	Disk Data = μP Data?	1	0	Yes	Disk Data = μP Data
		0	1	No	Disk Data ≠ μP Data
Scan Low or Equal	Disk Data ≤ μP Data?	1	0	Yes	Disk Data = μP Data
		0	0	Yes	Disk Data < μP Data
		0	1	No	Disk Data > μP Data
Scan High or Equal	Disk Data ≥ μP Data?	1	0	Yes	Disk Data = μP Data
		0	0	Yes	Disk Data > μP Data
		0	1	No	Disk Data < μP Data

SCAN EQUAL

Command Phase:

MT	MFM	SK	1	0	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase:

MT	MFM	SK	1	1	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Status Register 0							
Status Register 1							
Status Register 2							
Track Number							
Head Number							
Sector Number							
Bytes per Sector							

SCAN HIGH OR EQUAL

Command Phase:

MT	MFM	SK	1	1	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN LOW OR EQUAL

Command Phase:

MT	MFM	SK	1	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

4.1.16 Seek Command

The Seek command steps the selected drive in or out until the desired track number is reached. During the Execution Phase of the Seek command, the track number to seek to is compared with the present track number. The controller will determine how many step pulses to issue, and the DIR disk interface output will indicate which direction the R/W head should move. The DRx BUSY bit is set in the MSR for the appropriate drive. The controller will wait the Motor On time before issuing the first step pulse.

After the Motor On time, the controller will enter the Idle Phase. The execution of the actual step pulses occurs in the Drive Polling phase of the controller. The step pulse rate is determined by the value programmed in the Specify command. An interrupt will be generated one step pulse period after the last step pulse is issued. A Sense Interrupt command should be issued to determine the cause of the interrupt. There is no Result Phase.

While the internal microengine is capable of performing seek commands on 2 or more drives at the same time, software should ensure that only one drive is seeking at a time. This is because the drives are actually selected via the DOR, which can only select one drive at a time. No other command except a Sense Interrupt command should be issued while a Seek command is in progress.

If the extended track range mode is enabled with the ETR bit in the Mode command, a fourth command byte should be written in the Command Phase to indicate the four most significant bits of the desired track number. Otherwise, only three command bytes should be written.

Command Phase:

0	0	0	0	1	1	1	1
X	X	X	X	X	HD	DR1	DR0
New Track Number							
MSN of Track Number				0	0	0	0

Note: The last Command Phase byte is required only if ETR is set in Mode Command.

Execution Phase: Disk drive head is stepped in or out to a programmed track.

Result Phase: None.

4.1.17 Sense Drive Status Command

The Sense Drive Status command returns the status of the selected disk drive in ST3. This command does not generate an interrupt.

Command Phase:

0	0	0	0	0	1	0	0
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Disk drive status information is detected and reported.

Result Phase:

Status Register 3

4.1.18 Sense Interrupt Command

The Sense Interrupt command is used to determine the cause of an interrupt when the interrupt is a result of the change in status of any disk drive.

Command Phase:

0	0	0	0	1	0	0	0

Execution Phase: Status of interrupt is reported.

Result Phase:

Status Register 0				
Present Track Number (PTR)				
MSN of PTR	0	0	0	0

Note: The third Result Phase byte can only be read if ETR is set in the Mode Command.

Four possible causes for the interrupt are:

1. Entry into the Result Phase of any of the following commands:
   a. Read Data
   b. Read Deleted Data
   c. Read a Track
   d. Read ID
   e. Write Data
   f. Write Deleted Data
   g. Format
   h. Scan
   i. Verify
2. Occurrence of a data transfer in the Execution Phase while in the Non-DMA mode.

3. The Ready Signal changed state during the polling mode for an internally selected drive. (Occurs only after a hardware or software reset.)
4. A Seek, Relative Seek, or Recalibrate command terminates.

An interrupt due to reasons 1 or 2 does not require the Sense Interrupt command and is cleared automatically. This type of interrupt occurs during normal command operations and is easily discernible by the μP via the MSR. It is cleared when reading or writing information from or to the Data Register (FIFO).

An interrupt caused by reasons 3 or 4 is identified with the aid of the Sense Interrupt command. This type of interrupt is cleared after the first result byte has been read. Use bits 5, 6, and 7 of ST0 to identify the cause of the interrupt as shown in Table 4-14.

Issuing a Sense Interrupt command without an interrupt pending is treated as an Invalid command. If the extended track range mode is enabled, a third byte should be read in the Result Phase, which will indicate the four most significant bits of the present track number. Otherwise, only two result bytes should be read.

TABLE 4-14. Status Register 0 Termination Codes

Status Register 0			Cause
Interrupt Code		Seek End	
D7	D6	D5	
1	1	0	Internal Ready Went True
0	0	1	Normal Seek Termination
0	1	1	Abnormal Seek Termination

4.1.19 Set Track Command

This command is used to inspect or change the value of the internal Present Track Register. This can be useful for recovery from disk mistracking errors, where the real current track can be read through the Read ID command, and then the Set Track command can be used to set the internal Present Track Register to the correct value.

If the WNR bit is a 0, a track register is to be read. In this case, the Result Phase byte contains the value in the internal register specified, and the third byte in the Command Phase is a dummy byte.

If the WNR bit is a 1, data is written to a track register. In this case the third byte of the Command Phase is written to the specified internal track register, and the Result Phase byte contains this new value.

The DS1 and DS0 bits select the Present Track Register for the particular drive. The internal register address depends on MSB, DS1, and DS0 as shown in Table 4-15. This command does not generate an interrupt.

TABLE 4-15. Set Track Register Address

DS1	DS0	MSB	Register Addressed
0	0	0	PTR0 (LSB)
0	0	1	PTR0 (MSB)
0	1	0	PTR1 (LSB)
0	1	1	PTR1 (MSB)
1	0	0	PTR2 (LSB)
1	0	1	PTR2 (MSB)
1	1	0	PTR3 (LSB)
1	1	1	PTR3 (MSB)

Command Phase:

0	WNR	1	0	0	0	0	1
0	0	1	1	0	MSB	DS1	DS0
Present Track Number (PTR)							

Execution Phase: Internal register selected by MSB of DS1 or DS0 is read or written.

Result Phase:

Value

4.1.20 Specify Command

The Specify command sets the initial values for three internal timers. The parameters of this command are undefined after power-up, and are unaffected by any reset. Thus, software should always issue a Specify command as part of an initialization routine. This command does not generate an interrupt.

Command Phase:

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

Execution Phase: Internal registers are written.

Result Phase: None.

Step Rate Time: These four bits define the time interval between successive step pulses during a seek, implied seek, recalibrate, or relative seek. The programming of this step rate is shown in Table 4-16.

TABLE 4-16. Step Rate Time (SRT) Values

Data Rate	Value	Range	Units
1 Mbps	(16 − SRT)/2	0.5–8	ms
500 kbps	(16 − SRT)	1–16	ms
300 kbps	(16 − SRT) × 1.67	1.67–26.7	ms
250 kbps	(16 − SRT) × 2	2–32	ms

Motor Off Time: These four bits determine the simulated Motor Off time as shown in Table 4-17.

Motor On Time: These seven bits determine the simulated Motor On time as shown in Table 4-18.

DMA: This bit selects the data transfer mode in the Execution Phase of a read, write, or scan operation.

0 = DMA mode is selected

1 = Non-DMA mode is selected

TABLE 4-17. Motor Off Time (MFT) Values

Data Rate	Mode 1 (TMR = 0)		Mode 2 (TMR = 1)		Units
	Value	Range	Value	Range	
1 Mbps	MFT × 8	8–128	MFT × 512	512–8192	ms
500 kbps	MFT × 16	16–256	MFT × 512	512–8192	ms
300 kbps	MFT × 80/3	26.7–427	MFT × 2560/3	853–13653	ms
250 kbps	MFT × 32	32–512	MFT × 1024	1024–16384	ms

Note: Motor Off Time = 0 is treated as MFT = 16.

TABLE 4-18. Motor On Time (MNT) Values

Data Rate	Mode 1 (TMR = 0)		Mode 2 (TMR = 1)		Units
	Value	Range	Value	Range	
1 Mbps	MNT	1–128	MNT × 32	32–4096	ms
500 kbps	MNT	1–128	MNT × 32	32–4096	ms
300 kbps	MNT × 10/3	3.3–427	MNT × 160/3	53–6827	ms
250 kbps	MNT × 4	4–512	MNT × 64	64–8192	ms

Note: Motor On Time = 0 is treated as MNT = 128.

The Motor Off and Motor On timers are artifacts of the NEC μPD765. These timers determine both the delay from selecting a drive motor until a read or write operation is started, and the delay of deselecting the drive motor after the command is completed. Since the FDC enables the drive and motor select line directly through the DOR, these timers only provide some delay from the initiation of a command until it is actually started.

4.1.21 Verify Command

The Verify command reads logical sectors containing a Normal Data AM from the selected drive without transferring the data to the host. This command is identical to the Read Data command, except that no data is transferred during the Execution Phase.

The Verify command is designed for post-format or post-write verification. Data is read from the disk, as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value on the disk. The EOT value should be set to the final sector to be checked on each side. If EOT is greater than the number of sectors per side, the command will terminate with an error and no useful Address Mark or CRC data will be given.

The TC pin cannot be used to terminate this command since no data is transferred. The verify command can simulate a TC by setting the EC bit to a 1. In this case, the command will terminate when SC (Sector Count) sectors have been read. (If SC = 0 then 256 sectors will be verified.) If EC = 0, then the command will terminate when EOT is equal to the last sector to be checked. In this case, the Data Length parameter should be set to FFh. Refer to Table 4-10 for the Result Phase values for a successful completion of the command. Also see Table 4-19 for further explanation of the result bytes with respect to the MT and EC bits.

Command Phase:

MT	MFM	SK	1	0	1	1	0
EC	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length/Sector Count							

Execution Phase: Data is read from disk but not transferred to the system.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

TABLE 4-19. Verify Command Result Phase

MT	EC	SC/EOT Value (Notes 1, 2)	Termination Result
0	0	DTL used (should be FFh) EOT ≤ # Sectors per Side	No Errors
0	0	DTL used (should be FFh) EOT > # Sectors per Side	Abnormal Termination
0	1	SC ≤ # Sectors per Side AND SC ≤ EOT	No Errors
0	1	SC > # Sectors Remaining OR SC > EOT	Abnormal Termination
1	0	DTL used (should be FFh) EOT ≤ # Sectors per Side	No Errors
1	0	DTL used (should be FFh) EOT > # Sectors per Side	Abnormal Termination
1	1	SC ≤ # Sectors per Side AND SC ≤ EOT	No Errors
1	1	SC ≤ (EOT × 2) AND EOT ≤ # Sectors per Side	No Errors
1	1	SC > (EOT × 2)	Abnormal Termination

Note 1: # Sectors per Side = number of formatted sectors per each side of the disk.

Note 2: # Sectors Remaining = number of formatted sectors remaining which can be read, which includes side 1 of the disk if the MT bit is set to 1.

Note 3: If MT = 1 and the SC value is greater than the number of remaining formatted sectors on side 0, verifying will continue on side 1 of the disk.

4.1.22 Version Command

The Version command can be used to determine the floppy controller being used. The Result Phase uniquely identifies the floppy controller version. The FDC returns a value of 90h in order to be compatible with the 82077. The DP8473 and other NEC765 compatible controllers will return a value of 80h (invalid command).

Command Phase:

0	0	0	1	0	0	0	0

Execution Phase: None.

Result Phase:

1	0	0	1	0	0	0	0

4.1.23 Write Data Command

The Write Data command receives data from the host and writes logical sectors containing a Normal Data AM to the selected drive. The operation of this command is similar to the Read Data command except that the data is transferred from the μP to the controller instead of the other way around.

The controller will simulate the Motor On time before starting the operation. If implied seeks are enabled, the seek and sense interrupt functions are then performed. The controller then starts the Data Separator and waits for the Data Separator to find the next sector Address Field. The controller compares the Address ID (track, head, sector, bytes per sector) with the desired ID specified in the Command Phase. If there is no match, the controller waits to find the next sector Address Field. This process continues until the desired sector is found. If an error condition occurs, the IC bits in ST0 are set to Abnormal Termination, and the controller enters the Result Phase. Possible errors are:

1. The μP aborted the command by writing to the FIFO. If there is no disk in the drive, the controller will hang up. The μP must then take the controller out of this hung state by writing a byte to the FIFO. This will put the controller into the Result Phase.
2. Two index pulses were detected since the search began, and no valid ID has been found. If the track address ID differs, the WT bit or BT bit (if the track address is FFh) will be set in ST2. If the head, sector, or bytes per sector code did not match, the ND bit is set in ST1. If the Address Field AM was never found, the MA bit is set in ST1.
3. The Address Field was found with a CRC error. The CE bit is set in ST1.
4. If the controller detects the Write Protect disk interface input is Asserted. Bit 1 of ST1 is set.

If the correct Address Field is found, the controller waits for all (conventional mode) or part (perpendicular mode) of GAP2 to pass. The controller will then write the preamble field, address marks, and data bytes to the Data Field. The data bytes are transferred to the controller by the μP.

Having finished writing the sector, the controller will continue reading the next logical sector unless one or more of the following termination conditions has occurred:

1. The DMA controller asserted TC. The IC bits in ST0 are set to Normal Termination.
2. The last sector address (of side 1 if MT was set) was equal to EOT. The EOT bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. This is the expected condition during Non-DMA transfers.
3. Underrun error. The OR bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. If the μP cannot service a transfer request in time, the last correctly written byte will be written to the disk.

If MT was set in the Opcode command byte, and the last sector of side 0 has been transferred, the controller will then continue with side 1.

Command Phase:

MT	MFM	0	0	0	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

4.1.24 Write Deleted Data

The Write Deleted Data command receives data from the host and writes logical sectors containing a Deleted Data AM to the selected drive. This command is identical to the Write Data command except that a Deleted Data AM is written to the Data Field instead of a Normal Data AM.

Command Phase:

MT	MFM	0	0	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

4.0 FDC Command Set Description (Continued)

4.2 COMMAND SET SUMMARY

CONFIGURE

Command Phase:

0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	FIFO	POLL	THRESH			
PRETRK							

Execution Phase: Internal registers written.

Result Phase: None.

DUMPREG

Command Phase:

0	0	0	0	1	1	1	0

Execution Phase: Internal registers read.

Result Phase:

PTR Drive 0							
PTR Drive 1							
PTR Drive 2							
PTR Drive 3							
Step Rate Time				Motor Off Time			
Motor On Time							DMA
Sector per Track/End of Track (Note)							
LOCK	0	DC3	DC2	DC1	DC0	GAP	WG
0	EIS	FIFO	POLL	THRESH			
PRETRK							

Note: Sectors per Track parameter returned if last command issued was Format. End of Track parameter returned if last command issued was Read or Write.

FORMAT TRACK

Command Phase:

0	MFM	0	0	1	1	0	1
X	X	X	X	X	HD	DR1	DR0
Bytes per Sector							
Sectors per Track							
Format Gap							
Data Pattern							

Execution Phase: System transfers four ID bytes (track, head, sector, bytes/sector) per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the Data Field of each sector is filled with the data pattern byte.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Undefined
Undefined
Undefined
Undefined

INVALID

Command Phase:

Invalid Op Codes

Execution Phase: None.

Result Phase:

Status Register 0 (80h)

LOCK

Command Phase:

LOCK	0	0	1	0	1	0	0

Execution Phase: Internal Lock register is written.

Result Phase:

0	0	0	LOCK	0	0	0	0

MODE

Command Phase:

0	0	0	0	0	0	0	1
TMR	IAF	IPS	0	LOW PWR		1	ETR
FWR	FRD	BST	R255	0	0	0	0
DENSEL		BFR	WLD	Head Settle			
0	0	0	0	0	RG	0	PU

Execution Phase: Internal registers are written.

Result Phase: None.

NSC

Command Phase:

0	0	0	1	1	0	0	0

Execution Phase: None.

Result Phase:

0	1	1	1	0	0	1	1

PERPENDICULAR MODE

Command Phase:

0	0	0	1	0	0	1	0
OW	0	DC3	DC2	DC1	DC0	GAP	WG

Execution Phase: Internal registers are written.

Result Phase: None.

4.0 FDC Command Set Description (Continued)

READ DATA

Command Phase:

MT	MFM	SK	0	0	1	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ DELETED DATA

Command Phase:

MT	MFM	SK	0	1	1	0	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ ID

Command Phase:

0	MFM	0	0	1	0	1	0
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Controller reads first ID Field header bytes it can find and reports these bytes to the system in the result bytes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ A TRACK

Command Phase:

0	MFM	0	0	0	0	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or non-DMA modes.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

RECALIBRATE

Command Phase:

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

Execution Phase: Disk drive head is stepped out to Track 0.

Result Phase: None.

4.0 FDC Command Set Description (Continued)

RELATIVE SEEK

Command Phase:

1	DIR	0	0	1	1	1	1
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Disk drive head stepped in or out a programmable number of tracks.

Result Phase: None.

SCAN EQUAL

Command Phase:

MT	MFM	SK	1	0	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase:

MT	MFM	SK	1	1	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Status Register 0							
Status Register 1							
Status Register 2							
Track Number							
Head Number							
Sector Number							
Bytes per Sector							

SCAN HIGH OR EQUAL

Command Phase:

MT	MFM	SK	1	1	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN LOW OR EQUAL

Command Phase:

MT	MFM	SK	1	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SEEK

Command Phase:

0	0	0	0	1	1	1	1
X	X	X	X	X	HD	DR1	DR0
New Track Number							
MSN of Track Number				0	0	0	0

Note: The last Command Phase byte is required only if ETR is set in Mode Command.

Execution Phase: Disk drive head is stepped in or out to a programmed track.

Result Phase: None.

4.0 FDC Command Set Description (Continued)

SENSE DRIVE STATUS

Command Phase:

0	0	0	0	0	1	0	0
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Disk drive status information is detected and reported.

Result Phase:

Status Register 3

SENSE INTERRUPT

Command Phase:

0	0	0	0	1	0	0	0

Execution Phase: Status of interrupt is reported.

Result Phase:

Status Register 0				
Present Track Number (PTR)				
MSN of PTR	0	0	0	0

Note: The third Result Phase byte can only be read if ETR is set in the Mode Command.

SET TRACK

Command Phase:

0	WNR	1	0	0	0	0	1
0	0	1	1	0	MSB	DS1	DS0
Present Track Number (PTR)							

Execution Phase: Internal register selected by MSB of DS1 or DS0 is read or written.

Result Phase:

Value

SPECIFY

Command Phase:

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

Execution Phase: Internal registers are written.

Result Phase: None.

VERIFY

Command Phase:

MT	MFM	SK	1	0	1	1	0
EC	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length/Sector Count							

Execution Phase: Data is read from disk but not transferred to the system.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

VERSION

Command Phase:

0	0	0	1	0	0	0	0

Execution Phase: None.

Result Phase:

1	0	0	1	0	0	0	0

4.0 FDC Command Set Description (Continued)

WRITE DATA

Command Phase:

MT	MFM	0	0	0	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

WRITE DELETED DATA

Command Phase:

MT	MFM	0	0	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase:

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

4.0 FDC Command Set Description (Continued)

4.3 MNEMONIC DEFINITIONS FOR FDC COMMANDS

Symbol	Description
BFR	Buffer enable bit used in the Mode command. Enabled open-collector output buffers.
BST	Burst Mode disable control bit used in Mode command. Selects the Non-Burst FIFO mode if the FIFO is enabled.
DC0–3	Drive Configuration 0–3. Used to set DC1a drive to conventional or perpendicular DC2 mode. Used in Perpendicular Mode DC3 command.
DENSEL	Density Select control bits used in the Mode command.
DIR	Direction control bit used in Relative Seek command to indicate step in or out.
DMA	DMA mode enable bit used in the Specify command.
DR0–1	Drive Select 0–1 bits used in most commands. Selects the logical drive.
DTL	Data Length parameter used in the Read, Write, Scan and Verify commands.
EC	Enable Count control bit used in the Verify command. When this bit is 1, the DTL parameter becomes SC (Sector Count).
EIS	Enable Implied Seeks. Used in the Configure command.
EOT	End of Track parameter set in the Read, Write, Scan, and Verify commands.
ETR	Extended Track Range used with the Seek command.
FIFO	First-In First-Out buffer. Also a control bit used in the Configure command to enable or disable the FIFO.
FRD	FIFO Read disable control bit used in the Mode command.
FWR	FIFO Write disable control bit used in the Mode command.
GAP	GAP2 control bit used in the Perpendicular Mode command.
HD	Head Select control bit used in most commands. Selects Head 0 or 1 of the disk.
IAF	Index Address Field control bit used in the Mode command. Enables the ISO Format during the Format command.
IPS	Implied Seek enable bit used in the Mode, Read, Write, and Scan commands.
LOCK	Lock enable bit in the Lock command. Used to make certain parameters be unaffected by a software reset.
LOW PWR	Low Power control bits used in the Mode command.
MFM	Modified Frequency Modulation control bit used in the Read, Write, Format, Scan and Verify commands. Selects MFM or FM data encoding.
MFT	Motor Off Time programmed in the Specify command.
MNT	Motor On Time programmed in the Specify command.
MT	Multi-Track enable bit used in the Read, Write, Scan and Verify commands.
OW	Overwrite control bit used in the Perpendicular Mode command.
POLL	Enable Drive Polling bit used in the Configure command.
PRETRK	Precompensation Track Number used in the Configure command.
PTR	Present Track Register. Contains the internal track number for one of the four logical disk drives.
PU	Pump diagnostic enable bit used in the Mode command.
R255	Recalibrate control bit used in Mode command. Sets maximum recalibrate step pulses to 255.
RG	Read Gate diagnostic enable bit used in the Mode command.
RTN	Relative Track Number used in the Relative Seek command.
SC	Sector Count control bit used in the Verify command.
SK	Skip control bit used in read and scan operations.
SRT	Step Rate Time programmed in the Specify command. Determines the time between step pulses for seek and recalibrates.
ST0–3	Status Register 0–3. Contains status ST1 information about the execution of an ST2 command. Read in the Result Phase of some ST3 commands.
THRESH	FIFO threshold parameter used in the Configure command.
TMR	Timer control bit used in the Mode command. Affects the timers set in the Specify command.
WG	Write Gate control bit used in the Perpendicular Mode command.
WLD	Wildcard bit in the Mode command used to enable or disable the wildcard byte (FF) during Scan commands.

5.0 FDC Functional Description

The PC87332 is software compatible with the DP8473 and 82077 floppy disk controllers. Upon a power-on reset, the 16 byte FIFO will be disabled. Also, the disk interface outputs will be configured as active push-pull outputs, which are compatible with both CMOS inputs and open-collector resistor terminated disk drive inputs. The FIFO can be enabled with the Configure command. The FIFO can be very useful at the higher data rates, with systems that have a large amount of DMA bus latency, or with multi-tasking systems such as the EISA or MicroChannel bus structures.

The FDC will support all the DP8473 Mode command features as well as some additional features. Additional features include control over the enabling of the FIFO for reads and writes, a Non-Burst mode for the FIFO, a bit that will configure the disk interface outputs as open-drain outputs, and programmability of the DENSEL output.

5.1 MICROPROCESSOR INTERFACE

The FDC interface to the microprocessor consists of the A9–3, AEN, $\overline{RD}$, and $\overline{WR}$ lines, which access the chip for reads and writes; the data lines D7–0; the address lines A2–0, which select the appropriate register (see Table 3-1); the IRQ6 signal, and the DMA interface signals DRQ, $\overline{DACK}$, and TC. It is through this microprocessor interface that the floppy controller receives commands, transfers data, and returns status information.

5.2 MODES OF OPERATION

The FDC has three modes of operation: PC-AT mode, PS/2 mode, and Model 30 mode, which are determined by the state of the IDENT pin and MFM pin. IDENT can be tied directly to V_{DD} or GND. The MFM pin must be tied high or low with a 10k resistor (there is an internal 40k–50k resistor on the MFM pin). The state of these pins is interrogated by the controller during a chip reset to determine the mode of operation. See Section 3.0 FDC Register Description, for more details on the register set used for each mode of operation. After chip reset, the state of IDENT can be changed to change the polarity of DENSEL (see Section 1.0 Pin Description).

PC-AT Mode—(IDENT tied high, MFM is a don't care): The PC-AT register set is enabled. The DMA enable bit in the Digital Output Register becomes valid (IRQ6 and DRQ can be TRI-STATE). TC and DENSEL become active high signals (defaults to a 5.25″ floppy drive).

PS/2 Mode—(IDENT tied low, MFM pulled high internally): This mode supports the PS/2 Models 50/60/80 configuration and register set. The DMA enable bit in the Digital Output Register becomes a don't care (IRQ6 and DRQ signals are always valid). TC and DENSEL become active low signals (default to 3.5″ floppy drive).

Model 30 Mode—(IDENT tied low, MFM pulled low externally): This mode supports the PS/2 Model 30 configuration and register set. The DMA enable bit in the Digital Output Register becomes valid (IRQ6 and DRQ can be TRI-STATE). TC is active high and DENSEL becomes active low (default to 3.5″ floppy drive).

5.3 CONTROLLER PHASES

The FDC has three separate phases of a command, the Command Phase, the Execution Phase, and the Result Phase. Each of these controller phases determine how data is transferred between the floppy controller and the host microprocessor. In addition, when no command is in progress, the controller is in the Idle Phase or Drive Polling Phase.

5.3.1 Command Phase

During the Command Phase, the μP writes a series of bytes to the Data Register. The first command byte contains the opcode for the command, and the controller knows how many more bytes to expect based on this opcode byte. The remaining command bytes contain the particular parameters required for the command. The number of command bytes varies for each particular command. All the command bytes must be written in the order specified in the Command Description Table. The Execution Phase starts immediately after the last byte in the Command Phase is written. Prior to performing the Command Phase, both the Digital Output Register and the data rate should be set with the Data Rate Select Register or Configuration Control Register.

The Main Status Register controls the flow of command bytes, and must be polled by the software before writing each Command Phase byte to the Data Register. Prior to writing a command byte, the RQM bit (D7) must be set and the DIO bit (D6) must be cleared in the MSR. After the first command byte is written to the Data Register, the CMD PROG bit (D4) is also set and remains set until the last Result Phase byte is read. If there is no Result Phase, the CMD PROG bit is cleared after the last command byte is written.

A new command may be initiated after reading all the result bytes from the previous command. If the next command requires selecting a different drive or changing the data rate, the DOR and DSR or CCR should be updated. If the command is the last command, the software should deselect the drive.

Note: As a general rule, the operation of the controller core is independent of how the μP updates the DOR, DSR, and CCR. The software must ensure that the manipulation of these registers is coordinated with the controller operation.

5.3.2 Execution Phase

During the Execution Phase, the disk controller performs the desired command. Commands that involve data transfers (e.g., read, write, or format operation) require the μP to write or read data to or from the Data Register at this time. Some commands such as a Seek or Recalibrate control the read/write head movement on the disk drive during the Execution Phase via the disk interface signals. Execution of other commands does not involve any action by the μP or disk drive, and consists of an internal operation by the controller.

If there is data to be transferred between the μP and the controller during the Execution Phase, there are three methods that can be used: DMA mode, interrupt transfer mode, and software polling mode. The last two modes are called the Non-DMA modes. The DMA mode is used if the system has a DMA controller. This allows the μP to do other tasks while the data transfer takes place during the Execution Phase. If the Non-DMA mode is used, an interrupt is issued for each byte transferred during the Execution Phase. Also,

instead of using the interrupt during Non-DMA mode, the Main Status Register can be polled by software to indicate when a byte transfer is required. All of these data transfer modes work with the FIFO enabled or disabled.

5.3.2.1 DMA Mode—FIFO Disabled

The DMA mode is selected by writing a 0 to the DMA bit in the Specify command and by setting the DMA enabled bit (D3) in the DOR. With the FIFO disabled, a DMA request (DRQ) is generated in the Execution Phase when each byte is ready to be transferred. The DMA controller should respond to the DRQ with a DMA acknowledge ($\overline{DACK}$) and a read or write strobe. The DRQ is cleared by the leading edge of the active low $\overline{DACK}$ input signal. After the last byte is transferred, an interrupt is generated, indicating the beginning of the Result Phase. During DMA operations the chip select input ($\overline{CS}$) must be held high. The $\overline{DACK}$ signal acts as the chip select for the FIFO in this case, and the state of the address lines A2–A0 is a don't care. The Terminal Count (TC) signal can be asserted by the DMA controller to terminate the data transfer at any time. Due to internal gating, TC is only recognized when $\overline{DACK}$ is low.

PC-AT Mode. When in the PC-AT interface mode with the FIFO disabled, the controller is in single byte transfer mode. That is, the system has one byte time to service a DMA request (DRQ) from the controller. DRQ is deasserted between each byte.

PS/2 and Model 30 Modes. When in the PS/2 or Model 30 modes, DMA transfers with the FIFO disabled are performed differently. Instead of a single byte transfer mode, the FIFO is actually enabled with THRESH = 0Fh. Thus, DRQ is asserted when one byte has entered the FIFO during reads, and when one byte can be written to the FIFO during writes. DRQ is deasserted by the leading edge of the $\overline{DACK}$ input, and is reasserted when $\overline{DACK}$ goes inactive high. This operation is very similar to Burst mode transfer with the FIFO enabled except that DRQ is deasserted between each byte.

5.3.2.2 DMA Mode—FIFO Enabled

Read Data Transfers

Whenever the number of bytes in the FIFO is greater than or equal to (16 − THRESH), a DRQ is generated. This is the trigger condition for the FIFO read data transfers from the floppy controller to the μP.

Burst Mode. DRQ remains active until enough bytes have been read from the controller to empty the FIFO.

Non-Burst Mode. DRQ is deasserted after each read transfer. If the FIFO is not completely empty, DRQ is reasserted after a 350 ns delay. This allows other higher priority DMA transfers to take place between floppy transfers. In addition, this mode allows the controller to work correctly in systems where the DMA controller is put into a read verify mode, where only $\overline{DACK}$ signals are sent to the FDC, with no $\overline{RD}$ pulses. This read verify mode of the DMA controller is used in some PC software. The FIFO Non-Burst mode allows the $\overline{DACK}$ input from the DMA controller to be strobed, which correctly clocks data from the FIFO.

For both the Burst and Non-Burst modes, when the last byte in the FIFO has been read, DRQ goes inactive. DRQ is then reasserted when the FIFO trigger condition is satisfied. After the last byte of a sector has been read from the disk, DRQ is again generated even if the FIFO has not yet reached its threshold trigger condition. This guarantees that all the current sector bytes are read from the FIFO before the next sector byte transfer begins.

Write Data Transfers

Whenever the number of bytes in the FIFO is less than or equal to THRESH, a DRQ is generated. This is the trigger condition for the FIFO write data transfers from the μP to the floppy controller.

Burst Mode. DRQ remains active until enough bytes have been written to the controller to completely fill the FIFO.

Non-Burst Mode. DRQ is deasserted after each write transfer. If the FIFO is not full DRQ is reasserted after a 350 ns delay. This deassertion of DRQ allows other higher priority DMA transfers to take place between floppy transfers.

The FIFO has a byte counter which monitors the number of bytes being transferred to the FIFO during write operations for both Burst and Non-Burst modes. When the last byte of a sector is transferred to the FIFO, DRQ is deasserted even if the FIFO has not been completely filled. Thus, the FIFO is cleared after each sector is written. Only after the floppy controller has determined that another sector is to be written is DRQ asserted again. Also, since DRQ is deasserted immediately after the last byte of a sector is written to the FIFO, the system does not need to tolerate any DRQ deassertion delay and is free to do other work.

Read and Write Data Transfers

The $\overline{DACK}$ input signal from the DMA controller may be held active during an entire burst or it may be strobed for each byte transferred during a read or write operation. When in the Burst mode, the floppy controller deasserts DRQ as soon as it recognizes that the last byte of a burst was transferred. If $\overline{DACK}$ is strobed for each byte, the leading edge of this strobe is used to deassert DRQ. If $\overline{DACK}$ is strobed, $\overline{RD}$ or $\overline{WR}$ is not required. This is the case during the Read-Verify mode of the DMA controller. If $\overline{DACK}$ is held active during the entire burst, the trailing edge of the $\overline{RD}$ or $\overline{WR}$ strobe is used to deassert DRQ. DRQ is deasserted within 50 ns of the leading edge of $\overline{DACK}$, $\overline{RD}$, or $\overline{WR}$. This quick response should prevent the DMA controller from transferring extra bytes in most applications.

Overrun Errors

An overrun or underrun error terminates the execution of the command if the system does not transfer data within the allotted data transfer time (see Section 3.7), which puts the controller into the Result Phase. During a read overrun, the μP is required to read the remaining bytes of the sector before the controller asserts IRQ6, signifying the end of execution. During a write operation, an underrun error terminates the Execution Phase after the controller has written the remaining bytes of the sector with the last correctly written byte to the FIFO and generated the CRC bytes. Whether there is an error or not, an interrupt is generated at the end of the Execution Phase, and is cleared by reading the first Result Phase byte.

$\overline{DACK}$ asserted alone without a RD or WR strobe is also counted as a transfer. If RD or WR are not being strobed for each byte, then $\overline{DACK}$ must be strobed for each byte so that the floppy controller can count the number of bytes correctly. A new command, the Verify command, has been added to allow easier verification of data written to the disk without the need of actually transferring the data on the data bus.

5.3.2.3 Interrupt Mode—FIFO Disabled

If the Interrupt (Non-DMA) mode is selected, IRQ6 is asserted instead of DRQ when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. The RQM and non-DMA bits (D7 and D5) in the MSR are set. The interrupt is cleared when the byte is transferred to or from the Data Register. $\overline{CS}$ and $\overline{RD}$ or $\overline{CS}$ and $\overline{WR}$ must be used to transfer the data in or out of the Data Register (A2–A0 must be valid). $\overline{CS}$ asserted by itself is not significant. $\overline{CS}$ must be asserted with $\overline{RD}$ or $\overline{WR}$ for a read or write transfer to be recognized.

The μP should transfer the byte within the data transfer service time (see Section 3.7). If the byte is not transferred within the time allotted, an Overrun Error is indicated in the Result Phase when the command terminates at the end of the current sector.

An interrupt is also generated after the last byte is transferred. This indicates the beginning of the Result Phase. The RQM and DIO bits (D7 and D6) in the MSR are set, and the non-DMA bit (D5) is cleared. This interrupt is cleared by reading the first Result Phase byte.

5.3.2.4 Interrupt Mode—FIFO Enabled

The Interrupt (Non-DMA) mode with the FIFO enabled is very similar to the Non-DMA mode with the FIFO disabled. In this case, IRQ6 is asserted instead of DRQ under the exact same FIFO threshold trigger conditions. The MSR should be read to verify that the interrupt is for a data transfer. The RQM and non-DMA bits (D7 and D5) in the MSR are set. $\overline{CS}$ and $\overline{RD}$ or $\overline{CS}$ and $\overline{WR}$ must be used to transfer the data in or out of the Data Register (A2–A0 must be valid). $\overline{CS}$ asserted by itself is not significant. $\overline{CS}$ must be asserted with $\overline{RD}$ or $\overline{WR}$ for a read or write transfer to be recognized.

The Burst mode may be used to hold the IRQ6 pin active during a burst, or the Non-Burst mode may be used to toggle the IRQ6 pin for each byte of a burst. The Main Status Register is always valid from the μP point of view. For example, during a read command, after the last byte of data has been read from the disk and placed in the FIFO, the MSR still indicates that the Execution Phase is active, and that data needs to be read from the Data Register. Only after the last byte of data has been read by the μP from the FIFO does the Result Phase begin.

The same overrun and underrun error procedures from the DMA mode apply to the Non-DMA mode. Also, whether there is an error or not, an interrupt is generated at the end of the Execution Phase, and is cleared by reading the first Result Phase byte.

5.3.2.5 Software Polling

If the Non-DMA mode is selected and interrupts are not suitable, the μP can poll the MSR during the Execution Phase to determine when a byte is ready to be transferred. The RQM bit (D7) in the MSR reflects the state of the IRQ6 signal. Otherwise, the data transfer is similar to the Interrupt Mode described above. This is true for the FIFO enabled or disabled.

5.3.3 Result Phase

During the Result Phase, the μP reads a series of bytes from the data register. These bytes indicate the status of the command. This status may indicate whether the command executed properly, or it may contain some control information (see the Command Description Section 4.1 and Status Register Description Section 3.0). These Result Phase bytes are read in the order specified for that particular command. Some commands do not have a result phase. Also, the number of result bytes varies with each command. All of the result bytes must be read from the Data Register before the next command can be issued.

Like the Command Phase, the Main Status Register controls the flow of result bytes, and must be polled by the software before reading each Result Phase byte from the Data Register. The RQM bit (D7) and DIO bit (D6) must both be set before each result byte can be read. After the last result byte is read, the COM PROG bit (D4) in the MSR is cleared, and the controller is ready for the next command.

5.3.4 Idle Phase

After a hardware or software reset, or after the chip has recovered from the power-down mode, the controller enters the Idle Phase. Also, when there are no commands in progress the controller is in the Idle Phase. The controller waits for a command byte to be written to the Data Register. The RQM bit is set and the DIO bit is cleared in the MSR. After receiving the first command (opcode) byte, the controller enters the Command Phase. When the command is completed the controller again enters the Idle Phase. The Data Separator remains synchronized to the reference frequency while the controller is idle. While in the Idle Phase, the controller periodically enters the Drive Polling Phase (see Section 5.3.5).

5.3.5 Drive Polling Phase

The National FDC supports the polling mode of the old generation 8-inch drives as a means of monitoring any change in status for each disk drive present in the system. This mode is supported for the sole purpose of providing backward compatibility with software that expects its presence.

While in the Idle Phase the controller enters a Drive Polling Phase every 1 ms (based on a 500 kbps data rate). While in the Drive Polling Phase, the controller interrogates the Ready Changed status for each of the four logical drives. The internal Ready line for each drive is toggled only after a hardware or software reset, and an interrupt is generated for drive 0. At this point, the software must issue four Sense Interrupt commands to clear the Ready Changed State status for each drive. This requirement can be eliminated if drive polling is disabled via the POLL bit in the Configure command. The Configure command must be issued within 500 μs (worst case) of the hardware or software reset for drive polling to be disabled.

Even if drive polling is disabled, drive stepping and delayed power-down occur in the Drive Polling Phase. The controller checks the status of each drive and if necessary it issues a step pulse on the STEP output with the DIR signal at the appropriate logic level. Also, the controller uses the Drive Polling Phase to control the Automatic Low Power mode. When the Motor Off time has expired, the controller waits 512 ms, based on a 500 kbps or 1 Mbps data rate, before powering down if this function is enabled via the Mode command.

If a new command is issued when the FDC is in the middle of a polling routine, the MSR will not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This can cause a delay between the first and second bytes of up to 500 μs at 250 kbps.

5.4 DATA SEPARATOR

The internal data separator is a Fully Digital PLL (FDPLL). The FDPLL synchronizes the raw data signal read from the disk drive. The synchronized signal is used to separate the encoded clock and data pulses. The data pulses are deserialized into bytes, and then sent to the μP by the controller.

The FDC supports five data rates: 250 kbps, 300 kbps, 500 kbps, 1 Mbps and 2 Mbps.

The FDC has a dynamic window margin and lock range performance capable of handling a wide range of floppy disk drives. In addition, the data separator operates well under a variety of conditions, including the high motor speed fluctuations of floppy-compatible tape drives.

Figure 5-1 shows the floppy disk controller dynamic window margin performance at the four different data rates. Dynamic window margin is the primary indicator of the quality and performance level of the data separator. This measurement indicates how much motor speed variation (MSV) of the drive spindle motor and bit jitter (or window margin) can be tolerated by the data separator.

MSV is shown on the x-axis of the dynamic window margin graph. MSV is translated directly to the actual data rate of the data as it is read from the disk by the data separator. That is, a faster than nominal motor results in a higher frequency in the actual data rate.

The dynamic window margin performance curves also indicate how much bit jitter (or window margin) can be tolerated by the data separator. This parameter is shown on the y-axis of the graphs. Bit jitter is caused by the magnetic interaction of adjacent data pulses on the disk, which effectively shifts the bits away from their nominal positions in the middle of the bit window. Window margin is commonly measured as a percentage. This percentage indicates how far a data bit can be shifted early or late with respect to its nominal bit position, and still be read correctly by the data separator. If the data separator cannot correctly decode a shifted bit, then the data is misread and a CRC error results.

The dynamic window margin performance curves contain two pieces of information:

1. the maximum range of MSV (also called ''lock range'') that the data separator can handle with no read errors, and
2. the maximum percentage of window margin (or bit jitter) that the data separator can handle with no read errors.

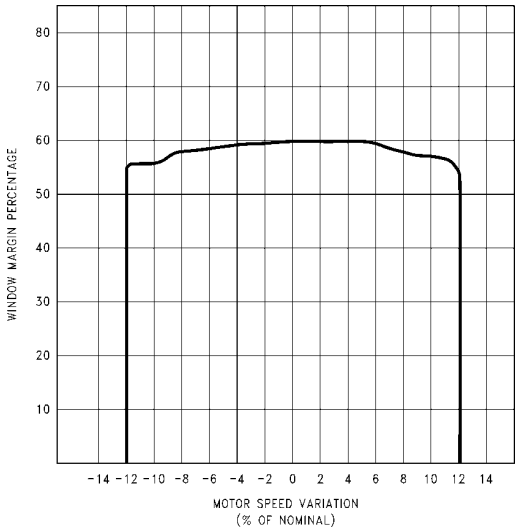
Thus, the area under the dynamic window margin curves in *Figure 5-1* is the range of MSV and bit jitter that the FDC can handle with no read errors. The FDC internal digital data separator has a much better performance than comparable digital data separator designs, and does not require any external components.

Note: The dynamic window margin curves were generated using a FlexStar FS-540 Floppy Disk Simulator and a proprietary dynamic window margin test program written by National Semiconductor.

The controller takes best advantage of the internal digital data separator by implementing a sophisticated read algorithm.

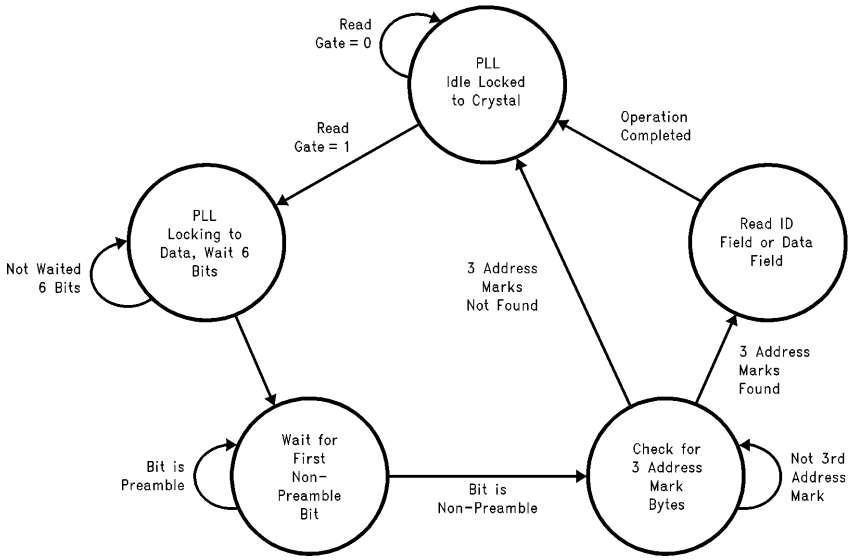
This ID search algorithm, shown in *Figure 5-2*, enhances the FDPLL's lock characteristics by forcing the FDPLL to relock to the crystal reference frequency any time the data separator attempts to lock to a non-preamble pattern. This algorithm ensures that the FDPLL is not thrown way out of lock by write splices or bad data fields.

250/300/500 kbps and 1 Mbps



TL/C/11930–8

FIGURE 5-1. PC87332 Dynamic Window Margin Performance
(Typical Performance at V_{DD} = 5.0V, 25°C)



TL/C/11930–9

FIGURE 5-2. Read Data Algorithm—State Diagram

5.5 CRYSTAL OSCILLATOR

The FDC is clocked by a single 24 MHz signal. An on-chip oscillator is provided to enable the attachment of a crystal or a clock signal.

A parallel resonant crystal is preferred if at all possible. In some cases, a series resonant crystal can be used, but care must be taken to ensure that the crystal does not oscillate at a sub-harmonic frequency. The oscillator is able to work with high profile, low profile, and surface mount type crystal enclosures. External bypass capacitors (5 pF to 10 pF) should be connected from XTAL1 and XTAL2 to GND. If an external oscillator circuit is used, it must have a duty cycle of at least 40%–60%, and minimum input levels of 2.4V and 0.4V. The controller should be configured so that the external oscillator clock is input into the X1/OSC pin, and XTAL2 is left unconnected.

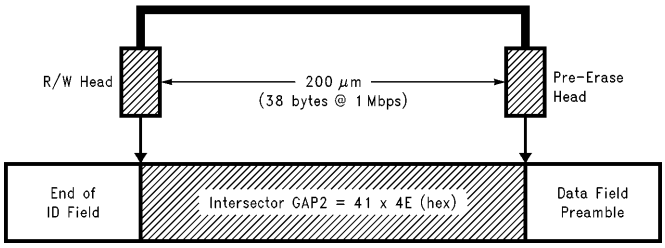
5.6 PERPENDICULAR RECORDING MODE

The FDC is fully compatible with perpendicular recording mode disk drives at all data rates. These perpendicular mode drives are also called 4 Mbyte (unformatted) or 2.88 Mbyte (formatted) drives, which refers to their maximum storage capacity. Perpendicular recording will orient the magnetic flux changes (which represent bits) vertically on the disk surface, allowing for a higher recording density than the conventional longitudinal recording methods. With this increase in recording density comes an increase in the data rate of up to 1 Mbps, thus doubling the storage capacity. In addition, the perpendicular 2.88M drive is read/write compatible with 1.44M and 720k diskettes (500 kbps and 250 kbps respectively).

The 2.88M drive has unique format and write data timing requirements due to its read/write head and pre-erase head design (see *Figure 5-3*). Unlike conventional disk drives which have only a read/write head, the 2.88M drive has both a pre-erase head and read/write head. With conventional disk drives, the read/write head by itself is able to rewrite the disk without problems. For 2.88M drives, a pre-erase head is needed to erase the magnetic flux on the disk surface before the read/write can write to the disk surface. The pre-erase head is activated during disk write operations only, i.e., Format and Write Data commands.

In 2.88M drives, the pre-erase head leads the read/write head by 200 μm, which translates to 38 bytes at 1 Mbps (19 bytes at 500 kbps). For both conventional and perpendicular drives, WGATE is asserted with respect to the position of the read/write head. With conventional drives, this means that WGATE is asserted when the read/write head is located at the beginning of the Data Field preamble. With the 2.88M drives, since the preamble must be pre-erased before it is rewritten, WGATE should be asserted when the pre-erase head is located at the beginning of the Data Field preamble. This means that WGATE should be asserted when the read/write head is at least 38 bytes (at 1 Mbps) before the preamble. See Table 4-6 for a description of the WGATE timing for perpendicular drives at the various data rates.

Because of the 38 byte spacing between the read/write head and the pre-erase head at 1 Mbps, the GAP2 length of 22 bytes used in the standard IBM disk format is not long enough. There is a new format standard for 2.88M drives at 1 Mbps called the Perpendicular Format, which increases the GAP2 length to 41 bytes (see *Figure 4-7*). The Perpendicular Mode command will put the floppy controller into perpendicular recording mode, which allows it to read and write perpendicular media. Once this command is invoked, the read, write and format commands can be executed in the normal manner. The perpendicular mode of the floppy controller will work at all data rates, adjusting the format and write data parameters accordingly. See Section 4.1.8 for more details.



TL/C/11930–10

FIGURE 5-3. Perpendicular Recording Drive R/W Head and Pre-Erase Head

5.7 DATA RATE SELECTION

The data rate can be chosen two different ways with the FDC. For PC compatible software, the Configuration Control Register at address 3F7h is used to program the data rate for the floppy controller. The lower bits D1 and D0 are used in the CCR to set the data rate. The other bits should be set to zero. See Table 3-7 for the data rate select encoding.

The data rate can also be set using the Data Rate Select Register at address 4. Again, the lower two bits of the register are used to set the data rate. The encoding of these bits is exactly the same as those in the CCR. The remainder of the bits in the DSR are used for other functions. Consult the Register Description (Section 3.1.6) for more details.

The data rate is determined by the last value that is written to either the CCR or the DSR. In other words, either the CCR or the DSR can override the data rate selection of the other register. When the data rate is selected, the microengine and data separator clocks are scaled appropriately. Also, the DRATE0 and DRATE1 output pins will reflect the state of the data select bits that were last written to either the CCR or the DSR.

5.8 WRITE PRECOMPENSATION

Write precompensation is a way of preconditioning the WDATA output signal to adjust for the effects of bit shift on the data as it is written to the disk surface. Bit shift is caused by the magnetic interaction of data bits as they are written to the disk surface, and has the effect of shifting these data bits away from their nominal position in the serial MFM data pattern. Data that is subject to bit shift is much harder to read by a data separator, and can cause soft read errors. Write precompensation predicts where bit shift could occur within a data pattern. It then shifts the individual data bits early, late, or not at all such that when they are written to the disk, the resultant shifted data bits will be back in their nominal position.

The FDC supports software programmable write precompensation. Upon power-up, the default write precomp values will be used (see Table 3-6). The programmer can choose a different value of write precomp with the DSR register if desired (see Table 3-7). Also on power-up, the default starting track number for write precomp is track zero. This starting track number for write precomp can be changed with the Configure command.

5.9 FDC LOW POWER MODE LOGIC

The FDC section of the PC87332 supports two low power modes described here in detail. Other low power modes of the PC87332 are described in Section 2.6. Details concerning entering and exiting low power mode via setting Data Rate Select Register bit 6 or by executing the FDC Mode Command are covered in this section, in Section 3.1.6 and Section 4.1.6. The microcode is driven from the clock, so it will be disabled while the clock is off. The FDC clock is always disabled upon entering this mode, however, the oscillator is only disabled when PTR1 = 1. Upon entering the power-down state, the RQM (Request For Master) bit in the MSR will be cleared.

There are two modes of low power in the floppy controller: manual low power and automatic low power. Manual low power is enabled by writing a 1 to bit 6 of the DSR. The chip will go into low power immediately. This bit will be cleared to 0 after the chip is brought out of low power. Manual low power can also be accessed via the Mode command. The function of the manual low power mode is a logical OR function between the DSR low power bit and the Mode command manual low power bit setting.

Automatic low power mode will switch the controller into low power 500 ms (at the 500 kbps MFM data rate) after it has entered the idle state. Once the auto low power mode is set, it does not have to be set again, and the controller will automatically go into low power mode after it has entered the idle state. Automatic low power mode can only be set with the Mode command.

There are two ways the FDC section of the SuperI/O can recover from the power-down state. 1) The part will power-up after a software reset via the DOR or DSR. Since a software reset requires reinitialization of the controller, this method can be undesirable. 2) The part will also power-up after a read or write to either the Data Register or Main Status Register. This is the preferred method of power-up since all internal register values are retained. It may take a few milliseconds for the oscillator to stabilize, and the μP will be prevented from issuing commands during this time through the normal Main Status Register protocol. That is, the RQM bit in the MSR will be a 0 until the oscillator has stabilized. When the controller has completely stabilized from power-up, the RQM bit in the MSR is set to 1 and the controller can continue where it left off.

The Data Rate Select, Digital Output, and Configuration Control Registers are unaffected by the power-down mode. They will remain active. It is up to the user to ensure that the Motor and Drive Select signals are turned off.

Note: If the power to an external oscillator driving the PC87334 is to be independently removed during the FDC low power mode, it must not be done until 2 ms after the FDC low power command is issued.

5.10 RESET OPERATION

The floppy controller can be reset by hardware or software. Hardware reset is enacted by pulsing the Master Reset input pin. A hardware reset will set all of the user addressable registers and internal registers to their default values. The

5.0 FDC Functional Description (Continued)

Specify command values will be don't cares, so they must be reinitialized. The major default conditions are: FIFO disabled, FIFO threshold = 0, Implied Seeks disabled, and Drive Polling enabled.

A software reset can be performed through the Digital Output Register or Data Rate Select Register. The DSR reset bit is self-clearing, while the DOR reset bit is not self-clearing. If the LOCK bit in the Lock command was set to a 1 previous to the software reset, the FIFO, THRESH, and PRETRK parameters in the Configure command will be retained. In addition, the FWR, FRD, and BST parameters in the Mode command will be retained if LOCK is set to 1. This function eliminates the need for total reinitialization of the controller after a software reset.

After a hardware (assuming the FDC is enabled in the FER) or software reset, the Main Status Register is immediately available for read access by the μP. It will return a 00h value until all the internal registers have been updated and the data separator is stabilized. When the controller is ready to receive a command byte, the MSR will return a value of 80h (Request for Master bit is set). The MSR is guaranteed to return the 80h value within 2.5 μs after a hardware or software reset. All other user addressable registers other than the Main Status Register and Data Register (FIFO) can be accessed at any time, even while the part is in reset.

6.0 Serial Ports

Each of these serial ports functions as a serial data input/output interface in a microcomputer system. The system software determines the functional configuration of the UARTs via an 8-bit bidirectional data bus.

The UARTs are completely independent. They perform serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of either UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

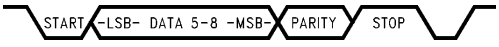
The UARTs have programmable baud rate generators that are capable of dividing the internal reference clock by divisors of 1 to ($2^{16}-1$), and producing a 16x clock for driving the transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs have complete MODEM-control capability and a prioritized interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

6.1 SERIAL PORT REGISTERS

Two identical register sets, one for each channel, are in the PC87332. All register descriptions in this section apply to the register sets in both channels. See Table 6-1.

6.2 LINE CONTROL REGISTER (LCR) Read/Write

The system programmer uses the Line Control Register (LCR) to specify the format of the asynchronous data communications exchange and set the Divisor Latch Access bit. This is a read and write register. Table 6-2 shows the contents of the LCR. Details on each bit follow.



TL/C/11930–11

FIGURE 6-1. PC87332 Composite Serial Data

TABLE 6-1. PC87332 UART Register Addresses (AEN = 0)

DLAB	A2	A1	A0	Selected Register
0	0	0	0	Receiver Buffer (Read), Transmitter Holding (Write)
0	0	0	1	Interrupt Enable
0	0	1	0	Interrupt Identification (Read) FIFO Control (Write)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (Least Significant Byte)
1	0	0	1	Divisor Latch (Most Significant Byte)

Bits 0,1 These two bits specify the number of data bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Data Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2 This bit specifies the number of Stop bits transmitted with each serial character. If it is 0, one Stop bit is generated in the transmitted data. If it is 1 when a 5-bit data length is selected, one and a half Stop bits are generated. If it is 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.

Bit 3 This bit is the Parity Enable bit. When it is 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data bit and the following Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data bits and the Parity bit are summed.)

Bit 4 This bit is the Even Parity Select bit. When parity is enabled and bit 4 is 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When parity is enabled and bit 4 is a 1, an even number of logic 1s is transmitted or checked.

Bit 5 This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0, Stick Parity is disabled.

6.0 Serial Ports (Continued)

Bit 6 This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to 1, the serial output (SOUT) is forced to the Spacing state (0). The break is disabled by setting bit 6 to 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note that this feature enables the CPU to alert a terminal. If the following sequence is used, no erroneous characters will be transmitted because of the break.

1. Wait for the transmitter to be idle (TEMT = 1).
2. Set break for the appropriate amount of time. If the transmitter will be used to time the break duration then check that TEMT = 1 before clearing the Break Control bit.
3. Clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration by sending characters and monitoring THRE and TEMT.

Bit 7 This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud rate Generator during a Read or Write operation or to have the Baud Out (BOUT) signal appear on the BOUT pin. It must be set low (logic 0) to access any other register.

TABLE 6-2. PC87332 Register Summary for an Individual UART Channel

Bit No.	Register Address											
	A0–2 = 0 DLAB = 0	A0–2 = 0 DLAB = 0	A0–2 = 1 DLAB = 0	2	2	3	4	5	6	7	A0–2 = 0 DLAB = 1	A0–2 = 1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Interrupt Empty	Interrupt ID Bit	RCVR FIFO Reset	Word Length Select Bit 1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit	XMIT FIFO Reset	Number of Stop Bits	Out 1 Bit (Note 3)	Parity Error (PE)	Trailing Edge Ring Indicator	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt	Interrupt ID Bit (Note 2)	Reserved	Parity Enable	IRQ Enable	Framing Error (FE)	Delta Data Carrier Detect	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the NS16450 Mode.

Note 3: This bit no longer has a pin associated with it.

6.0 Serial Ports (Continued)

TABLE 6-3. PC87332 UART Reset Configuration

Register or Signal	Reset Control	Reset State
Interrupt Enable	Master Reset (MR)	**0000** 0000 (Note 1)
Interrupt Identification	Master Reset	00**00** 0001
FIFO Control	Master Reset	00**00** 0000
Line Control	Master Reset	0000 0000
MODEM Control	Master Reset	**000**0 0000
Line Status	Master Reset	0110 0000
MODEM Status	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errors)	Read LSR/MR	Low/TRI-STATE
INTR (RCVR Data Ready)	Read RBR/MR	Low/TRI-STATE
INTR (THRE)	Read IIR/Write THR/MR	Low/Low/TRI-STATE
INTR (Modem Status Changes)	Read MSR/MR	Low/TRI-STATE
Interrupt Enable Bit	Master Reset	Low
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
RCVR FIFO	MR or (FCR1 = 1 and FCR0 = 1) or Change in FCR0	All Bits Low
XMIT FIFO	MR or (FCR2 = 1 and FCR0 = 1) or Change in FCR0	All Bits Low

Note 1: Boldface bits are permanently low.

Note 2: Bits 7–4 are driven by the input signals.

6.3 PROGRAMMABLE BAUD RATE GENERATOR

The PC87332 contains two independently programmable Baud rate Generators. The 24 MHz crystal oscillator frequency input is divided by 13, resulting in a frequency of 1.8462 MHz. This is sent to each Baud rate Generator and divided by the divisor of the associated UART. The output frequency of the Baud rate Generator (BOUT1,2) is 16 × the baud rate.

divisor # = (frequency input) (baud rate × 16)

The output of each Baud rate Generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded. Table 6-4 provides decimal divisors to use with crystal frequencies of 24 MHz. The oscillator input to the chip should always be 24 MHz to ensure that the Floppy Disk Controller timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

TABLE 6-4. PC87332 UART Divisors, Baud Rates and Clock Frequencies

24 MHz Input Divided to 1.8462 MHz		
Baud Rate	**Decimal Divisor for 16 x Clock**	**Percent Error (Note)**
50	2304	0.1
75	1536	
110	1047	
134.5	857	0.4
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.5
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
57600	2	
115200	1	

Note: The percent error for all baud rates, except where indicated otherwise, is 0.2%.

6.4 LINE STATUS REGISTER (LSR)

This 8-bit register provides status information to the CPU concerning data transfers. Table 6-2 shows the contents of the Line Status Register. Details on each bit follow:

Bit 0 This bit is the receiver Data Ready (DR) indicator. It is set to 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. It is reset to 0 by reading the data in the Receiver Buffer Register or the FIFO.

Bit 1 This bit is the Overrun Error (OE) indicator. It indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to 1 upon detection of an overrun condition, and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an Overrun error will occur only after the FIFO is completely full and the next character has been received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2 This bit is the Parity Error (PE) indicator. It indicates that the received data character does not have the correct parity, as selected by the even parity select bit. The PE bit is set to 1 upon detection of a parity error and is reset to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character that it applies to in the FIFO. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3 This bit is the Framing Error (FE) indicator. It indicates that the received character did not have a valid Stop bit. It is set to 1 whenever the Stop bit following the last data bit or parity bit is a 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character that it applies to in the FIFO. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error by assuming that the error was due to the next start bit. It samples this ''start'' bit twice and then takes in the bits following it as the rest of the frame.

Bit 4 This bit is the Break Interrupt (BI) indicator. It is set to 1 whenever the received data input is held in the Spacing (0) state for longer than a full word transmission time (i.e., the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character that it applies to in the FIFO. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs only one character is loaded into the FIFO. To Restart after a break is received, the SIN pin must be 1 for at least one half bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5 This bit is the Transmitter Holding Register Empty (THRE) indicator. It indicates that the UART is ready to accept a new character for transmission. In addition, it causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to 0 whenever the CPU loads the Transmitter Holding Register. In the FIFO mode it is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6 This bit is the Transmitter Empty (TEMT) indicator. It is set to 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to 0 if either the THR or TSR contains a data character. In the FIFO mode this bit is set to 1 whenever the transmitter FIFO and the shift register are both empty.

Bit 7 In the NS16450 Mode this is 0. In the FIFO Mode this bit is set when there is at least one parity error, framing error or break indication in the FIFO. It is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing. In the FIFO mode the software must load a data byte in the Rx FIFO via the Loopback Mode in order to write to LSR2–LSR4. LSR0 and LSR7 can't be written to in the FIFO Mode.

6.5 FIFO CONTROL REGISTER (FCR)

This is a write-only register at the same location as the IIR (the IIR is a read-only register). This register is used to enable the FIFOs, clear the FIFOs and to set the RCVR FIFO trigger level.

Bit 0 Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 clears all bytes in both FIFOs. When changing from FIFO Mode to NS16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must already be 1 when other FCR bits are written to or they will not be programmed.

Bit 1 Writing 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2 Writing 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3 Writing to FCR3 does not change UART operations.

Bits 4, 5 FCR4 to FCR5 are reserved for future use.

Bits 6, 7 The combination of FCR6 and FCR7 is used to designate the interrupt trigger level (see *Figure 6.2*). When the number of bytes in the RCVR FIFO equals the designated interrupt trigger level, a Received Data Available Interrupt is activated. This interrupt must be enabled by setting the Interrupt Enable Register (IER) bit 0.

FCR Bits		RCVR FIFO Trigger Level (Bytes)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIGURE 6-2. Receiver FIFO Trigger Level

6.6 INTERRUPT IDENTIFICATION REGISTER (IIR)

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates to the CPU which pending interrupt has the highest priority. While the CPU accesses this interrupt routine, the UART records new interrupts, but does not change its current indication until the current access is complete. Table 6-2 shows the contents of the IIR. Details on each bit follow:

Bit 0 This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When it is 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When it is 1, no interrupt is pending. See Table 6-5.

Bits 1, 2 These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 6-5.

Bit 3 In the 16450 mode this bit is 0. In the FIFO mode it is set along with bit 2 when a time-out interrupt is pending. See Table 6-5.

Bits 4, 5 These bits of the IIR are always 0.

Bits 6, 7 These two bits are set when FCR0 = 1. (FIFO Mode enabled.)

TABLE 6-5. PC87332 Interrupt Control Functions

Interrupt Identification Register				Interrupt Set and Reset Functions			
Bit 3 (FIFO Mode Only)	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer
1	1	0	0	Second (FIFO mode only)	Character Time-Out Indication	No Characters have been removed from or input to the RCVR FIFO during the last 4 char. times and there is at least 1 char. in it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

6.7 INTERRUPT ENABLE REGISTER (IER)

This register enables the five types of UART interrupts. Each interrupt can individually activate the appropriate inter rupt (IRQ3 or IRQ4) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of this register to 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the interrupt output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table 6-2 shows the contents of the IER. Details on each bit follow. See MODEM Control Register bit 3 for more information on enabling the interrupt pin.

Bit 0 When set to 1 this bit enables the Received Data Available Interrupt and Timeout Interrupt in the FIFO Mode.

Bit 1 This bit enables the Transmitter Holding Register Empty Interrupt when set to 1.

Bit 2 This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3 This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4–7 These four bits are always logic 0.

6.8 MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register (MCR) are indicated in Table 6-2 and are described as follows:

Bit 0 This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When it is set to 1, the $\overline{DTR}$ output is forced to a logic 0. When it is reset to 0, the $\overline{DTR}$ output is forced to 1. In Local Loopback Mode, this bit controls bit 5 of the MODEM Status Register.

Note: The $\overline{DTR}$ and $\overline{RTS}$ output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the MODEM or data set.

Bit 1 This bit controls the Request to Send ($\overline{RTS}$) output. Its effect on the $\overline{RTS}$ output is identical to that described above for bit 0. In Local Loopback Mode, this bit controls bit 4 of the MODEM Status Register.

Bit 2 This bit is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In Local Loopback Mode, this bit controls bit 6 of the MODEM Status Register.

Bit 3 This bit enables the interrupt when set. No external pin is associated with this bit other than IRQ3, 4. In Local Loopback Mode, this bit controls bit 7 of the MODEM Status Register.

Bit 4 This bit provides a Local Loopback feature for diagnostic testing of the UART. When it is set to 1, the following changes take place: the transmitter Serial Output (SOUT) is set to the Marking (1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is ''looped back'' (connected) to the Receiver Shift Register; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, RI and $\overline{DCD}$) are disconnected; and the DTR, RTS, OUT1, IRQ ENABLE bits in MCR are internally connected to DSR, CTS, RI and DCD in MSR, respectively. The MODEM Control output pins are forced to their high (inactive) states. In the Loopback Mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-received-data paths of the serial port.

In the Loopback Mode, the receiver and transmitter interrupts are fully operational. The MODEM Status Interrupts are also operational, but the interrupts' sources are the lower four bits of MCR instead of the four MODEM control inputs. Writing a 1 to any of these 4 MCR bits will cause an interrupt. In Loopback Mode the interrupts are still controlled by the Interrupt Enable Register. The IRQ3 and IRQ4 pins will be at TRI-STATE in the Loopback Mode.

Bits 5–7 These bits are permanently set to 0.

6.9 MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register. Table 6-2 shows the contents of the MSR. Details on each bit follow.

Bit 0 This bit is the Delta Clear to Send (DCTS) indicator. It indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1 This bit is the Delta Data Set Ready (DDSR) indicator. It indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2 This bit is the Trailing Edge of Ring Indicator (TERI) detector. It indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3 This bit is the Delta Data Carrier Detect (DDCD) indicator. It indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4 This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.

Bit 5 This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to 1, this bit is equivalent to DTR in the MCR.

Bit 6 This bit is the complement of the Ring Indicator (RI) input. If bit 4 of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.

Bit 7 This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to 1, this bit is equivalent to IRQ ENABLE in the MCR.

6.10 SCRATCHPAD REGISTER (SCR)

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

7.0 Parallel Port

7.1 INTRODUCTION

This parallel interface is designed to provide all of the signals and registers needed to communicate through a standard parallel printer port as found in the IBM PC-XT, PC-AT, PS/2 and Centronics systems. This parallel port supports three standard modes of operation: SPP, EPP, ECP. The Standard Parallel Port (SPP) is a software based protocol with performance of up to 150 kbps.

The Enhanced Parallel Port (EPP) is a hardware protocol which offers up to 2 Mbps.

The Extended Capabilities Port (ECP) is also a hardware protocol with up to 2 Mbps transfer rate. In addition, the ECP has FIFO's for receive and transmit, and DMA support, to reduce the CPU overhead. The ECP mode 0 is in fact compatible with the SPP mode. The ECP specification defines the AC/DC parameters of the signals to allow fast communication without termination problems.

All the above standards are incorporated into the 1284 IEEE specifications.

The address decoding of the registers utilizing A0 and A1 is shown in Table 7-1. Table 7-3 shows the Reset states of Parallel port registers and pin signals. These registers are shown in Section 7.2 to Section 7.4.

TABLE 7-1. Parallel Interface Register Addresses

A1	A0	Address	Register	Access
0	0	0	Data	Read/Write
0	1	1	Status	Read
1	0	2	Control	Read/Write
1	1	3	TRI-STATE	

Special circuitry provides protection against damage that might be caused when the printer is powered but the PC87332 is not.

There are two Standard Parallel Port (SPP) modes of operation (Compatible and Extended; see Table 7-2), two Enhanced Parallel Port (EPP) modes of operation and one Extended Capabilities Port (ECP) mode to complete a full IEEE 1284 parallel port.

TABLE 7-2. Standard Parallel Port Modes Selection

Port Function	PTR7
Compatible	0
Extended	1

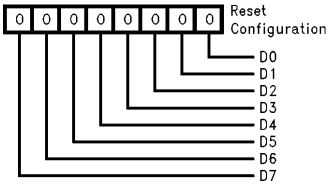
In Compatible mode a write operation causes the data to be presented on pins PD0–7. A read operation in this mode causes the Data Register to present the last data written to it by the CPU. See Table 7-3.

In the Extended mode a write operation to the data register causes the data to be latched. If the Data Port Direction bit (Control Register (CTR) bit 5) is 0, the latched data is presented to the pins and a read operation from this register allows the CPU to read the last data it wrote to the port. If CTR5 is 1, the data is only latched and a read from this register causes the port to present the data on pins PD0–7. See Table 7-2.

TABLE 7-3. SPP Data Register Read and Write Modes

PTR7	CTR5	$\overline{RD}$	$\overline{WR}$	Result
0	X	1	0	Data Written to PD0–7
0	X	0	1	Data Read from the Output Latch
1	0	1	0	Data Written to PD0–7
1	1	1	0	Data Written is Latched
1	0	0	1	Data Read from the Output Latch
1	1	0	1	Data Read from PD0–7

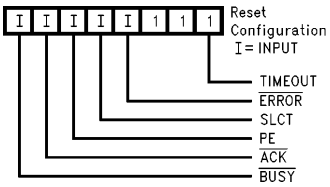
7.2 DATA REGISTER (DTR)



TL/C/11930–12

This is a bidirectional data port that transfers 8-bit data. The direction is determined by the Power and Test Configuration Register (PTR) bit 7 and the CTR5 bits. When PTR7 is high, the CTR5 bit will determine the data direction in conjunction with the Read and Write strobes. When PTR7 bit is low, the parallel port operates in the output mode only. The reset value of this register is 0. See Table 7-3.

7.3 STATUS REGISTER (STR)



TL/C/11930–13

This register provides status for the TIMEOUT, $\overline{ERROR}$, SLCT, PE, $\overline{ACK}$, and $\overline{BUSY}$ signals for a connected printer. It is a read only register. Writing to it is an invalid operation that has no effect.

Bit 0 When in EPP mode, this is the timeout status bit. When this bit is 0, no timeout.

When this bit is 1, timeout occurred on EPP cycle (minimum 10 μsec). It is cleared to 0 after STR is read, i.e., consecutive reads (after the first read) always return 0. It is also cleared to 0 when EPP is enabled (bit 0 of PCR is changed from 0 to 1).

When not in EPP mode, this bit is 1.

Bit 1 Reserved; this bit is always 1.

Bit 2 In the compatible mode (PTR7 bit is 0), or in ECP and EPP mode with bit 4 of PCR = 0, this bit is always one.

In the Extended Mode (PTR7 bit is 1), or in ECP and EPP with bit 4 of PCR = 1, this bit is the $\overline{IRQ}$ Status bit.

In the Extended mode, if CTR4 = 1, then this bit is latched low when the $\overline{ACK}$ signal makes a transition from low to high.

Reading this bit sets it to a 1.

Bit 3 This bit represents the current state of the printer error signal ($\overline{ERROR}$). The printer sets this bit low when there is a printer error. This bit follows the state of the $\overline{ERR}$ pin.

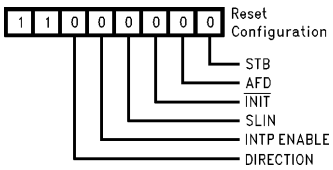
Bit 4 This bit represents the current state of the printer select signal (SLCT). The printer sets this bit high when it is selected. This bit follows the state of the SLCT pin.

Bit 5 This bit represents the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

Bit 6 This bit represents the current state of the printer acknowledge signal ($\overline{ACK}$). The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the $\overline{ACK}$ pin.

Bit 7 This bit represents the current state of the printer busy signal ($\overline{BUSY}$). The printer sets this bit low when it is busy and cannot accept another character. This bit is the inverse of the (BUSY/$\overline{WAIT}$) pin.

7.4 CONTROL REGISTER (CTR)



TL/C/11930–14

This register provides all output signals to control the printer. Except for bit 5, it is a read and write register.

Bit 0 This bit (STB) directly controls the data strobe signal to the printer via the $\overline{STB}$ pin. This bit is the inverse of the $\overline{STB}$ pin.

Bit 1 This bit (AFD) directly controls the automatic feed XT signal to the printer via the $\overline{AFD}$ pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the $\overline{AFD}$ pin.

Bit 2 This bit ($\overline{INIT}$) directly controls the signal to initialize the printer via the $\overline{INIT}$ pin. Setting this bit to low initializes the printer. This bit follows the $\overline{INIT}$ pin.

Note: This bit must be set to 1 before enabling the EPP or ECP modes via bits 0 or 2 of the PCR register.

Bit 3 This bit directly controls the select-in (SLIN) signal to the printer via the $\overline{SLIN}$ pin. Setting this bit high selects the printer. It is the inverse of the $\overline{SLIN}$ pin.

Bit 4 This bit controls the interrupt generated by the $\overline{ACK}$ signal. Its function changes slightly depending on the parallel port mode selected. In ECP mode this bit should be set to 0. In the following description, IRQx indicates either IRQ5 or IRQ7 (based upon PTR3):

Compatible mode:
when bit 4 = 0 IRQx is floated
when bit 4 = 1 IRQx follows $\overline{ACK}$ transitions

Extended mode:
when bit 4 = 0 IRQx is floated
when bit 4 = 1 IRQx becomes active on $\overline{ACK}$ trailing edge

EPP mode:
when bit 4 = 0 IRQx is floated
when bit 4 = 1 IRQx is pulsed when $\overline{ACK}$ is activated, or an EPP timeout occurs

Bit 5 This bit determines the parallel port direction when bit 7 of PTR is 1. The default condition results in the parallel port being in the output mode. This is a **Read/Write** bit in EPP mode. In SPP mode it is a write only bit; a read from it will return 1. See Table 7-3 for further details.

Bits 6, 7 Reserved. These bits are always 1.

Normally when the Control Register is read, the bit values are provided by the internal output data latch. These bit values can be superseded by the logic level of the $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, and $\overline{SLIN}$ pins if these pins are forced high or low by an external voltage. In order to force these pins high or low the corresponding bits should be set to their inactive state (e.g., AFD = STB = SLIN = 0, $\overline{INIT}$ = 1). See Table 7-4.

TABLE 7-4. Parallel Port Reset States

Signal	Reset Control	State after Reset
$\overline{SLIN}$	MR	TRI-STATE
$\overline{INIT}$	MR	Zero
$\overline{AFD}$	MR	TRI-STATE
$\overline{STB}$	MR	TRI-STATE
IRQ5,7	MR	TRI-STATE

7.5 ENHANCED PARALLEL PORT OPERATION

EPP mode provides for greater throughput, and more complexity, than the Compatible or Extended modes by supporting faster transfer times and a mechanism that allows the host to address peripheral device registers directly. Faster transfers are achieved by automatically generating the address and data strobes. EPP is compatible with both Compatible and Extended mode parallel-port devices. It consists of eight (0–7) single-byte registers. (See Table 7-5.)

There are two EPP modes:

EPP rev. 1.7 is supported when bit 0 of PCR is 1, and bit 1 of PCR is 0.

EPP rev. 1.9 (IEEE 1284) is supported when bit 0 of PCR is 1, and bit 1 of PCR is 1.

EPP is supported for a parallel port whose base address is 278h or 378h, but not for a parallel port whose base address is 3BCh (there are no EPP registers at 3BFh). There are four EPP transfer operations: address write, address read, data write and data read. An EPP transfer operation is composed of a host read or write cycle (from or to an EPP register) and an EPP read or write cycle (from a peripheral device to an EPP register, or from an EPP register to a peripheral device).

TABLE 7-5. EPP Register Addresses

A2	A1	A0	Address	Register	Access	Description
0	0	0	0	Data (DTR)	R/W	A write to this register sets the state of the eight data pins on the 25-pin D-shell connector.
0	0	1	1	Status (STR)	R	A read from this register presents the system micro-processor with the real-time status of five pins on the 25-pin D-shell connector, and the IRQ.
0	1	0	2	Control (CTR)	R/W	A write operation to this register sets the state of four pins on the 25-pin D-shell connector, and controls both the parallel port interrupt enable and direction.
0	1	1	3	Address	R/W	A write operation to this register initiates an EPP device/register selection operation.
1	0	0	4	Data Port 0	R/W	Accesses to this port initiate device read or write operations with bits 0–7.
1	0	1	5	Data Port 1	R/W	This port is only accessed to transfer bits 8 to 15 of a 16-bit read or write to data port 0.
1	1	0	6	Data Port 2	R/W	This port is only accessed to transfer bits 16 to 23 of a 32-bit read or write to data port 0.
1	1	1	7	Data Port 3	R/W	This port is only accessed to transfer bits 24 to 31 of a 32-bit read or write to data port 0.

The software must write zero to bits 0, 1 and 3 of the CTR register, before accessing the EPP registers, since the pins controlled by these bits are controlled by hardware during EPP access. Once these bits are written with zero, the software may issue multiple EPP access cycles. The software must set bit 7 of the PTR register to 1, if bit 5 of CTR is to control direction.

To meet the EPP 1.9 specifications, the software should change direction (bit 5 of CTR) only when bit 7 of STR is 1 (i.e., change direction at EPP Idle Phase, as defined in the IEEE 1284 document).

When bit 7 of PTR is 0, EPP cycles to the external device are generated by invoking read or write cycles to the EPP.

When bit 7 of PTR is 1:

1. Reading an EPP register during forward direction (bit 5 of CTR is 0) is allowed only in EPP 1.7. It returns the register latched value (not the PD0–7 pins' value), and does not generate an EPP read cycle.
2. Writing to an EPP register during backward direction (bit 5 of CTR is 1) updates the register data, and does not generate an EPP write cycle.

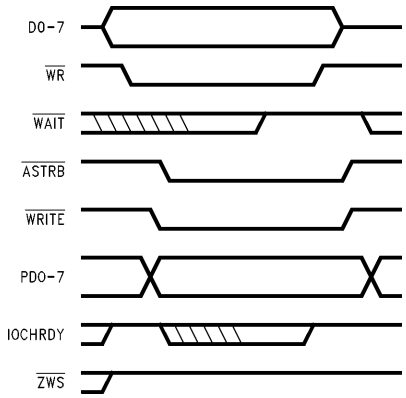
EPP 1.7 Address Write

The following procedure selects a peripheral device or register. See also *Figure 7-1*.

1. The host writes a byte to the EPP address register. $\overline{WR}$ goes low to latch D0–7 into the address register. The latch drives the address register onto PD0–7 and the EPP pulls $\overline{WRITE}$ low.
2. The EPP pulls $\overline{ASTRB}$ low to indicate that data has been sent.
3. If $\overline{WAIT}$ is low during the host write cycle, IOCHRDY goes low.

   When $\overline{WAIT}$ goes high, the EPP pulls IOCHRDY high.
4. When IOCHRDY goes high it causes $\overline{WR}$ to go high. If $\overline{WAIT}$ is high during the host write cycle then the EPP does not pull IOCHRDY to low.
5. When $\overline{WR}$ goes high it causes the EPP to pull $\overline{WRITE}$ and $\overline{ASTRB}$ to high.

   Only when $\overline{WRITE}$ and $\overline{ASTRB}$ are high can the EPP change PD0–7.



TL/C/11930–15

FIGURE 7-1. EPP 1.7 Address Write

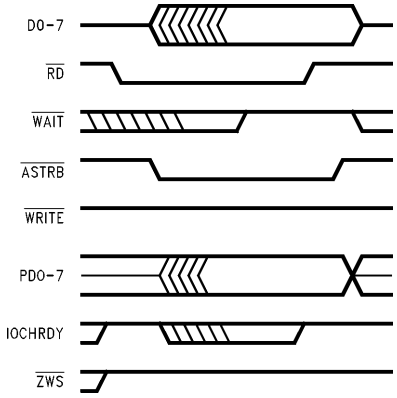
EPP 1.7 Address Read

The following procedure reads from the address register. See also *Figure 7-2*.

1. The host reads a byte from the EPP address register. $\overline{RD}$ goes low to gate PD0–7 into D0–7.
2. The EPP pulls $\overline{ASTRB}$ low to signal the peripheral to start sending data.
3. If $\overline{WAIT}$ is low during the host read cycle, then the EPP pulls IOCHRDY low.

   When $\overline{WAIT}$ goes high, the EPP stops pulling IOCHRDY to low.
4. When IOCHRDY goes high it causes $\overline{RD}$ to go high. If $\overline{WAIT}$ is high during the host read cycle then the EPP does not pull IOCHRDY to low.
5. When $\overline{RD}$ goes high, it causes the EPP to pull $\overline{ASTRB}$ high.

   Only when $\overline{ASTRB}$ is high can the EPP change PD0–7. After $\overline{ASTRB}$ goes high, the EPP pins D0–7 are at TRI-STATE.



TL/C/11930–16

FIGURE 7-2. EPP 1.7 Address Read

EPP 1.7 Data Write and Data Read

This procedure writes to the selected peripheral device or register. See also *Figure 7-3*.

An EPP 1.7 data write operation is similar to the EPP 1.7 address write operation, and an EPP 1.7 data read operation is similar to the EPP 1.7 address read operation, except that the data strobe ($\overline{DSTRB}$ signal), and a data register, replace the address strobe ($\overline{ASTRB}$ signal) and the address register respectively.

EPP Zero Wait State (ZWS) Address Write Operation (both 1.7 and 1.9)

The following procedure performs a short write to the selected peripheral device or register.

ZWS should be configured as follows: bit 5 of FCR is 1 and bit 6 of FCR is 0.

1. The host writes a byte to the EPP address register. $\overline{WR}$ goes low to latch D0–7 into the data register. The latch drives the data register onto PD0–7.
2. The EPP first pulls $\overline{WRITE}$ low, and then pulls $\overline{ASTRB}$ low to indicate that data has been sent.
3. If $\overline{WAIT}$ is high during the host write cycle, $\overline{ZWS}$ goes low and IOCHRDY goes high.
4. When the host pulls $\overline{WR}$ high, the EPP pulls $\overline{ASTRB}$, $\overline{ZWS}$ and $\overline{WRITE}$ to high.

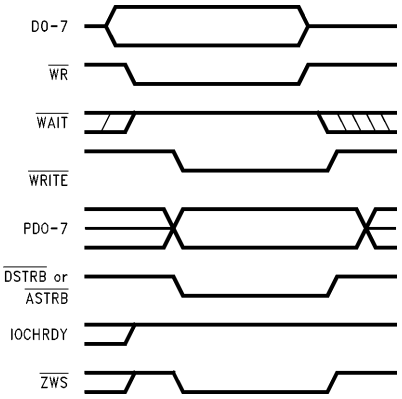
   Only when $\overline{WRITE}$ and $\overline{ASTRB}$ are high can the EPP change PD0–7.

Note: Read operation is similar, except for data direction, and activation of $\overline{RD}$ instead of write.

5. If the peripheral is fast enough to pull $\overline{WAIT}$ low before the host terminates the write cycle, the EPP pulls IOCHRDY to low, but does not pull $\overline{ZWS}$ to low, thus carrying out a normal (non-ZWS EPP 1.7) write operation.

EPP Zero Wait State (ZWS) Data Write Operation (both 1.7 and 1.9)

EPP 1.7 and 1.9 Zero Wait State data write/read operations are similar to the EPP Zero Wait State address write/read operations, with the exception that the data strobe ($\overline{DSTRB}$ signal), and a data register, replace the address strobe ($\overline{ASTRB}$ signal) and the address register, respectively. See *Figure 7-3*.



TL/C/11930–17

FIGURE 7-3. EPP Write with ZWS

EPP 1.9 Address Write

The following procedure selects a peripheral or register. See also *Figure 7-4*.

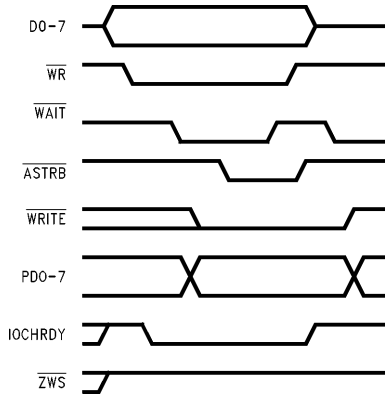
1. The host writes a byte to the EPP address register.
2. The EPP pulls IOCHRDY low, and waits for $\overline{WAIT}$ to go low.
3. When $\overline{WAIT}$ goes low the EPP pulls $\overline{WRITE}$ to low and drives the latched byte onto PD0–7.

   If $\overline{WAIT}$ was already low, then steps 2 and 3 occur concurrently.
4. The EPP pulls $\overline{ASTRB}$ low and waits for $\overline{WAIT}$ to go high.
5. When $\overline{WAIT}$ goes high, the EPP stops pulling IOCHRDY low, pulls $\overline{ASTRB}$ high, and waits for $\overline{WAIT}$ to go low.

7.0 Parallel Port (Continued)

6. Only if no EPP write is pending, when $\overline{WAIT}$ goes low (or when bit 7 of PTR is 1, and the direction is changed to Backwards by setting bit 5 of CTR to 1), the EPP pulls $\overline{WRITE}$ to high.

   If an EPP write is pending, $\overline{WRITE}$ remains low and the EPP may change PD0–7.



TL/C/11930–18

FIGURE 7-4. EPP 1.9 Address Write

EPP 1.9 Address Read

The following procedure reads from the address register. See also *Figure 7-5*.

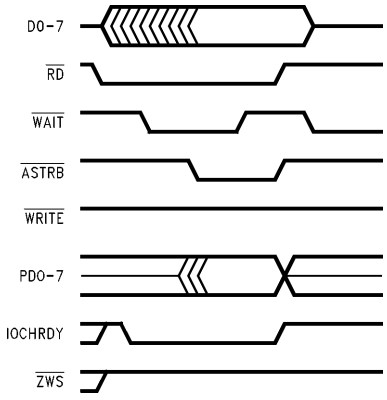
1. The host reads a byte from the EPP address register. When $\overline{RD}$ goes low, the EPP pulls IOCHRDY low, and waits for $\overline{WAIT}$ to go low.
2. When $\overline{WAIT}$ goes low, the EPP pulls $\overline{ASTRB}$ low and waits for $\overline{WAIT}$ to go high.

   If wait was already low, steps 2 and 3 occur concurrently.
3. When $\overline{WAIT}$ goes high, the EPP stops pulling IOCHRDY low, latches PD0–7, and pulls $\overline{ASTRB}$ high.
4. When $\overline{RD}$ goes high, the EPP pins D0–7 are at TRI-STATE.

EPP 1.9 Data Write and Data Read

This procedure writes to the selected peripheral drive or register. See *Figure 7-5*.

EPP 1.9 data read and write operations are similar to EPP 1.9 address read and write operations, respectively, except that the data strobe ($\overline{DSTRB}$ signal) and a data register replace the address strobe ($\overline{ASTRB}$ signal) and the address register.



TL/C/11930–19

FIGURE 7-5. EPP 1.9 Address Read

Parallel Port Multiplexor (PPM)

A PPM is used for a PC to interface with either a printer or an external FDD, via a 25-pin DIN connector. It may have an internal Floppy Disk Drive (FDD) connected via regular FDC pins. The printer and external FDD may be switched without turning the PC off, and without updating the DOS device tables. The software may assign ''A:'' to the FDD connected to the regular FDC pins, and ''B:'' to the FDD connected to the PPM pins (the default assignment), or vice versa.

The Multiplexors:

1. The FDC output signals are always connected to the regular FDC output pins.

   The FDC output signals are connected to the PPM output pins when the PPM is enabled (bit 2 of FCR is 1) and a floppy drive is connected to it (PFN = 0). (See Table 7-5.)

   The FDC input signals are connected to the regular FDC pins when either bit 2 of FCR is 0 or PNF = 1.

   The FDC input pins are internally multiplexed between the regular FDC pins and the PPM pins when bit 2 of FCR is 1 and PNF = 0 as follows:

   — the PPM pins are connected to the FDC input signals when $\overline{DR1}$ = 0

   — the regular pins are connected to the FDC input signals when $\overline{DR1}$ = 1
2. Floating the PPM pins:

   To support ''true'' floating pins, the pins are back-drive protected.

   When bit 3 of FCR is 1, the PPM pins are floated.

7.0 Parallel Port (Continued)

3. Multiplexing parallel port signals with FDC signals on the PPM pins:

   When the PPM is not enabled (bit 2 of FCR is 0), the parallel port signals are connected to the PPM pins.

   When bit 2 of FCR is 1, and PNF = 1, the parallel port signals are connected to the PPM pins.

   When bit 2 of FCR is 1, and PNF = 0, the FDC output signals are connected to the PPM pins.

   Reading back the DTR or CTR returns their written values and thus the parallel port module sees ''cable not connected''.

   Input signals assume their default values (STR register):

   BUSY = 1, PE = 0, SLCT = 0, $\overline{ACK}$ = 1

Table 7-6 shows the standard 25-pin, D-type connector definition for various parallel port operations.

TABLE 7-6. Parallel Port Pin Out

Connector Pin No.	Chip Pin No.	SPP, ECP Mode	Pin Direction	EPP Mode	Pin Direction	PPM Mode and PNF = 0	Pin Direction
1	95	$\overline{STB}$	I/O	$\overline{WRITE}$	I/O	—	—
2	94	PD0	I/O	PD0	I/O	$\overline{INDEX}$	I
3	93	PD1	I/O	PD1	I/O	$\overline{TRK0}$	I
4	92	PD2	I/O	PD2	I/O	$\overline{WP}$	I
5	91	PD3	I/O	PD3	I/O	$\overline{RDATA}$	I
6	89	PD4	I/O	PD4	I/O	$\overline{DSKCHG}$	I
7	88	PD5	I/O	PD5	I/O	MSEN0	I
8	87	PD6	I/O	PD6	I/O	—	—
9	86	PD7	I/O	PD7	I/O	MSEN1	I
10	85	$\overline{ACK}$	I	$\overline{ACK}$	I	$\overline{DR1}$	O
11	84	BUSY	I	$\overline{WAIT}$	I	$\overline{MTR1}$	O
12	83	PE	I	PE	I	$\overline{WDATA}$	O
13	82	SLCT	I	SLCT	I	$\overline{WGATE}$	O
14	78	$\overline{AFD}$	I/O	$\overline{DSTRB}$	I/O	DENSEL	O
15	79	$\overline{ERR}$	I	$\overline{ERR}$	I	$\overline{HDSEL}$	O
16	80	$\overline{INIT}$	I/O	$\overline{INIT}$	I/O	$\overline{DIR}$	O
17	81	$\overline{SLIN}$	I/O	$\overline{ASTRB}$	I/O	$\overline{STEP}$	O

7.6 EXTENDED CAPABILITIES PARALLEL PORT (ECP)

7.6.1 Introduction

The ECP support includes a 16-byte FIFO that can be configured for either direction, command/data FIFO tags (one per byte), a FIFO threshold interrupt for both directions, FIFO empty and full status bits, automatic generation of strobes (by hardware) to fill or empty the FIFO, transfer of commands and data, and a Run Length Encoding (RLE) expanding (decompression) as explained below.

The Extended Capabilities Port (ECP) is enabled when bit 2 of PCR is 1. Once enabled, its mode is controlled via the mode field of ECR—bits 5, 6, 7 of the ECR register.

The ECP has ten registers: See Table 7-7.

The AFIFO, CFIFO, DFIFO and TFIFO registers access the same ECP FIFO. The FIFO is accessed at Base + 000h, or Base + 400h, depending on the mode field of ECR and the register.

The FIFO can be accessed by host DMA cycles, as well as host PIO cycles.

When DMA is configured and enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically (by hardware) issues DMA requests to fill the FIFO (in the forward direction when bit 5 of DCR is 0) or to empty the FIFO (in the back ward direction when bit 5 of DCR is 1). All DMA transfers are to or from these registers. The ECP does not assert a DMA request for more than 32 consecutive DMA cycles. The ECP stops requesting DMA when Terminal Count, TC, is detected during an ECP DMA cycle.

A write operation to a full FIFO, or a read operation from an empty FIFO, are ignored. The written data is lost, and the read data is undefined. The FIFO empty and full status bits are not affected by such an access.

Some registers are not accessible in all modes of operation, or may be accessed in one direction only. Accessing a non-accessible register has no effect: Data read is undefined, data written is ignored, the FIFO does not update. The PC87334 Parallel Port registers (DTR, STR and CTR) are not accessible when ECP is enabled.

To improve noise immunity in ECP cycles, the state machine does not examine the control handshake response lines until the data has had time to switch.

In ECP mode:

DATAR replaces DTR of SPP/EPP
DSR replaces SPR of SPP/EPP
DCR replaces CTR of SPP/EPP

A detailed description of the various modes follow in Sections 7.8–7.11.

TABLE 7-7. ECP Registers Summary

A10	A1	A0	Offset Address	Register	Access	Size	Mode # ECR (5–7)	Function
0	0	0	0	DATAR	R/W	Byte	000,001	Parallel Port Data Register
0	0	0	0	AFIFO	W	Byte	011	ECP Address FIFO
0	0	1	1	DSR	R	Byte	ALL	Status Register
0	1	0	2	DCR	R/W	Byte	ALL	Control Register
1	0	0	3	CFIFO	W	Byte	010	Parallel Port Data FIFO
1	0	0	3	DFIFO	R/W	Byte	011	ECP Data FIFO
1	0	0	3	TFIFO	R/W	Byte	110	Test FIFO
1	0	0	3	CNFGA	R	Byte	111	Configuration Register A
1	0	1	4	CNFGB	R	Byte	111	Configuration Register B
1	1	0	5	ECR	R/W	Byte	ALL	Extended Control Register

Note: The Base address is stored in bits A2–A9. It is 278h, 378h or 3BCh, as specified in the FAR register.

7.6.2 Software Operation

Software operation is detailed in the IEEE document *Extended Capabilities Port Protocol and ISA Interface Standard*. To highlight the ECP usage some software operations are detailed below:

1. The software should enable ECP (bit 2 of PCR is 1) after bits 0–3 of the Parallel Port Control Register (CTR) are 100.
2. When ECP is enabled, and the software wishes to switch modes, it should switch only through modes 000 or 001.
3. When ECP is enabled, the software should change direction only in mode 001.
4. The software should switch from mode 010 or 011, to mode 000 or 001, only when the FIFO is empty.
5. The software should switch to mode 011 when bits 0 and 1 of DCR are 0.
6. The software should switch to mode 010 when bit 0 of DCR is 0.
7. The software should disable ECP (bit 2 of PCR is 0) only when in mode 000 or 001.

Software may switch from mode 011 backward direction to modes 000 or 001 when there is an on-going ECP read cycle. In this case the read cycle is aborted by deasserting $\overline{AFD}$. The FIFO is reset (empty) and a potential byte expansion (RLE) is automatically terminated since the new mode is 000 or 001.

The $\overline{ZWS}$ signal is asserted by the ECP when ECP is enabled, and an ECP register is accessed by host PIO instructions, thus using a host zero wait state cycle.

The ECP uses the X1/OSC clock. This clock can be frozen (a power-down mode). When this power-down mode occurs, the DMA is disabled, all interrupts (except $\overline{ACK}$) are masked, and the FIFO registers are not accessible (access is ignored). The other ECP registers are always accessible when the ECP is enabled. During this period the FIFO status and contents are not lost, although the host reads bit 2 of ECR as 0, bit 1 of ECR as 1 and bit 0 of ECR as 1, regardless of the actual values of these bits. When the clock starts toggling again these bits resume their original functions (and values).

When the clock is frozen, an on-going ECP cycle may be corrupted, but the next ECP cycle will not start. This is true even if in forward direction the FIFO is not empty, and in backward direction the FIFO is not full. If the ECP clock starts or stops toggling during a host cycle that accesses the FIFO, the cycle may yield invalid data.

Note 1: The ECP outputs are inactive when the ECP is disabled.

Note 2: Only the FIFO/DMA/RLE are not functional when the clock is frozen. All other registers are accessible and functional. The FIFO/DMA/RLE are affected by ECR modifications, i.e., they are reset even when exits from modes 010/011 are carried out while the clock is frozen.

7.7 REGISTER DEFINITIONS

DATAR: Parallel Port Data Register. Same as DTR register, except that read always returns the values of the PD0–7 pins (not the register latched data).

AFIFO: ECP Address FIFO Register. Write Only. In the forward direction (bit 5 of DCR is 0) a byte written into this register is pushed into the FIFO and tagged as a command.

Unpredictable results will occur when reading this register. Writes to this register during backward direction (bit 5 of DCR is 1) have no effect and the data is ignored.

DSR: Data Status Register. Read only. Same as the current STR register, except for bit 2, which is reserved.

Writes to this register have no effect and the data is ignored.

Note: The FDC has a register of the same name (DSR).

DCR: Data Control Register. Same as the current SPP CTR register, with the following exceptions:

When bit 5 of the DCR is 0 the ECP is in forward direction, and when bit 5 is 1 the ECP is in backward direction.

The ECP drives the PD0–7 pins in the forward direction but does not drive them in the backward direction.

The direction bit, bit 5, is readable and writable, except in modes 000 and 010. In modes 000 and 010 the direction bit is forced to 0, and data written into this bit is ignored.

Bit 4 of the DCR enables the $\overline{ACK}$ deassertion interrupt event (1 = enable, 0 = mask). If a level interrupt is configured (bit 4 of PCR is 1) clearing this bit clears the $\overline{ACK}$ pending interrupt request. This bit does not float the IRQ pin.

In modes 010 and 011 the $\overline{STB}$ is controlled by both ECP hardware and software (bit 0 of this register).

In mode 011 the $\overline{AFD}$ is controlled by both ECP hardware and software (bit 1 of this register).

CFIFO: Parallel Port FIFO Register. Write only. A byte written, or DMAed, to this register is pushed into the FIFO and tagged as data. Reading this register has no effect and the data read is undefined.

DFIFO: ECP Data FIFO Register. In the forward direction (bit 5 of DCR is 0) a byte written, or DMAed, to this register is pushed into the FIFO and tagged as data. Reading this register has no effect and the data read is undefined.

In the backward direction (bit 5 of DCR is 1) the ECP automatically issues ECP read cycles to fill the FIFO. Reading this register pops a byte from the FIFO. Writing this register has no effect and the data written is ignored.

TFIFO: Test FIFO Register. A byte written into this register is pushed into the FIFO. A byte read from this register is popped from the FIFO. The ECP does not issue a ECP cycle to transfer the data to or from the peripheral device.

The TFIFO is readable and writable in both directions. In the forward direction (bit 5 of DCR is 0) PD0–7 is driven, but the data is undefined.

The FIFO does not stall when overwritten or underrun (access is ignored). Bytes are always read from the top of the FIFO, regardless of the direction bit (bit 5 of DCR). For example if 44h, 33h, 22h, 11h are written into the FIFO, reading the FIFO returns 44h, 33h, 22h, 11h (in the same order it was written).

CNFGA: Configuration Register A. Read only. Reading this register always returns 00010000. Writing this register has no effect and the data is ignored.

CNFGB: Configuration Register B. Read only. Reading this register returns the configuration parallel port interrupt line, and its state, as follows.

Bit 7 This bit is always 0.

Bit 6 Holds the (non-inverted) value on the configured IRQ pin.

Bits 5, 4 These bits are 1 when IRQ5 is configured, and 0 when IRQ7 is configured.

Bit 3 This bit is always 1.

Bits 2, 1, 0 These bits are always 0. Writing to this register has no effect and the data is ignored.

ECR: Extended Control Register. This register controls the ECP and parallel port functions. On reset this register is initialized to 00010101. IOCHRDY is driven low on an ECR read when the ECR status bits do not hold updated data.

Bit 7, 6, 5 These three bits determine the mode of operation. (Mode) Bit 7 is the MSB.

000: Standard mode. Write cycles are performed under software control.

Bit 5 of DCR is forced to 0 (forward direction) and PD0−7 is driven. The FIFO is reset (empty).

001: PS/2 mode. Read and write cycles are performed under software control. The FIFO is reset (empty).

010: Parallel Port FIFO mode. Write cycles are performed under hardware control ($\overline{STB}$ is controlled by hardware). Bit 5 of DCR is forced to 0 (forward direction) and PD0−7 are driven.

011: ECP FIFO mode. The FIFO direction is controlled by bit 5 of DCR.

Read and write cycles to the device are performed under hardware control ($\overline{STB}$ and $\overline{AFD}$ are controlled by hardware).

100: Reserved.

101: Reserved.

110: FIFO test mode. The FIFO is accessible via the TFIFO register.

The ECP does not issue ECP cycles to fill/empty the FIFO.

111: Configuration mode. The CNFGA and CNFGB registers are accessible in this mode.

Bit 4 ECP Interrupt Mask bit. When this bit is 0 an interrupt is generated on $\overline{ERR}$ assertion (the high-to-low edge of $\overline{ERR}$). An interrupt is also generated when ERR is asserted while this bit is changed from 1 to 0; this prevents the loss of an interrupt between an ECR read and ECR write. When this bit is 1, no interrupt is generated.

Bit 3 ECP DMA Enable bit. When this bit is 0, DMA is disabled and the PDRQ pin is in TRI-STATE. When this bit is 1, DMA is enabled and DMA starts when bit 2 of ECR is 0.

Note: $\overline{PDACK}$ is assumed inactive when this bit is 0.

Bit 2 ECP Service bit. When this bit is 0, and one of the following three interrupt events occur, an interrupt is generated and this bit is set to 1 by hardware.

1. Bit 3 of ECR is 1 and terminal count is reached during DMA.

2. Bit 3 of ECR is 0 and bit 5 of DCR is 0, and there are eight or more bytes free in the FIFO.

3. Bit 3 of ECR is 0 and bit 5 of DCR is 1, and there are eight or more bytes to be read from the FIFO.

When this bit is 1, DMA and the above three interrupts are disabled.

Writing 1 to this bit does not cause an interrupt.

When the ECP clock is frozen this bit is read as 0, regardless of its actual value (even though the bit may be modified by software when the ECP clock is frozen).

Bit 1 FIFO Full bit. Read only.

This bit is 0 when the FIFO has at least one free byte.

This bit is 1 when the FIFO is full.

This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored.

When the ECP clock is frozen this bit is read as 1, regardless of the actual FIFO state.

Bit 0 FIFO Empty bit. Read only.

This bit is 0 when the FIFO has at least one byte of data.

This bit is 1 when the FIFO is empty.

This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored.

When the ECP clock is frozen, this bit is read as 1, regardless of the actual FIFO state.

7.8 SOFTWARE CONTROLLED DATA TRANSFER (Modes 000 and 001)

Software controlled data transfer is supported in modes 000 and 001. The software generates peripheral-device cycles by modifying the DATAR and DCR registers and reading the DSR, DCR and DATAR registers. The negotiation phase and nibble mode transfer, as defined in the IEEE 1284 standard, are performed in these modes.

In these modes the FIFO is reset (empty) and is not functional. The DMA and RLE are idle.

Mode 000 is for the forward direction only; the direction bit is forced to 0 and PD0−7 is driven. Mode 001 is for both the forward and backward directions. The direction bit controls whether PD0−7 are driven.

7.9 AUTOMATIC DATA TRANSFER (Modes 010 and 011)

Automatic data transfer (ECP cycles generated by hardware) is supported only in modes 010 and 011. Automatic DMA access to fill or empty the FIFO is supported in modes 010, 011 and 110. Mode 010 is for the forward direction only. The direction bit is forced to 0 and PD0–7 is driven. Mode 011 is for both the forward and backward directions. The direction bit controls whether PD0–7 is driven.

Automatic Run Length Expanding (RLE) is supported in the backward direction.

Note 1: FIFO-full condition is checked before every expanded byte push.

Note 2: A pending DMA request is removed and a pending RLE expansion is aborted when switching from modes 010 or 011 to other modes.

Note 3: The two FIFO ports are neither synchronized nor linked together, except via the empty and full FIFO status bits. The FIFO shall not delay the push and pop operations, even when they are performed concurrently. Care must be taken not to corrupt PD0–7 or D0–7 while the other FIFO port is accessed.

Note 4: In the forward direction, the empty bit is updated when the ECP cycle is completed, not right after the last byte is popped out of the FIFO (valid cleared on cycle end).

Note 5: $\overline{ZWS}$ is not asserted for DMA cycles.

Note 6: The one-bit command/data tag is used only in forward direction.

7.9.1 Forward Direction (Bit 5 of DCR = 0)

When the ECP is in forward direction and the FIFO is not full (bit 1 of ECR is 0) the FIFO can be filled by software writes to the FIFO registers (AFIFO and DFIFO in mode 011, and CFIFO in mode 010).

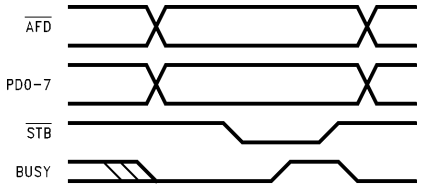
When DMA is enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically issues DMA requests to fill the FIFO with normal data bytes.

When the ECP is in forward direction and the FIFO is not empty (bit 0 of ECR is 0) the ECP pops a byte from the FIFO and issues a write cycle to the peripheral device. The ECP drives $\overline{AFD}$ according to the operation mode (ECR bits 5–7) and according to the tag of the popped byte as follows: In Parallel Port FIFO mode (mode 010) $\overline{AFD}$ is controlled by bit 1 of DCR. In ECP mode (mode 011) $\overline{AFD}$ is controlled by the popped tag. $\overline{AFD}$ is driven high for normal data bytes and driven low for command bytes.

7.9.2 ECP Forward Write Cycle

An ECP write cycle starts when the ECP drives the popped tag onto $\overline{AFD}$ and the popped byte onto PD0–7. When BUSY is low the ECP asserts $\overline{STB}$. In 010 mode the ECP deasserts $\overline{STB}$ to terminate the write cycle. In 011 mode the ECP waits for BUSY to be high.

When BUSY is high the ECP deasserts $\overline{STB}$. When $\overline{BUSY}$ is changed to low, it changes $\overline{AFD}$ and PD0–7.



TL/C/11930–20

FIGURE 7-6. ECP Forward Write Cycle

7.9.3 Backward Direction (Bit 5 of DCR is 1)

When the ECP is in the backward direction and the FIFO is not full (bit 1 of ECR is 0), the ECP issues a read cycle from the peripheral device and monitors the BUSY signal. If BUSY is high the byte is a data byte and it is pushed into the FIFO. If BUSY is low the byte is a command byte. The ECP checks bit 7 of the command byte, if it is high the byte is ignored, if it is low the byte is tagged as an RLC byte (not pushed into the FIFO but used as a Run Length Count to expand the next byte read). Following an RLC read, the ECP issues a read cycle from the peripheral device to read the data byte to be expanded. This byte is considered a data byte, regardless of its BUSY state (even if it is low). This byte is pushed into the FIFO (RLC + 1) times (i.e., RLC = 0: push the byte once, RLC = 127: push the byte 128 times).

When the ECP is in the backward direction and the FIFO is not empty (bit 0 of ECR is 0), the FIFO can be emptied by software reads from the FIFO register (only DFIFO in mode 011, no AFIFO and CFIFO read).

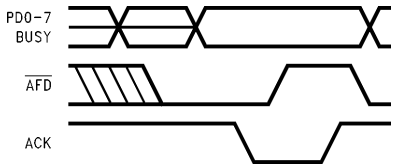
When DMA is enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically issues DMA requests to empty the FIFO (only in mode 011).

7.9.4 ECP Backward Read Cycle

An ECP read cycle starts when the ECP drives $\overline{AFD}$ low.

The peripheral device drives BUSY high for a normal data read cycle, or drives BUSY low for a command read cycle, and drives the byte to be read onto PD0–7.

When $\overline{ACK}$ is asserted the ECP drives $\overline{AFD}$ high. When $\overline{AFD}$ is high the peripheral device deasserts $\overline{ACK}$. The ECP reads the PD0–7 byte, then drives $\overline{AFD}$ low. When $\overline{AFD}$ is low the peripheral device may change BUSY and PD0–7 states in preparation for the next cycle.



TL/C/11930–21

FIGURE 7-7. ECP Backward Read Cycle

7.10 FIFO TEST ACCESS (Mode 110)

Mode 110 is used for testing the FIFO in PIO and DMA cycles. Both read and write operations (pop and push) are supported, regardless of the direction bit.

In the forward direction PD0–7 are driven, but the data is undefined. This mode can be used to measure the host-ECP cycle throughput, usually with DMA cycles. This mode can also be used to check the FIFO depth and its interrupt threshold, usually with PIO cycles.

7.0 Parallel Port (Continued)

7.11 CONFIGURATION REGISTERS ACCESS (Mode 111)

The two configuration registers, CNFGA and CNFGB, are accessible only in this mode.

7.12 INTERRUPT GENERATION

An interrupt is generated when any of the following events occur:

1. When bit 2 of ECR is 0, bit 3 of ECR is 1 and TC is asserted during the ECP DMA cycle.
2. When bit 2 of ECR is 0, bit 3 of ECR is 0, bit 5 of DCR is 0 and there are eight or more bytes free in the FIFO. It includes the case when bit 2 of ECR is cleared to 0 and there are already eight or more bytes free in the FIFO (modes 010, 011 and 110 only).
3. When bit 2 of ECR is 0, bit 3 of ECR is 0, bit 5 of DCR is 1 and there are eight or more bytes to be read from the FIFO. It includes the case when bit 2 of ECR is cleared to 0 and there are already eight or more bytes to be read from the FIFO (modes 011 and 110 only).
4. When bit 4 of ECR is 0 and $\overline{ERR}$ is asserted (high to low edge) or $\overline{ERR}$ is asserted when bit 4 of ECR is modified from 1 to 0.
5. When bit 4 of DCR is 1 and $\overline{ACK}$ is deasserted (low-to-high edge).

The interrupt is generated according to bits 5 and 6 of the PCR.

Note: Interrupt events #2, #3 and #4 are level events, thus they are shaped as interrupt pulses. These interrupts are masked (inactive) when the ECP clock is frozen. Interrupt event #1 is a pulse event. The last interrupt event behaves as in the normal SPP mode: the IRQ signal follows the $\overline{ACK}$ signal transition (when bit 5 of PCR is 0 and bit 6 of PCR is 0). Note that interrupt event #4 may be lost when the ECP clock is frozen.

8.0 Integrated Device Electronics Interface (IDE)

8.1 INTRODUCTION

Another key interface for PC design is facilitated through the use of the PC87332 **IDE** (Integrated Drive Electronics) Hard Disk interface. Only three buffer chips are required to construct the IDE Hard Disk Interface circuit.

The IDE interface is essentially the AT bus ported to the hard drive. The hard disk controller resides on the hard drive itself. So the IDE interface circuit must provide the AT bus signals, including data bits D15–0, address lines A3–0, as well as the common control signals.

8.2 IDE SIGNALS

Using 'LS244 devices in the IDE interface provides buffering of the control and address lines. Four control signals, $\overline{IDEHI}$, $\overline{IDELO}$, $\overline{HCS0}$, $\overline{HCS1}$, one status signal, $\overline{IOCS16}$, and one data signal, IDED7, are required by the IDE interface. The PC87332 provides all of these signals. They are summarized below.

$\overline{IDEHI}$ enables an 'LS245 octal bus transceiver for the upper data lines (D15–8) during 16-bit read and write operations at addresses 1F0–1F7. $\overline{IDEHI}$ will activate the 'LS245 only if the $\overline{IOCS16}$ output from the hard drive is active. $\overline{IDELO}$ enables another 'LS245 octal bus transceiver for the lower data lines (D7–0) during all (1F0–1F7, 3F6 and 3F7) reads and writes.

The IDED7 signal insures that the D7 data bus signal line is disabled for address 3F7 (this bit is used for the Disk Changed register on the floppy disk controller at that address).

8.0 Integrated Device Electronics Interface (IDE) (Continued)

The two 'LS245 chips are used to enable or TRI-STATE the data bus signals. In the PC-AT mode the PC87332 provides the two hard disk chip selects ($\overline{HCS0}$, $\overline{HCS1}$) for the IDE interface.

The $\overline{HCS0}$ output is active low when the 1F0–1F7h I/O address space is chosen and corresponds to the 1FX signal on the IDE header.

The $\overline{HCS1}$ output is active low when the 3F6 or 3F7 I/O addresses are chosen and corresponds to 3FX on the IDE header. These are the two address blocks used in the PC-AT hard disk controller.

Table 8-1 summarizes the addresses used by the PC-AT hard disk controller.

The equations shown in *Figure 8-1* define the signals of the PC87332 IDE pins.

TABLE 8-1. IDE Registers and Their ISA Addresses

Address	Read Function	Write Function
1F0	Data	Data
1F1	Error	Features (Write Precomp)
1F2	Sector Count	Sector Count
1F3	Sector Number	Sector Number
1F4	Cylinder Low	Cylinder Low
1F5	Cylinder High	Cylinder High
1F6	Drive/Head	Drive/Head
1F7	Status	Command
3F6	Alternate Status	Device Control
3F7	Drive Address (Note)	Not Used. Data Bus TRI-STATE

Note: Data bus bit D7 is dedicated to the floppy disk controller at this address. When reading this address the floppy disk controller disk change status will be provided by bit D7. There is no write function at this address in the IDE associated with this bit.

Equations	Comments
$\overline{HCS0} = \overline{A9}*A8*A7*A6*A5*A4*\overline{A3}*\overline{AEN}$	Active at 1F0–1F7
$\overline{HCS1} = A9*A8*A7*A6*A5*A4*\overline{A3}*A2*A1*\overline{AEN}$	Active at 3F6, 3F7
$\overline{IDELO} = [\overline{HCS0}*(\overline{RD} + \overline{WR})] + \{\overline{HCS1} * [(\overline{WR}*\overline{A0}) + \overline{RD}]\}$	Write 1F0–1F7, 3F6; Read 1F0–1F7, 3F6, 3F7
$\overline{IDEHI} = \overline{IOCS16}*\overline{HCS0}*(\overline{RD} + \overline{WR})$	Read or Write 1F0–1F7 in AT Mode
$IDED7\ (read) = (\overline{HCS0}*\overline{RD}) + [(\overline{HCS1}*\overline{A0})*\overline{RD}]$	Provides D7 during Read 1F0–1F7 and 3F6
$IDED7\ (write) = \overline{WR}*[\overline{HCS0} + (\overline{HCS1}*\overline{A0})]$	Provides D7 during Write 1F0–1F7 and 3F6

FIGURE 8-1. IDE Interface Signal Equations (Non-DMA)

9.0 Electrical Characteristics

9.1 DC Electrical Characteristics 5V ±10% (VLJ and VLJ-5)

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD}, V_{DDA})	−0.5V to +7.0V
Input Voltage (V_I)	−0.5 to V_{DD} +0.5V
Output Voltage (V_O)	−0.5 to V_{DD} +0.5V
Storage Temperature (T_{STG})	−65°C to +165°C
Power Dissipation (P_D)	1W
Lead Temperature (T_L) (Soldering, 10 seconds)	+260°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{DD})	4.5V to 5.5V
Operating Temperature (T_A)	0°C to 70°C
ESD Tolerance	1500V
C_{ZAP} = 100 pF	
R_{ZAP} = 1.5 kΩ (Note 3)	

CAPACITANCE T_A = 25°C, f = 1 MHz

Symbol	Parameter	Min	Typ	Max	Units
C_{IN}	Input Pin Capacitance		5	7	pF
C_{IN1}	Clock Input Capacitance		8	10	pF
C_{IO}	I/O Pin Capacitance		10	12	pF
C_O	Output Pin Capacitance		6	8	pF

DC CHARACTERISTICS Under Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
I_{CC}	V_{DD} Average Supply Current	V_{IL} = 0.5V V_{IH} = 2.4V No Load		20	55	mA
I_{CCSB} (Note 4)	V_{DD} Quiescent Supply Current in Low Power Mode	V_{IL} = V_{SS} V_{IH} = V_{DD} No Load		20		μA
I_{IL} (Note 5)	Input Leakage Current	V_{IN} = V_{DD}			10	μA
		V_{IN} = V_{SS}			−10	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Value based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

Note 4: The parameter I_{CCSB} is guaranteed by characterization. Due to test conditions, it is not 100% tested. I_{CCSB} is measured when UART1 and UART2's FCR bit is 1.

Note 5: During reset the MFM pin is rated for 10 μA; −150 μA leakage is due to an internal pull-up resistor. The $\overline{RTS1, 2}$ and SOUT1, 2 and $\overline{DTR1, 2}$ and $\overline{HCS0, 1}$ and $\overline{IDEHI}$ and $\overline{VLD0,1}$ and $\overline{IDEHLO}$ are rated for 200 μA; −160 μA leakage is due to internal pull-down resistors. During normal operation the BUSY, PE, and SLCT pins are rated for 100 μA; −200 μA leakage is due to internal pull-down resistors. The $\overline{ACK}$ and $\overline{ERR}$ pins are rated for 10 μA; −200 μA leakage is due to internal pull-up resistors.

9.0 Electrical Characteristics (Continued)

DC CHARACTERISTICS Under Recommended Operating Conditions (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MICROPROCESSOR AND IDE INTERFACE PINS						
V_{OH}	Output High Voltage	$I_{OH} = -15$ mA on: D0–7, IDED7, IRQ3–7, DRQ $I_{OH} = -6$ mA on: $\overline{DTR}$, $\overline{RTS}$, SOUT, MFM, DRATE0,1, $\overline{IDEHI}$, $\overline{IDELO}$, $\overline{HCS0}$, $\overline{HCS1}$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 24$ mA on: D0–7, IDED7, IRQ3–7, DRQ, $\overline{ZWS}$, IOCHRDY, MFM $I_{OL} = 12$ mA on: $\overline{DTR}$, $\overline{RTS}$, SOUT, $\overline{HCS0}$, $\overline{HCS1}$ $I_{OL} = 6$ mA on: DRATE0,1, $\overline{IDEHI}$, $\overline{IDELO}$			0.4	V
I_{OZ}	Input TRI-STATE Leakage Current (D7–0, IRQ3–7, DRQ)	$V_{IN} = V_{DD}$			50	μA
		$V_{IN} = V_{SS}$			−50	
DISK INTERFACE PINS (Note 6)						
V_H	Input Hysteresis			250		mV
V_{OH}	Output High Voltage (Note 7)	$I_{OH} = -4$ mA	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 40$ mA			0.4	V
I_{LKG}	Output High Leakage Current (Note 7)	$V_{IN} = V_{DD}$			10	μA
		$V_{IN} = V_{SS}$			−10	
OSCILLATOR PIN (X1/OSC)						
V_{IH}	XTAL1 Input High Voltage		2.0			V
V_{IL}	XTAL1 Input Low Voltage				0.4	V
I_{XLKG}	XTAL1 Leakage Current	$V_{IN} = V_{DD}$			400	μA
		$V_{IN} = V_{SS}$			−400	
PARALLEL PORT PINS						
I_{OH}	High Level Output Current (Note 8)	$V_{OH} = 2.4$V		12		mA
I_{OL}	Low Level Output Current	$V_{OL} = 0.4$V		12		mA

Note 6: When PPM is active and FDC is selected via the parallel port pins, the parallel port pins behave as the other Disk Interface pins. If FDC is not selected (PNF = 1) or PPM is not active, the parallel port pins behave normally.

Note 7: V_{OH} and I_{LKG} for the disk interface pins is valid for CMOS buffered outputs only.

Note 8: $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$, and $\overline{STB}$ are open drain pins when the PC87332 parallel port is operating in one of the following modes: Compatible, Extended, EPP1.7, ECP mode 0, or ECP mode 2 if PCR1 is 0. 4.7 kΩ resistors should be used.

9.0 Electrical Characteristics (Continued)

9.2 DC Electrical Characteristics 3.3V ±10% (VLJ)

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +7.0V
Input Voltage (V_I)	−0.5V to +5.5V
Output Voltage (V_O)	−0.5V to V_{DD} +0.3V
Storage Temperature (T_{STG})	−65°C to +165°C
Power Dissipation (P_D)	1W
Lead Temperature (T_L) (Soldering, 10 seconds)	+260°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{DD})	3.0V to 3.6V
Operating Temperature (T_A)	0°C to 70°C
ESD Tolerance	1500V
C_{ZAP} = 100 pF	
R_{ZAP} = 1.5 kΩ (Note 3)	

CAPACITANCE T_A = 25°C, f = 1 MHz

Symbol	Parameter	Min	Typ	Max	Units
C_{IN}	Input Pin Capacitance		5	7	pF
C_{IN1}	Clock Input Capacitance		8	10	pF
C_{IO}	I/O Pin Capacitance		10	12	pF
C_O	Output Pin Capacitance		6	8	pF

DC CHARACTERISTICS Under Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
I_{CC}	V_{DD} Average Supply Current	V_{IL} = 0.5V V_{IH} = 2.4V No Load		12	35	mA
I_{CCSB} (Note 4)	V_{DD} Quiescent Supply Current in Low Power Mode	V_{IL} = V_{SS} V_{IH} = V_{DD} No Load		10		μA
I_{IL} (Note 5)	Input Leakage Current	V_{IN} = V_{DD}			10	μA
		V_{IN} = V_{SS}			−10	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Value based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

Note 4: The parameter I_{CCSB} is guaranteed by characterization. Due to test conditions, it is not 100% tested. I_{CCSB} is measured when UART1 or 2's FCR bit is 1.

Note 5: During reset the MFM pin is rated for 10 μA; −150 μA leakage is due to an internal pull-up resistor. The $\overline{RTS1, 2}$ and SOUT1, 2 and $\overline{DTR1, 2}$ and $\overline{HCS0, 1}$ and $\overline{IDEHI}$ and $\overline{VLD0,1}$ and $\overline{IDEHLO}$ are rated for 200 μA; −160 μA leakage is due to internal pull-down resistors. During normal operation the BUSY, PE, and SLCT pins are rated for 100 μA; −200 μA leakage is due to internal pull-down resistors. The $\overline{ACK}$ and $\overline{ERR}$ pins are rated for 10 μA; −200 μA leakage is due to internal pull-up resistors.

9.0 Electrical Characteristics (Continued)

DC CHARACTERISTICS Under Recommended Operating Conditions (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MICROPROCESSOR AND IDE INTERFACE PINS						
V_{OH}	Output High Voltage	$I_{OH} = -7.5$ mA on: D0–7, IDED7, IRQ3–7, DRQ $I_{OH} = -3$ mA on: $\overline{DTR}$, $\overline{RTS}$, SOUT, PD0–7, MFM, DRATE0,1, $\overline{IDEHI}$, $\overline{IDELO}$, $\overline{HCS0}$, $\overline{HCS1}$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 12$ mA on: D0–7, IDED7, IRQ3–7, DRQ, $\overline{ZWS}$, IOCHRDY, MFM $I_{OL} = 6$ mA on: $\overline{DTR}$, $\overline{RTS}$, SOUT, $\overline{HCS0}$, $\overline{HCS1}$ $I_{OL} = 3$ mA on: DRATE0,1, $\overline{IDEHI}$, $\overline{IDELO}$			0.4	V
I_{OZ}	Input TRI-STATE Leakage Current (D7–0, IRQ3–7, DRQ)	$V_{IN} = V_{DD}$			50	μA
		$V_{IN} = V_{SS}$			−50	
DISK INTERFACE PINS (Note 6)						
V_H	Input Hysteresis			250		mV
V_{OH}	Output High Voltage (Note 7)	$I_{OH} = -2$ mA	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 20$ mA			0.4	V
I_{LKG}	Output High Leakage Current (Note 7)	$V_{IN} = V_{DD}$			10	μA
		$V_{IN} = V_{SS}$			−10	
OSCILLATOR PIN (X1/OSC)						
V_{IH}	XTAL1 Input High Voltage		2.0			V
V_{IL}	XTAL1 Input Low Voltage				0.4	V
I_{XLKG}	XTAL1 Leakage Current	$V_{IN} = V_{DD}$			400	μA
		$V_{IN} = V_{SS}$			−400	
PARALLEL PORT PINS						
I_{OH}	High Level Output Current (Note 8)	$V_{OH} = 2.4$V		12		mA
I_{OL}	Low Level Output Current	$V_{OL} = 0.4$V		12		mA

Note 6: When PPM is active and FDC is selected via the parallel port pins, the parallel port pins behave as the other Disk Interface pins. If FDC is not selected (PNF = 1) or PPM is not active, the parallel port pins behave normally.

Note 7: V_{OH} and I_{LKG} for the disk interface pins is valid for CMOS buffered outputs only.

Note 8: $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$, and $\overline{STB}$ are open drain pins when the PC87332 parallel port is operating in one of the following modes: Compatible, Extended, EPP1.7, ECP mode 0, or ECP mode 2 if PCR1 is 0. 4.7 kΩ resistors should be used.

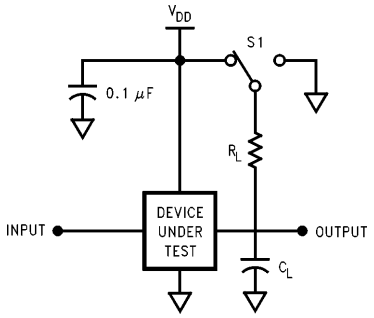
9.0 Electrical Characteristics (Continued)

9.3 AC Electrical Characteristics 5.0V ±10%, 3.3V ±10%

9.3.1 AC Test Conditions T_A = 0°C to 70°C, V_{DD} = 5.0V ± 10%, 3.3V ± 10%

Input Pulse Levels	Ground to 3V
Input Rise and Fall Times	6 ns
Input and Output Reference Levels	1.4V
TRI-STATE Reference Levels	Active High −0.5V Active Low +0.5V

LOAD CIRCUIT (Notes 1, 2, 3, 4)



TL/C/11930–22

AC TESTING INPUT AND OUTPUT WAVEFORM

TL/C/11930–23

Note 1: C_L = 100 pF, includes jig and scope capacitance.

Note 2: S1 = Open for push-pull outputs. S1 = V_{DD} for high impedance to active low and active low to high impedance measurements. S1 = GND for high impedance to active high and active high to high impedance measurements. R_L = 1.0 kΩ for μP interface pins.

Note 3: For the FDC Open Drive Interface Pins S1 = V_{DD} and R_L = 150Ω.

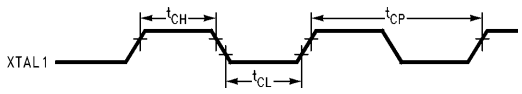
Note 4: For 3V operation, it is recommended to connect all reset strap pins to the CMOS input.

9.3.2 Clock Timing

Symbol	Parameter	Min	Max	Units
t_{CH}	Clock High Pulse Width	16		ns
t_{CL}	Clock Low Pulse Width	16		ns
t_{CP}	Clock Period	40	43	ns
t_{ICP}	Internal Clock Period	(See Table 10-1)		ns
t_{DRP}	Data Rate Period	(See Table 10-1)		ns

TABLE 9-1. Nominal t_{ICP} and t_{DRP} Values

MFM Data Rate	t_{DRP}	t_{ICP}	Value	Units
1 Mbps	1000	3 × t_{CP}	125	ns
500 kbps	2000	3 × t_{CP}	125	ns
300 kbps	3333	5 × t_{CP}	208	ns
250 kbps	4000	6 × t_{CP}	250	ns



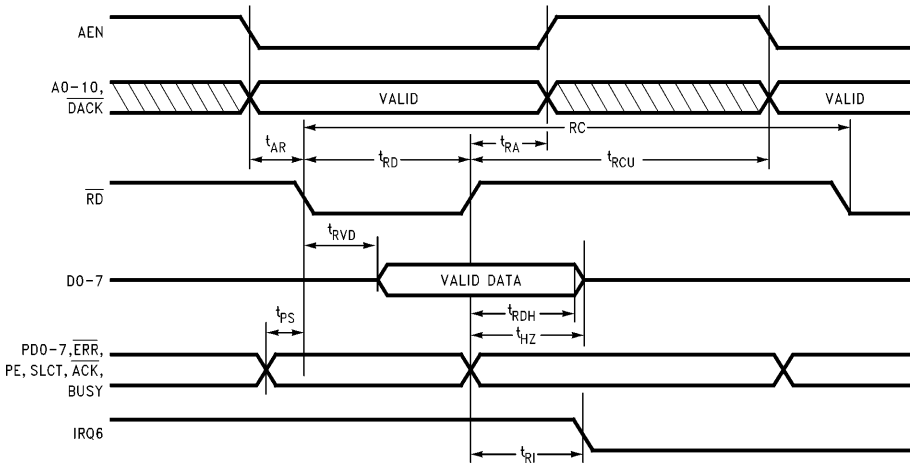
TL/C/11930–24

FIGURE 9-1. Clock Timing

9.0 Electrical Characteristics (Continued)

9.3.3 Microprocessor Interface Timing

Symbol	Parameter	Min	Max	Units
t_{AR}	Valid Address to Read Active	18		ns
t_{AW}	Valid Address to Write Active	18		ns
t_{DH}	Data Hold	0		ns
t_{DS}	Data Setup	18		ns
t_{HZ}	Read to Floating Data Bus	13	25	ns
t_{PS}	Port Setup	10		ns
t_{RA}	Address Hold from Inactive Read	0		ns
t_{RCU}	Read Cycle Update	45		ns
t_{RD}	Read Strobe Width	60		ns
t_{RDH}	Read Data Hold	10		ns
t_{RI}	Read Strobe to Clear IRQ6		55	ns
t_{RVD}	Active Read to Valid Data		55	ns
t_{WA}	Address Hold from Inactive Write	0		ns
t_{WCU}	Write Cycle Update	45		ns
t_{WI}	Write Strobe to Clear IRQ6		55	ns
t_{WO}	Write Data to Port Update		60	ns
t_{WR}	Write Strobe Width	60		ns
RC	Read Cycle $= t_{AR} + t_{RD} + t_{RCU}$	123		ns
WC	Write Cycle $= t_{AW} + t_{WR} + t_{WCU}$	123		ns



TL/C/11930–25

FIGURE 9-2. Microprocessor Read Timing

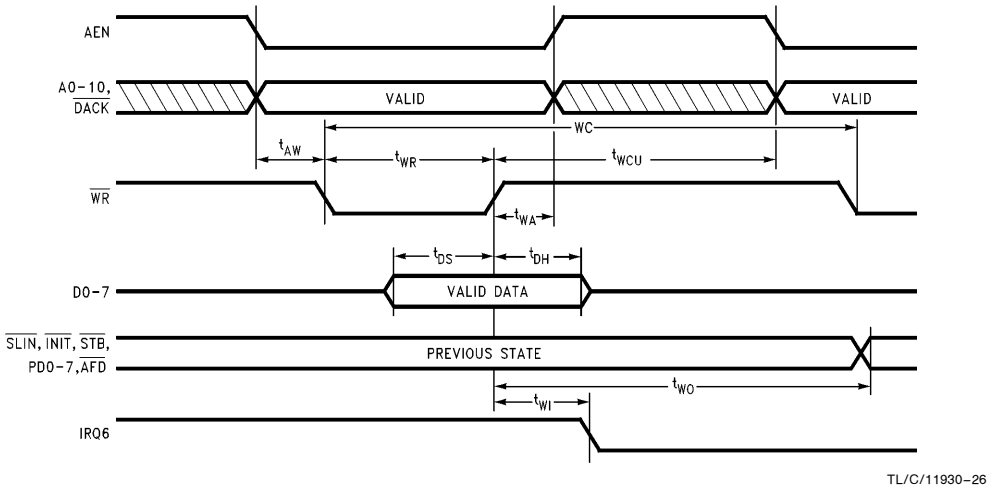


FIGURE 9-3. Microprocessor Write Timing

9.3.4 Baud Out Timing

Symbol	Parameter	Conditions	Min	Max	Units
N	Baud Divisor		1	65535	ns
t_{BHD}	Baud Output Positive Edge Delay	CLK = 24 MHz/2, 100 pF Load		56	ns
t_{BLD}	Baud Output Negative Edge Delay	CLK = 24 MHz/2, 100 pF Load		56	ns

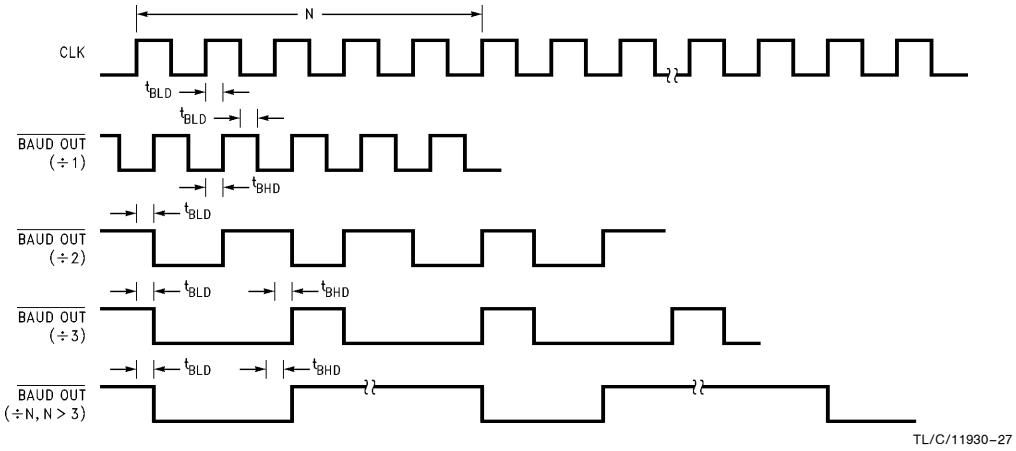
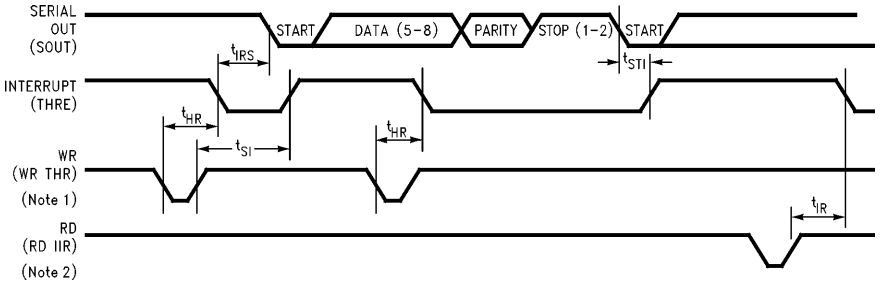


FIGURE 9-4. Baud Out Timing

9.0 Electrical Characteristics (Continued)

9.3.5 Transmitter Timing

Symbol	Parameter	Min	Max	Units
t_{HR}	Delay from $\overline{WR}$ (WR THR) to Reset IRQ		40	ns
t_{IR}	Delay from $\overline{RD}$ (RD IIR) to Reset IRQ (THRE)		55	ns
t_{IRS}	Delay from Initial IRQ Reset to Transmit Start	8	24	Baud Out Cycles
t_{SI}	Delay from Initial Write to IRQ	16	24	Baud Out Cycles
t_{STI}	Delay from Start Bit to IRQ (THRE)		8	Baud Out Cycles



TL/C/11930–28

Note 1: See Write cycle timing, *Figure 10-3.*

Note 2: See Read cycle timing, *Figure 10-2.*

FIGURE 9-5. Transmitter Timing

9.0 Electrical Characteristics (Continued)

9.3.6 Receiver Timing

Symbol	Parameter	Conditions	Min	Max	Units
t_{RAI}	Delay from Active Edge of $\overline{RD}$ to Reset IRQ			78	ns
t_{RINT}	Delay from Inactive Edge of $\overline{RD}$ (RD LSR) to Reset IRQ			55	ns
t_{SCD}	Delay from RCLK to Sample Time (Note 1)			41	ns
t_{SINT}	Delay from Stop Bit to Set Interrupt			2	Baud Out Cycles

Note 1: This is an internal timing and is therefore not tested.

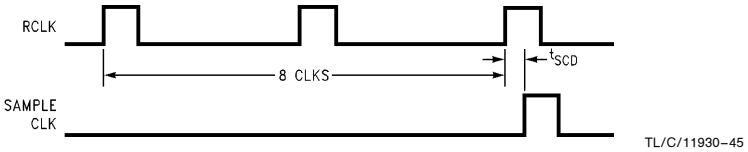


FIGURE 9-6a. Sample Clock Timing

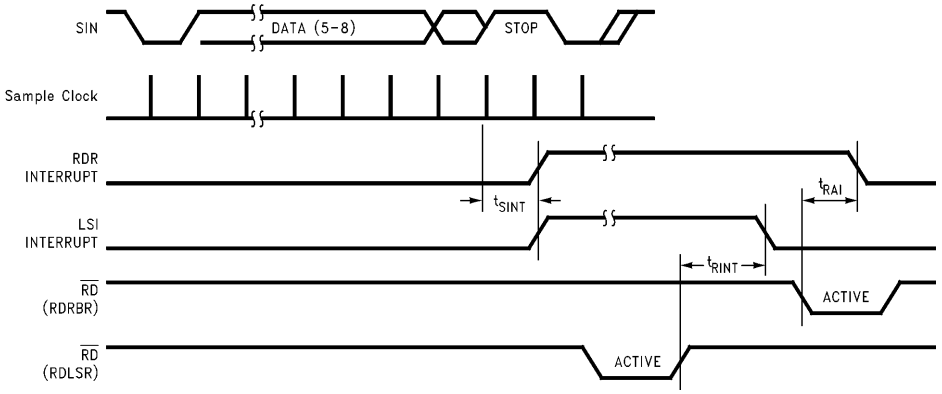
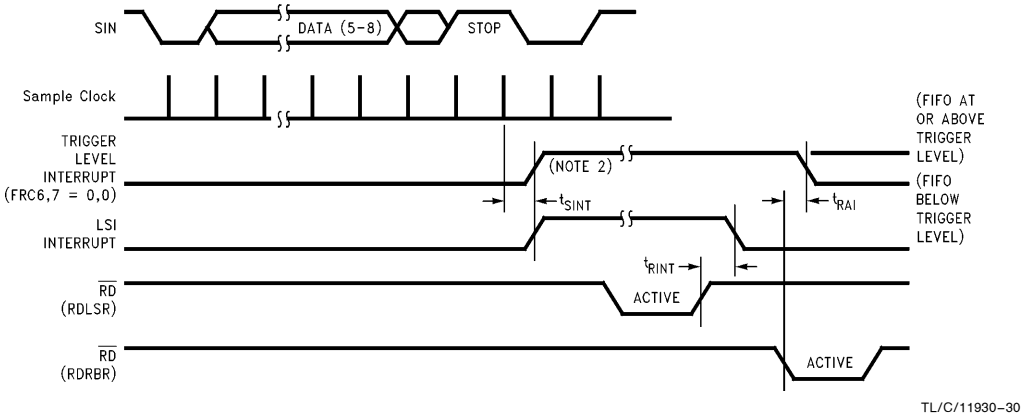
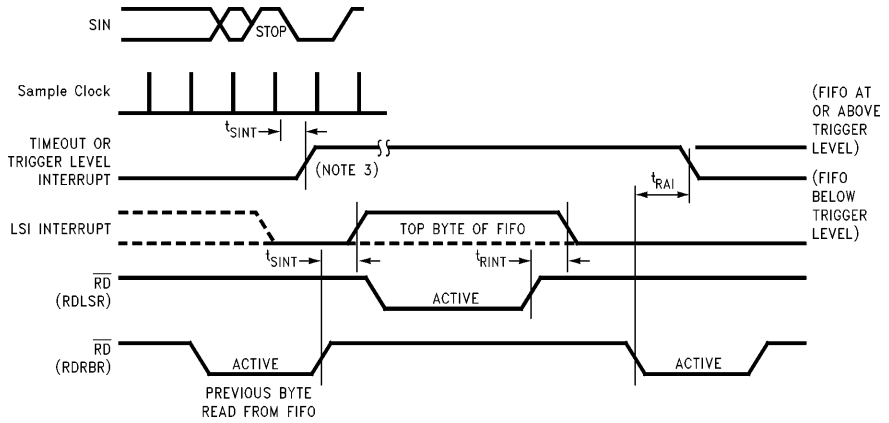


FIGURE 9-6b. Receiver Timing



Note 2: If SCR0 = 1, then t_{SINT} = 3 RCLKs. For a Timeout interrupt, t_{SINT} = 8 RCLKs.

FIGURE 9-6c. FIFO Mode Receiver Timing



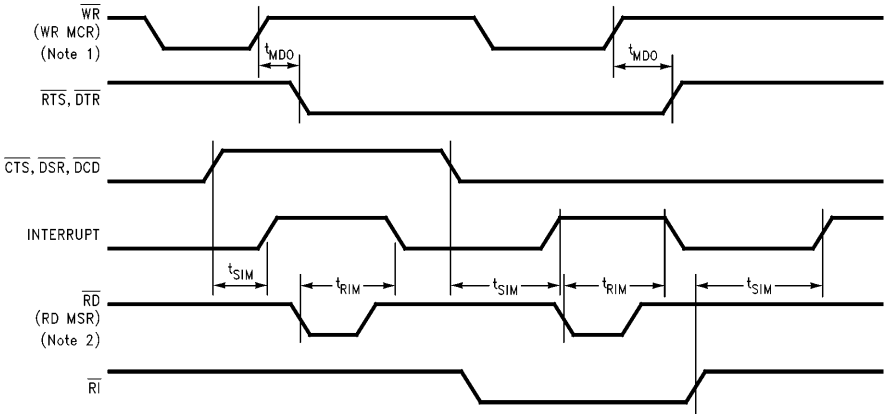
TL/C/11930–31

Note 3: If SCR0 = 1, then t_{SINT} = 3 RCLKs. For a Timeout interrupt, t_{SINT} = 8 RCLKs.

FIGURE 9-6d. Timeout Receiver Timing

9.3.7 MODEM Control Timing

Symbol	Parameter	Conditions	Min	Max	Units
t_{MDO}	Delay from $\overline{WR}$ (WR MCR) to Output			40	ns
t_{RIM}	Delay to Reset IRQ from $\overline{RD}$ (RD MSR)			78	ns
t_{SIM}	Delay to Set IRQ from MODEM Input			40	ns



TL/C/11930–32

Note 1: See Microprocessor Write cycle timing, *Figure 10-3*.

Note 2: See Microprocessor Read cycle timing, *Figure 10-2*.

FIGURE 9-7. MODEM Control Timing

9.0 Electrical Characteristics (Continued)

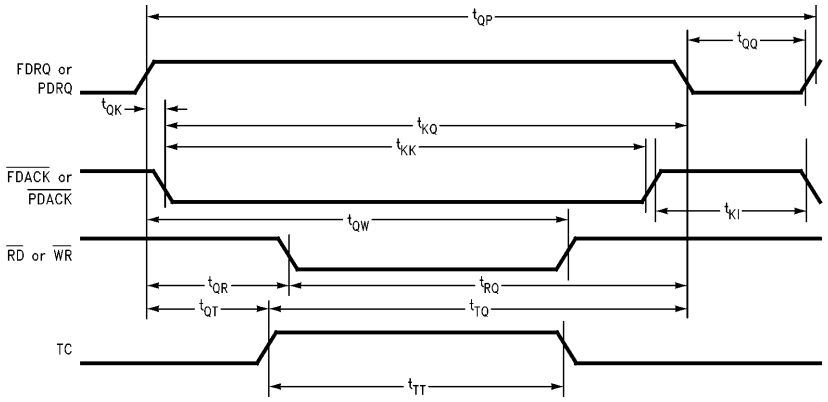
9.3.8 DMA Timing

Symbol	Parameter	Min	Max	Units
t_{KI}	$\overline{FDACK}$ or $\overline{PDACK}$ Inactive Pulse Width	25		ns
t_{KK}	$\overline{FDACK}$ or $\overline{PDACK}$ Active Pulse Width	65		ns
t_{KQ}	$\overline{FDACK}$ Active Edge to FDRQ Inactive (Note 1) $\overline{PDACK}$ Active Edge to PDRQ Inactive (Note 1)		65	ns
t_{QK}	FDRQ to $\overline{FDACK}$ Active Edge PDRQ to $\overline{PDACK}$ Active Edge	10		ns
t_{QP}	FDRQ Period (FDC-Burst DMA)	$8 \times t_{DRP}$		μs
	PDRQ Period (ECP)	330		μs
t_{QQ}	FDRQ or PDRQ Inactive Non-Burst Pulse Width	300	400	ns
t_{QR}	FDRQ to $\overline{RD}$ or $\overline{WR}$ Active PDRQ to $\overline{RD}$ or $\overline{WR}$ Active	15		ns
t_{QW}	FDRQ to End of $\overline{RD}$, $\overline{WR}$ (Note 1) (FDRQ Service Time)		$(8 \times t_{DRP}) - (16 \times t_{ICP})$	μs
t_{QT}	FDRQ to TC Active (Note 1) (FDRQ Service Time)		$(8 \times t_{DRP}) - (16 \times t_{ICP})$	μs
t_{RQ}	$\overline{RD}$, $\overline{WR}$ Active Edge to FDRQ or PDRQ Inactive (Note 2)		65	ns
t_{TQ}	TC Active Edge to FDRQ or PDRQ Inactive		75	ns
t_{TT}	TC Active Pulse Width	50		ns

Note 1: For FDC DMA: Values shown are with the FIFO disabled, or with FIFO enabled and THRESH = 0. For non-zero values of THRESH, add (THRESH $\times$ 8 $\times$ t_{DRP}) to the values shown.

For ECP DMA: Value shown is with the FIFO disabled. For FIFO enabled add (192 $\times$ T_{CP}) to the value shown (assuming IOCHRDY = 1).

Note 2: The active edge of $\overline{RD}$ or $\overline{WR}$ and TC is recognized only when $\overline{FDACK}$ or $\overline{PDACK}$ is active.



TL/C/11930–33

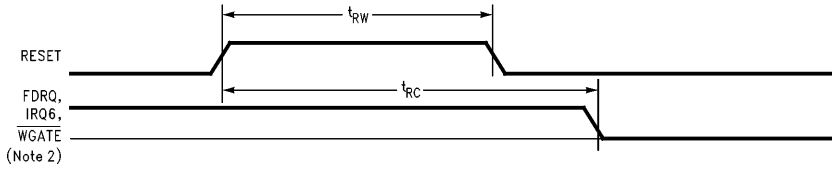
FIGURE 9-8. DMA Timing

9.0 Electrical Characteristics (Continued)

9.3.9 Reset Timing

Symbol	Parameter	Min	Max	Units
t_{RW}	Reset Width (Note 1)	22		μs
t_{RC}	Reset to Control Inactive		300	ns

Note 1: The FDC software reset pulse width is 100 ns.



TL/C/11930–34

Note 2: FDRQ and IRQ6 will be TRI-STATE after time t_{RC} when in the PC-AT or Model 30 mode.

FIGURE 9-9. Reset Timing

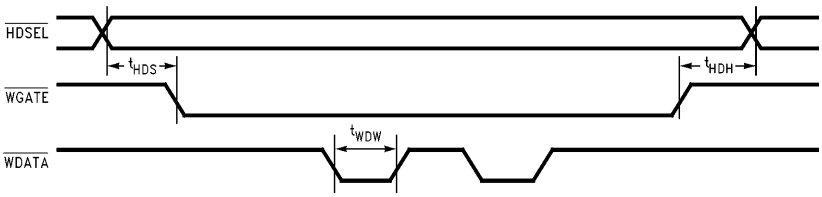
9.3.10 Write Data Timing

Symbol	Parameter	Min	Max	Units
t_{HDH}	$\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive	750		μs
t_{HDS}	$\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active	100		μs
t_{WDW}	Write Data Pulse Width	See Table 10-2		ns

TABLE 9-2. Minimum t_{WDW} Values

Data Rate	t_{DRP}	t_{WDW}	t_{WDW} Value	Units
1 Mbps	1000	$2 \times t_{ICP}$	250	ns
500 kbps	2000	$2 \times t_{ICP}$	250	ns
300 kbps	3333	$2 \times t_{ICP}$	375	ns
250 kbps	4000	$2 \times t_{ICP}$	500	ns

Note: See Section 10.3.2 for t_{ICP} description.



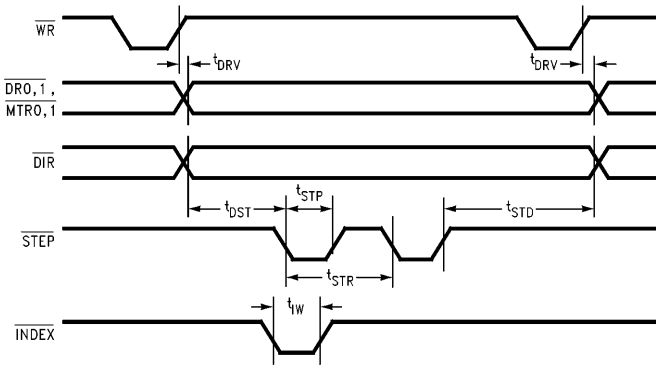
TL/C/11930–35

FIGURE 9-10. Write Data Timing

9.0 Electrical Characteristics (Continued)

9.3.11 Drive Control Timing

Symbol	Parameter	Min	Max	Units
t_{DRV}	$\overline{DR0}$–$\overline{DR3}$, $\overline{MTR0}$–$\overline{MTR3}$ from End of $\overline{WR}$		100	ns
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active	6		μs
t_{IW}	$\overline{INDEX}$ Pulse Width	100		ns
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		ms
t_{STP}	$\overline{STEP}$ Active High Pulse Width	8		μs
t_{STR}	$\overline{STEP}$ Rate Time (see Table 4-16)	1		ms

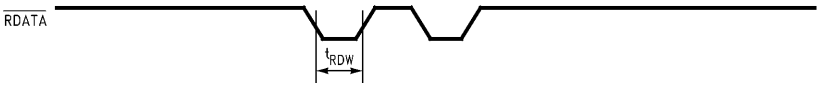


TL/C/11930–36

FIGURE 9-11. Drive Control Timing

9.3.12 Read Data Timing

Symbol	Parameter	Min	Max	Units
t_{RDW}	Read Data Pulse Width	50		ns

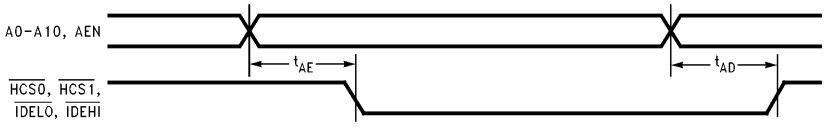


TL/C/11930–37

FIGURE 9-12. Read Data Timing

9.3.13 IDE Timing

Symbol	Parameter	Min	Max	Units
t_{AD}	Delay from Address to Disable Strobe		25	ns
t_{AE}	Delay from Address to Enable Strobe		25	ns



TL/C/11930–38

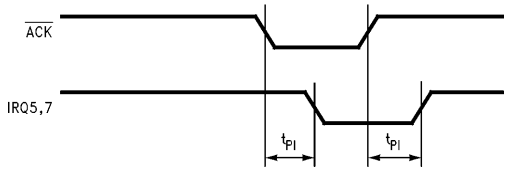
FIGURE 10-13. IDE Timing

9.0 Electrical Characteristics (Continued)

9.3.14 Parallel Port Timing

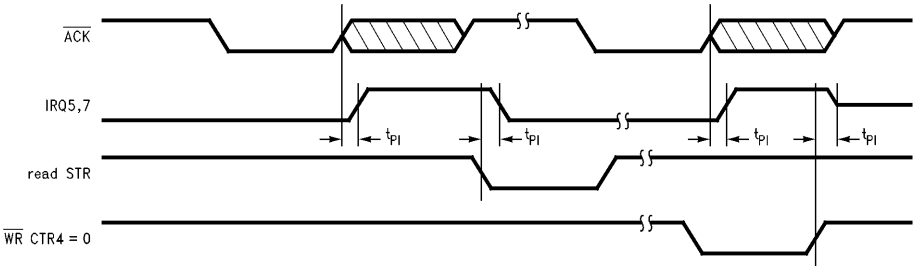
Symbol	Parameter	Conditions	Typ	Max	Units
t_{PDH}	Port Data Hold	(Note 1)	500		ns
t_{PDS}	Port Data Setup	(Note 1)	500		ns
t_{PI}	Port Interrupt			33	ns
t_{SW}	$\overline{STB}$ Width	(Note 1)	500		ns

Note 1: These times are system dependent and are therefore not tested.



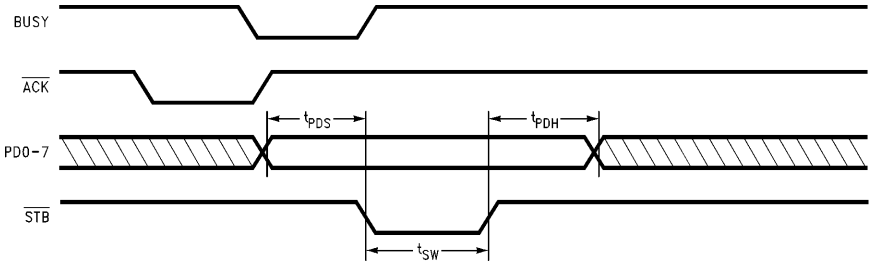
TL/C/11930–39

FIGURE 9-14. Compatible Mode Parallel Port Interrupt Timing



TL/C/11930–40

FIGURE 9-15. Extended Mode Parallel Port Interrupt Timing



TL/C/11930–41

FIGURE 9-16. Typical Parallel Port Data Exchange

9.0 Electrical Characteristics (Continued)

9.3.15 Enhanced Parallel Port Timing

Symbol	Parameter	Conditions	Min	Max	Units
t_{WW}	$\overline{WRITE}$ Active from $\overline{WR}$ Active (Note 1)			45	ns
t_{WST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WR}$ Active (Notes 1, 2)	EPP 1.7		45	ns
		EPP 1.9		65	ns
t_{WEST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active	EPP 1.7	0		ns
		EPP 1.9	10		ns
t_{WPDh}	PD0–7 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive		50		ns
t_{HRW}	IOCHRDY Active after $\overline{WAIT}$ Active (Note 3)	EPP 1.7		40	ns
t_{WPDS}	PD0–7 Valid after $\overline{WRITE}$ Active	D0–7 is Stable 15 ns before $\overline{WR}$ Active		15	ns
t_{EPDW}	PD0–7 Valid		80		ns
t_{EPDh}	PD0–7 Invalid after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive		0		ns
t_{ZWSa}	$\overline{ZWS}$ Valid after $\overline{WR}$ or $\overline{RD}$ Active			45	ns
t_{ZWSh}	$\overline{ZWS}$ Hold after $\overline{WR}$ or $\overline{RD}$ Inactive		0		ns

Note 1: t_{WST} and t_{WW} are valid in EPP 1.9 only if $\overline{WAIT}$ is low when $\overline{WR}$ becomes active, else t_{WST} and t_{WW} are measured from $\overline{WAIT}$.
Note 2: The PC87334 design guarantees that $\overline{WRITE}$ will not change from low to high before $\overline{DSTRB}$, or $\overline{ASTRB}$, goes from low to high.
Note 3: In EPP 1.9, IOCHRDY is measured from $\overline{WR}$ or $\overline{RD}$.

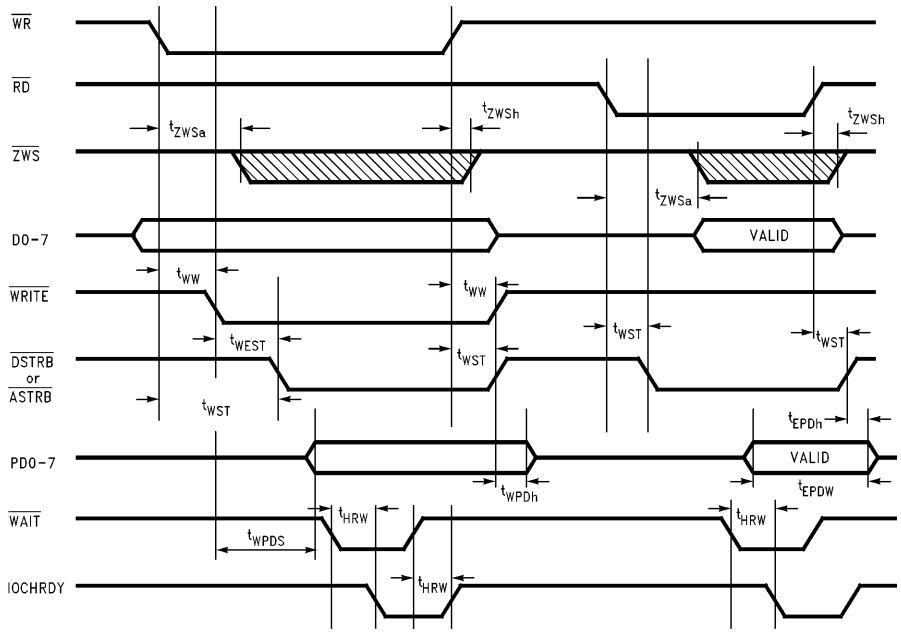
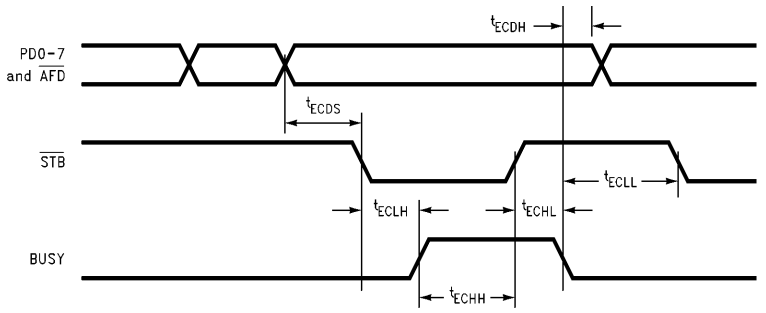


FIGURE 9-17. Enhanced Parallel Port Timing

9.0 Electrical Characteristics (Continued)

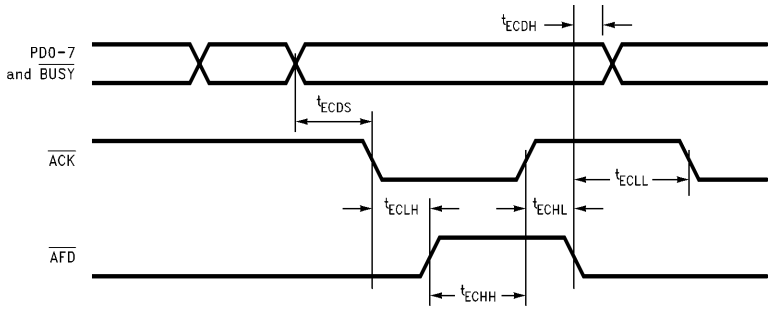
9.3.16 Extended Capabilities Parallel Port Timing

Symbol	Parameter	Conditions	Min	Max	Units
t_{ECDS}	Data Setup before $\overline{STB}$ Active		0		ns
t_{ECDH}	Data Hold after BUSY		0		ns
t_{ECLH}	BUSY Setup after $\overline{STB}$ Active		75		ns
t_{ECHH}	$\overline{STB}$ Active after BUSY		0	1	sec
t_{ECHL}	BUSY Setup after $\overline{STB}$ Inactive		0	35	ms
t_{ECLL}	$\overline{STB}$ Active after BUSY		0		ns



TL/C/11930–43

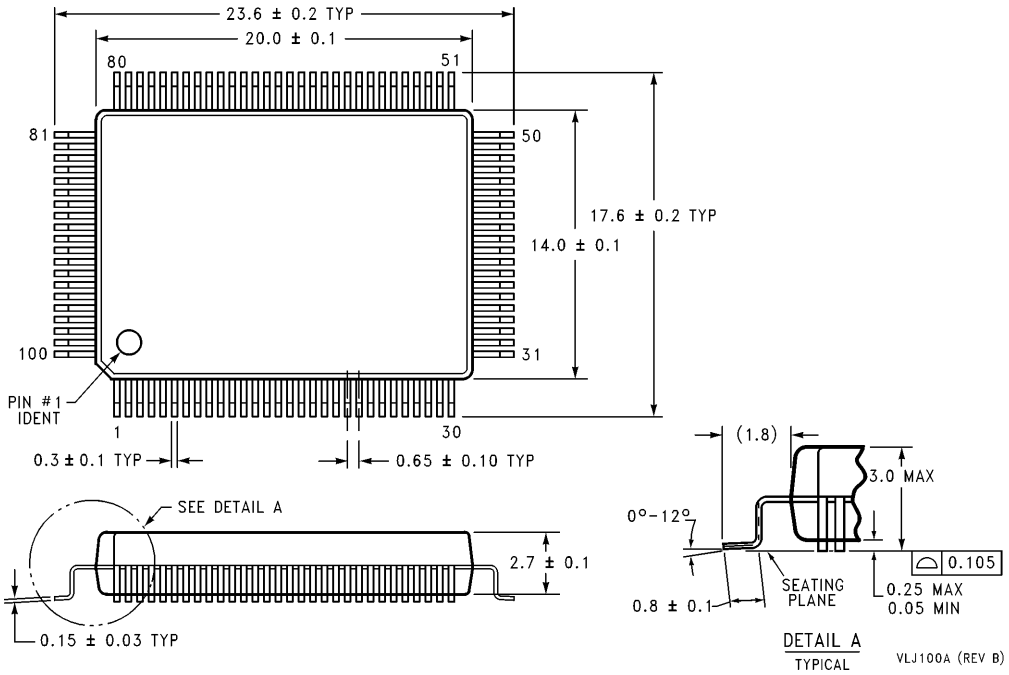
FIGURE 9-18. ECP Parallel Port Forward Timing Diagram



TL/C/11930–44

FIGURE 9-19. ECP Parallel Port Backward Timing Diagram

Physical Dimensions inches (millimeters) (Continued)



Plastic Quad Flatpak (EIAJ) (PQFP)
Order Number PC87332VLJ or PC87332VLJ-5
NS Package Number VLJ100A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.

National Semiconductor was acquired by Texas Instruments.

http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html

This file is the datasheet for the following electronic components:

PC87332VLJ - http://www.ti.com/product/pc87332vlj?HQS=TI-null-null-dscatalog-df-pf-null-wwe

PC87332VLJ-5 - http://www.ti.com/product/pc87332vlj-5?HQS=TI-null-null-dscatalog-df-pf-null-wwe