National Semiconductor

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PC16552D Dual Universal Asynchronous Receiver/Transmitter with FIFOs†

General Description

The PC16552D is a dual version of the PC16550D Universal Asynchronous Receiver/Transmitter (UART). The two serial channels are completely independent except for a common CPU interface and crystal input. On power-up both channels are functionally identical to the 16450*. Each channel can operate with on-chip transmitter and receiver FIFOs (FIFO mode) to relieve the CPU of excessive software overhead. In FIFO mode each channel is capable of buffering 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) of data in both the transmitter and receiver. All the FIFO control logic is on-chip to minimize system overhead and maximize system efficiency.

Signalling for DMA transfers is done through two pins per channel ($\overline{TXRDY}$ and $\overline{RXRDY}$). The $\overline{RXRDY}$ function is multiplexed on one pin with the $\overline{OUT\ 2}$ and BAUDOUT functions. The CPU can select these functions through a new register (Alternate Function Register).

Each channel performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of each channel at any time. Status information reported includes the type and condition of the transfer operations being performed by the DUART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The DUART includes one programmable baud rate generator for each channel. Each is capable of dividing the clock input by divisors of 1 to ($2^{16} - 1$), and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The DUART has complete MODEM-control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

The DUART is fabricated using National Semiconductor's advanced M^{2}CMOS™.

Features

- Dual independent UARTs
- Capable of running all existing 16450 and PC16550D software
- After reset, all registers are identical to the 16450 register set
- Read and write cycle times of 84 ns
- In the FIFO mode transmitter and receiver are each buffered with 16-byte FIFOs to reduce the number of interrupts presented to the CPU
- Holding and shift registers in the 16450 Mode eliminate the need for precise synchronization between the CPU and serial data
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generators divide any input clock by 1 to ($2^{16} - 1$) and generate the 16 × clock
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial-interface characteristics:
  - — 5-, 6-, 7-, or 8-bit characters
  - — Even, odd, or no-parity bit generation and detection
  - — 1-, 1½-, or 2-stop bit generation
  - — Baud generation (DC to 1.5M baud) with 16 × clock
- False start bit detection
- Complete status reporting capabilities
- TRI-STATE® TTL drive for the data and control buses
- Line break generation and detection
- Internal diagnostic capabilities:
  - — Loopback controls for communications link fault isolation
  - — Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls

*Can also be reset to 16450 Mode under software control.

†**Note: This part is patented.**

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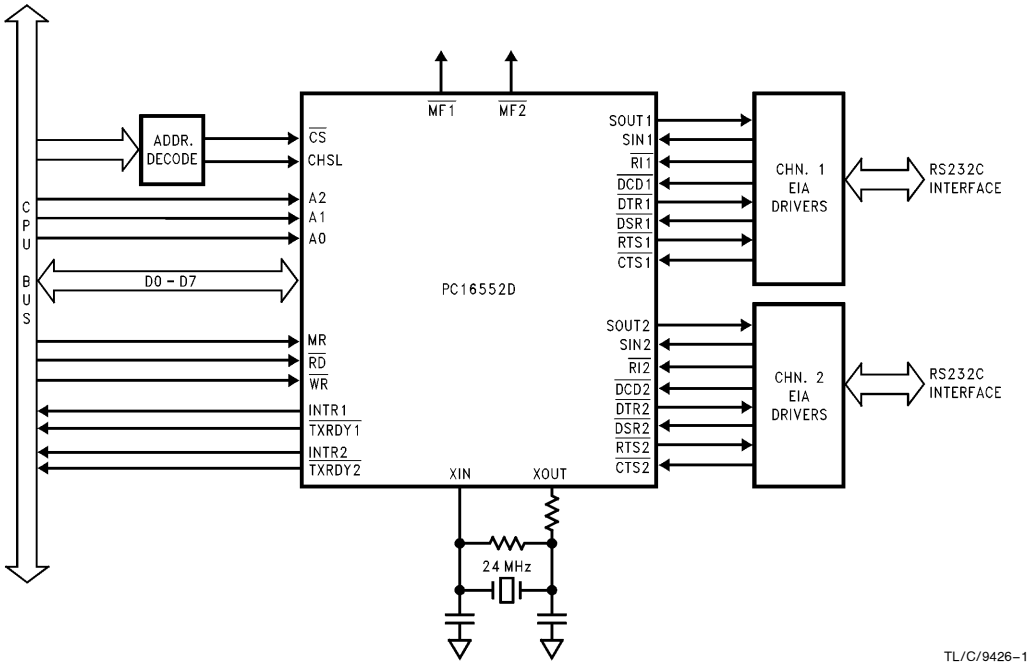
Basic Configuration



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1.0 Absolute Maximum Ratings

Temperature under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1W

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

2.0 DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ±10%, V_{SS} = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2	V_{CC}	V
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all (Note 1)		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA (Note 1)	2.4		V
I_{CC}(AV)	Average Power Supply Current	V_{DD} = 5.5V No Loads on Output; CS, RD, WR, SIN, DSR, DCD, CTS, RI = 2V All Other Inputs = 0.8V XIN = 24 MHz Divisor = EFFF		30	mA
I_{IL}	Input Leakage	V_{DD} = 5.5V, V_{SS} = 0V V_{IN} = 0V, 5.5V		±10	μA
I_{CL}	Clock Leakage			±10	μA
I_{OZ}	TRI-STATE Leakage	V_{DD} = 5.5V, V_{SS} = 0V V_{OUT} = 0V, 5.5V 1) Chip Deselected 2) WRITE Mode, Chip Selected		±20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2		V

Note 1: Does not apply to XOUT

Note 2: T_A = 25°C

Capacitance T_A = 25°C, V_{DD} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{XIN}	Clock Input Capacitance	f_c = 1 MHz Unmeasured Pins Returned to V_{SS}		7	9	pF
C_{XOUT}	Clock Output Capacitance			7	9	pF
C_{IN}	Input Capacitance			5	7	pF
C_{OUT}	Output Capacitance			6	8	pF
$C_{I/O}$	Input/Output Capacitance			10	12	pF

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Max	Units
t_{AR}	$\overline{RD}$ Delay from Address		15		ns
t_{AW}	$\overline{WR}$ Delay from Address		15		ns
t_{DH}	Data Hold Time		5		ns
t_{DS}	Data Setup Time		15		ns
t_{HZ}	$\overline{RD}$ to Floating Data Delay	(Note 2)	10	20	ns
t_{MR}	Master Reset Pulse Width		500		ns
t_{RA}	Address Hold Time from $\overline{RD}$		0		ns
t_{RC}	Read Cycle Update		29		ns
t_{RD}	$\overline{RD}$ Strobe Width		40		ns
t_{RVD}	Delay from $\overline{RD}$ to Data			25	ns
t_{WA}	Address Hold Time from $\overline{WR}$		0		ns
t_{WC}	Write Cycle Update		29		ns
t_{WR}	$\overline{WR}$ Strobe Width		40		ns
t_{XH}	Duration of Clock High Pulse	External Clock (24 MHz Max)	17		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (24 MHz Max)	17		ns
RC	Read Cycle $= t_{AR} + t_{RD} + t_{RC}$		84		ns
WC	Write Cycle $= t_{AW} + t_{WR} + t_{WC}$		84		ns
BAUD GENERATOR					
N	Baud Divisor		1	$2^{16} - 1$	
t_{BHD}	Baud Output Positive Edge Delay	$f_X = 24$ MHz, $\div 2$		45	ns
t_{BLD}	Baud Output Negative Edge Delay	$f_X = 24$ MHz, $\div 2$		45	ns
RECEIVER					
t_{RAI}	Delay from Active Edge of $\overline{RD}$ to Reset Interrupt			78	ns
t_{RINT}	Delay from Inactive Edge of $\overline{RD}$ (RD LSR) to Reset Interrupt			40	ns
t_{RXI}	Delay from READ to RXRDY Inactive			55	ns
t_{SCD}	Delay from RCLK to Sample Time			33	ns
t_{SINT}	Delay from Stop to Set Interrupt	(Note 1)		2	BAUDOUT Cycles

Note 1: In the FIFO mode (FCR0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

Note 2: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

Note 3: All AC timings can be met with current loads that don't exceed 3.2 mA or $-80\ \mu A$ at 100 pF capacitive loading.

Note 4: For capacitive loads that exceed 100 pF the following typical derating factors should be used:

$100\ pF < C_L \leq 150\ pF$ $t = (0.1\ ns/pF)(C_L - 100\ pF)$

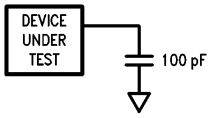
$150\ pF < C_L \leq 200\ pF$ $t = (0.08\ ns/pF)(C_L - 100\ pF)$

I_{SINK} $t = (0.5\ ns/mA)(I_{SINK}\ mA)$

I_{SOURCE} $t = (0.5\ ns/mA)(I_{SOURCE}\ mA)$

Limits: I_{SOURCE} is negative, $I_{SINK} \leq 4.8$ mA, $I_{SOURCE} \leq -120\ \mu A$, $C_L \leq 250$ pF

AC Testing Load Circuit



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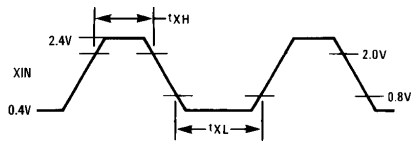
3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
TRANSMITTER					
t_{HR}	Delay from $\overline{WR}$ ($\overline{WR}$ THR) to Reset Interrupt			40	ns
t_{IR}	Delay from $\overline{RD}$ ($\overline{RD}$ IIR) to Reset Interrupt (THRE)			40	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt	(Note 1)	16	24	BAUDOUT Cycles
t_{STI}	Delay from Start to Interrupt (THRE)	(Note 1)		8	BAUDOUT Cycles
t_{SXA}	Delay from Start to TXRDY Active			8	BAUDOUT Cycles
t_{WXI}	Delay from Write to TXRDY Inactive			25	ns
MODEM CONTROL					
t_{MDO}	Delay from $\overline{WR}$ ($\overline{WR}$ MCR) to Output			40	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{RD}$ ($\overline{RD}$ MSR)			78	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input			40	ns

Note 1: This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active. (See FIFO Interrupt Mode Operation).

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1

External Clock Input (24 MHz Max)



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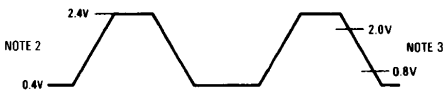
AC Test Points



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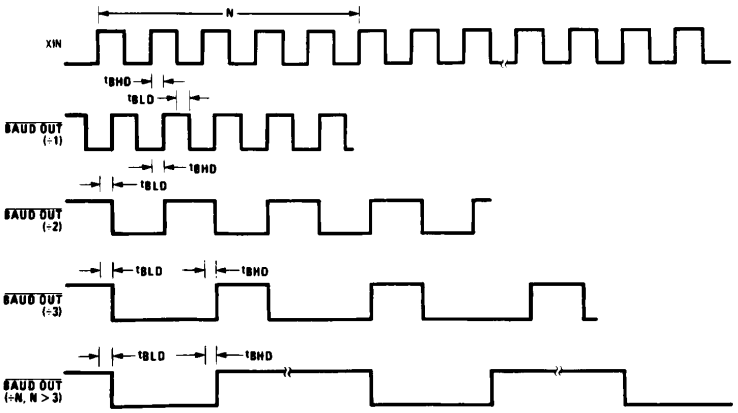
Note 2: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

Note 3: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

$\overline{BAUDOUT}$ Timing



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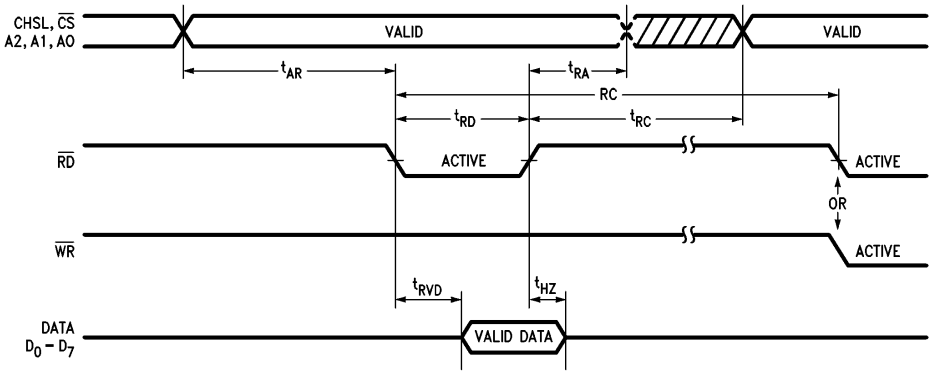
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

Read Cycle



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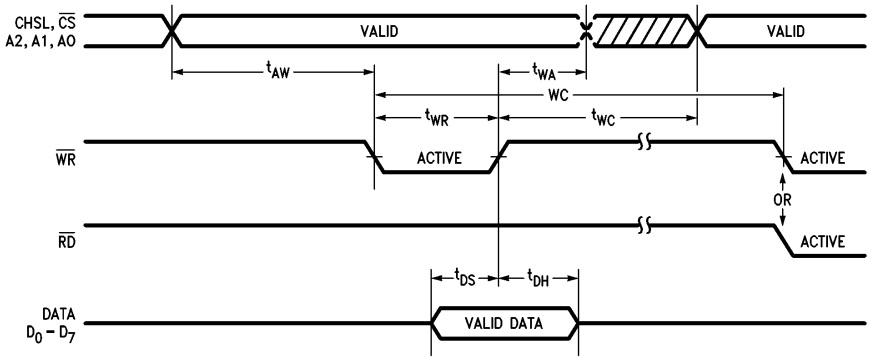
Write Cycle



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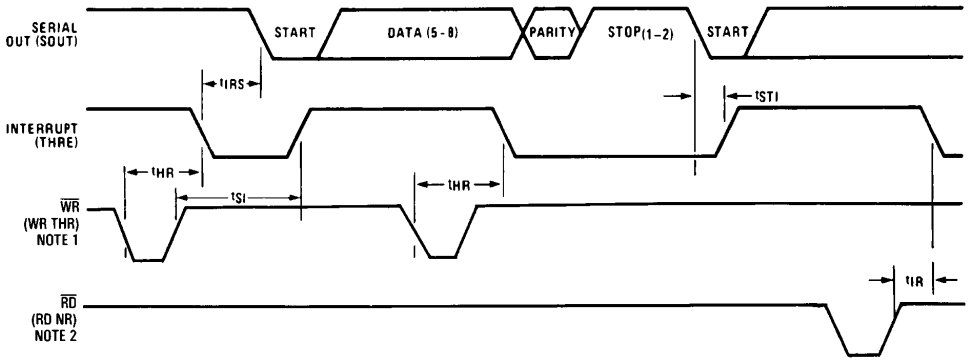
Transmitter Timing



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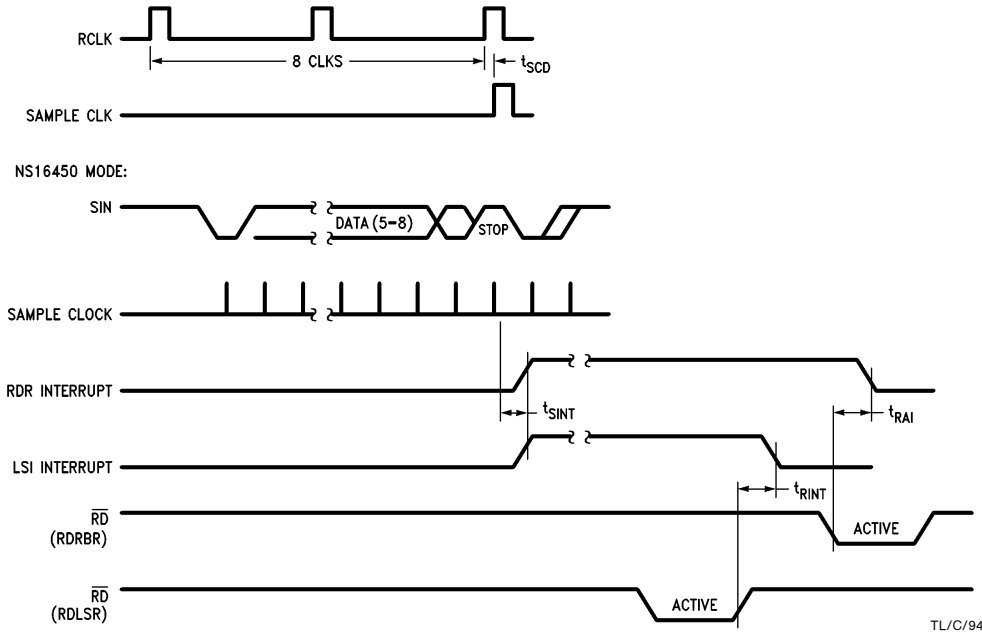
Note 1: See Write Cycle Timing.

Note 2: See Read Cycle Timing.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

Receiver Timing



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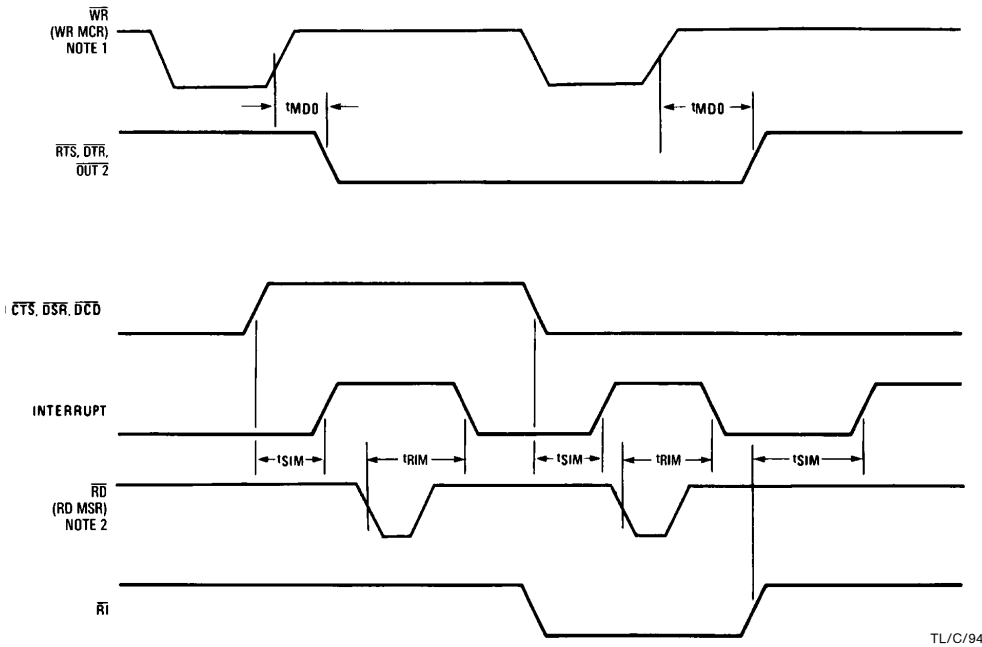
MODEM Control Timing



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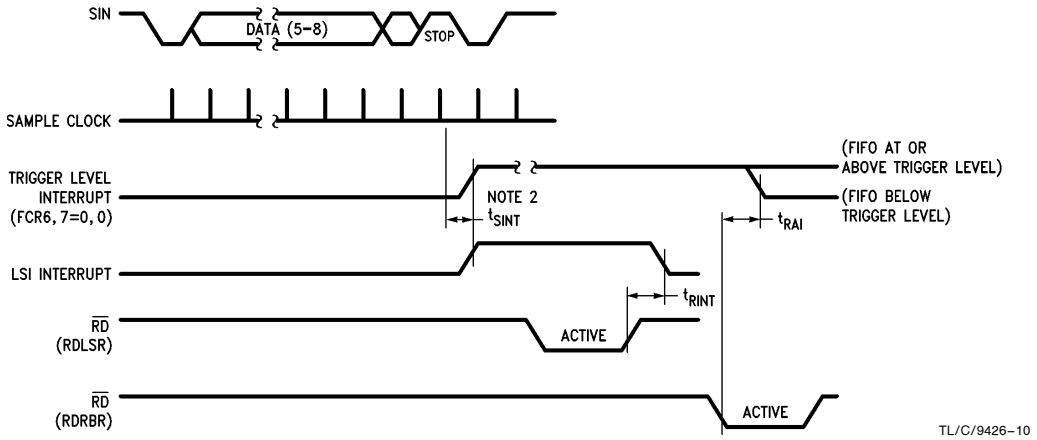
Note 1: See Write Cycle Timing.

Note 2: See Read Cycle Timing.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

RCVR FIFO First Byte (This Sets RDR)



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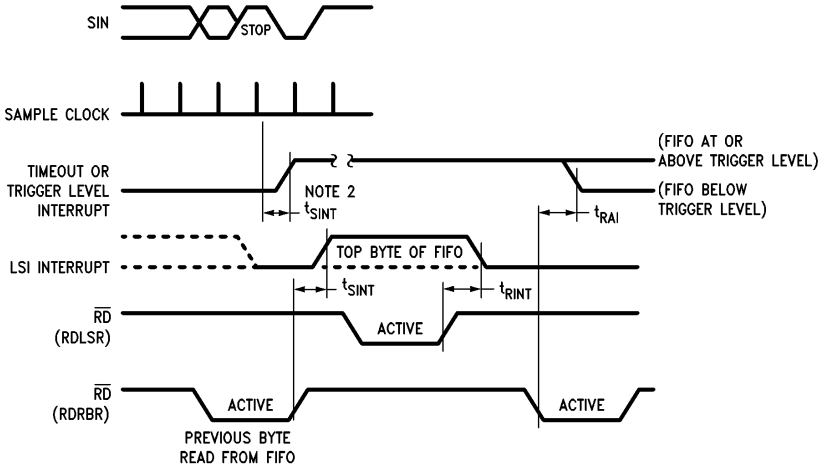
RCVR FIFO Bytes Other Than the First Byte (RDR Is Already Set)



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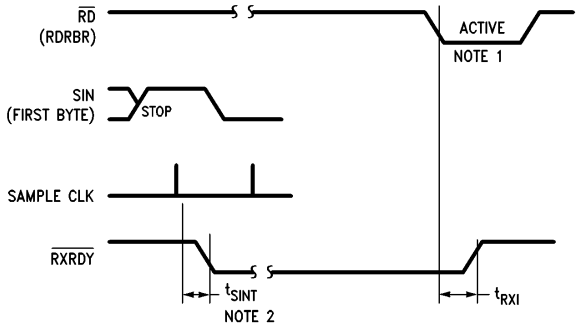
Receiver Ready FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



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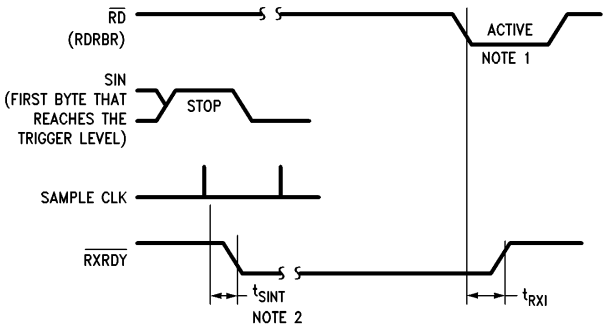
Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, then t_{SINT} = 3 RCLKs. For a timeout interrupt, t_{SINT} = 8 RCLKs.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

Receiver Ready FCR0 = 1 and FCR3 = 1 (Mode 1)



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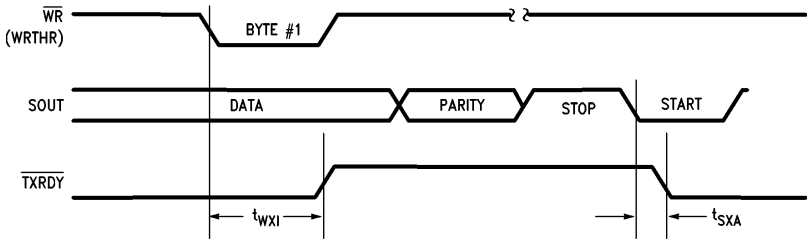
Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, t_{SINT} = 3 RCLKs.

Transmitter Ready FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



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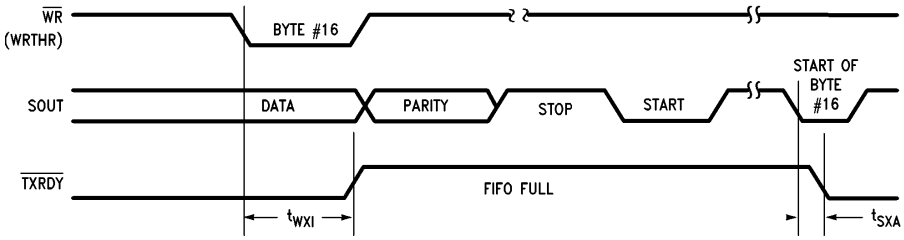
Transmitter Ready FCR0 = 1 and FCR3 = 1 (Mode 1)



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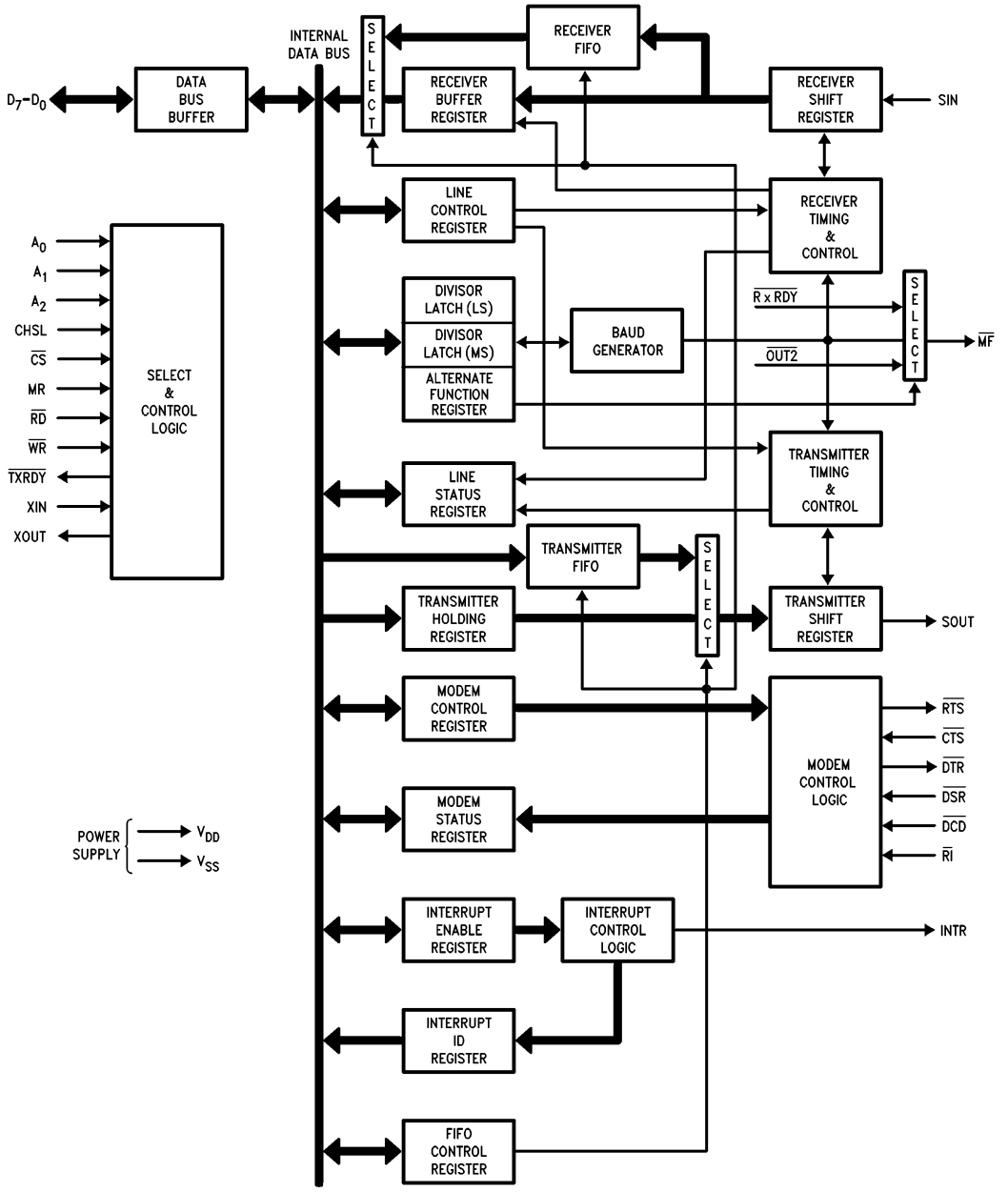
5.0 Block Diagram of a Single Channel



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6.0 Pin Descriptions

The following describes the function of all DUART pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Serial channels are designated by a numerical suffix (1 or 2) after each pin name. If a numerical suffix is **not** associated with the pin name, then the information applies to both channels.

A0, A1, A2 (Register Select), pins 10, 14, 15: Address signals connected to these 3 inputs select a DUART register for the CPU to read from or write to during data transfer. Table I shows the registers and their addresses. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain DUART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches and the Alternate Function Register.

CHSL (Channel Select), pin 16: This directs the address and data information to the selected serial channel. When CHSL is high, channel 1 is selected. When CHSL is low channel 2 is selected.

$\overline{\text{CS}}$ (Chip Select), pin 18: When $\overline{\text{CS}}$ is low, the chip is selected. This enables communication between the DUART and the CPU. Valid chip selects should stabilize according to the t_{AW} parameter.

$\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$ (Clear to Send), pins 40, 28: When low, this indicates that the MODEM or data set is ready to exchange data. The $\overline{\text{CTS}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 4 (CTS) of the MODEM Status Register for the appropriate channel. Bit 4 is the complement of the $\overline{\text{CTS}}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{\text{CTS}}$ has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

D_7–D_0 (Data Bus), pins 9–2: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D_7–D_0 Data Bus.

$\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$ (Data Carrier Detect), pins 42, 30: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{\text{DCD}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 7 (DCD) of the MODEM Status Register for the appropriate channel. Bit 7 is the complement of the $\overline{\text{DCD}}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{\text{DCD}}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{\text{DCD}}$ has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

$\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$ (Data Set Ready), pins 41, 29: When low, this indicates that the MODEM or data set is ready to establish the communications link with the DUART. The $\overline{\text{DSR}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 5 (DSR) of the MODEM Status Register for the appropriate channel. Bit 5 is the complement of the $\overline{\text{DSR}}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{\text{DSR}}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

$\overline{\text{DTR1}}$, $\overline{\text{DTR2}}$ (Data Terminal Ready), pins 37, 27: When low, this informs the MODEM or data set that the DUART is ready to establish a communications link. The $\overline{\text{DTR}}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

INTR1, INTR2 (Interrupt), pins 34, 17: This goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available: timeout (FIFO Mode only); Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

$\overline{\text{MF1}}$, $\overline{\text{MF2}}$ (Multi-Function), pins 35, 19: This can be programmed for any one of three signal functions $\overline{\text{OUT 2}}$, $\overline{\text{BAUDOUT}}$ or $\overline{\text{RXRDY}}$. Bits 2 and 1 of the Alternate Function Register select which output signal will be present on this pin. $\overline{\text{OUT 2}}$ is the default signal and it is selected immediately after master reset or power-up.

The $\overline{\text{OUT 2}}$ signal can be set active low by programming bit 3 (OUT 2) of the associated channel's MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop Mode holds this signal in its inactive state.

The $\overline{\text{BAUDOUT}}$ signal is the 16 × clock output that drives the transmitter and receiver logic of the associated serial channel. This signal is the result of the XIN clock divided by the value in the Division Latch Registers. The $\overline{\text{BAUDOUT}}$ signal for each channel is internally connected to provide the receiver clock (formerly RCLK on the PC16550D).

The $\overline{\text{RXRDY}}$ signal can be used to request a DMA transfer of data from the RCVR FIFO. Details regarding the active and inactive states of this signal are given in Section 8.5, Bit 3.

MR (Master Reset), pin 21: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the DUART. The states of various output signals (SOUT, INTR, $\overline{\text{OUT 2}}$, $\overline{\text{RTS}}$, $\overline{\text{DTR}}$) are affected by an active MR input (Refer to Table III.) This input is buffered with a TTL-compatible Schmitt Trigger.

$\overline{\text{RD}}$ (Read), pin 24: When $\overline{\text{RD}}$ is low while the chip is selected, the CPU can read status information or data from the selected DUART register.

$\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$ (Request to Send), pins 36, 23: When low, this informs the MODEM or data set that the UART is ready to exchange data. The $\overline{\text{RTS}}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

6.0 Pin Descriptions (Continued)

$\overline{RI1}$, $\overline{RI2}$ (Ring Indicator), pins 43, 31: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition the CPU can test by reading bit 6 (RI) of the MODEM Status Register for the appropriate channel. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input **signal** has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI **bit** of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

SIN1, SIN2 (Serial Input), pins 39, 25 : Serial data input from the communications link (peripheral device, MODEM, or data set).

SOUT1, SOUT2 (Serial Output), pins 38, 26: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

$\overline{TXRDY1}$, $\overline{TXRDY2}$ (Transmitter Ready), pins 1, 32: Transmitter DMA signalling is available through two pins. When operating in the FIFO mode, the CPU selects one of two types of DMA transfer via FCR3. When operating as in the 16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the XMIT FIFO has been filled. Details regarding the active and inactive states of this signal are given in Section 8.5, Bit 3.

V_{DD} (Power), pins 33, 44: +5V Supply

V_{SS} (Ground), pins 12, 22: 0V Reference

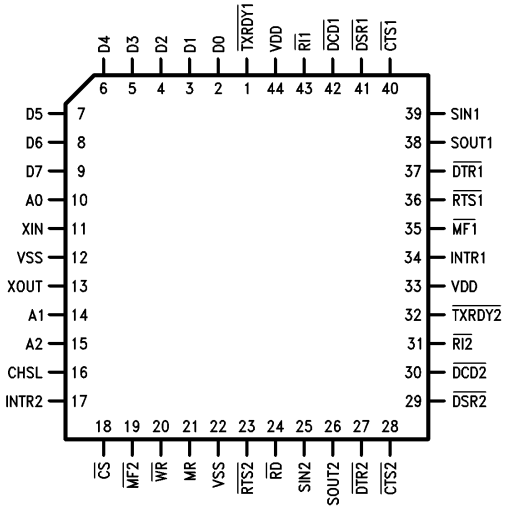
$\overline{WR}$ (Write), pin 20: When $\overline{WR}$ is low while the chip is selected, the CPU can write control words or data into the selected DUART register.

XIN (External Crystal Input), pin 11: This signal input is used in conjunction with XOUT to form a feedback circuit for the baud rate generator's oscillator. If a clock signal will be generated off-chip, then it should drive the baud rate generator through this pin.

XOUT (External Crystal Output), pin 13: This signal output is used in conjunction with XIN to form a feedback circuit for the baud rate generator's oscillator. If the clock signal will be generated off-chip, then this pin is unused.

7.0 Connection Diagram

Chip Carrier Package



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Top View

Order Number PC16552D
See NS Package Number V44A

8.0 Registers

TABLE I. Register Addresses

DLAB1	CHSL	A_2	A_1	A_0	Register	
0	1	0	0	0	Receiver Buffer (Read), Transmitter Holding Register (Write)	
0	1	0	0	1	Interrupt Enable	C
0	1	0	1	0	Interrupt Identification (Read)	H
0	1	0	1	0	FIFO Control (Write)	A
X	1	0	1	1	Line Control	N
X	1	1	0	0	MODEM Control	N
X	1	1	0	1	Line Status	E
X	1	1	1	0	MODEM Status	L
X	1	1	1	1	Scratch	
1	1	0	0	0	Divisor Latch (Least Significant Byte)	1
1	1	0	0	1	Divisor Latch (Most Significant Byte)	
1	1	0	1	0	Alternate Function	
DLAB2	**CHSL**	**A_2**	**A_1**	**A_0**	**Register**	
0	0	0	0	0	Receiver Buffer (Read), Transmitter Holding Register (Write)	
0	0	0	0	1	Interrupt Enable	C
0	0	0	1	0	Interrupt Identification (Read)	H
0	0	0	1	0	FIFO Control (Write)	A
X	0	0	1	1	Line Control	N
X	0	1	0	0	MODEM Control	N
X	0	1	0	1	Line Status	E
X	0	1	1	0	MODEM Status	L
X	0	1	1	1	Scratch	
1	0	0	0	0	Divisor Latch (Least Significant Byte)	2
1	0	0	0	1	Divisor Latch (Most Significant Byte)	
1	0	0	1	0	Alternate Function	

TABLE II. Register Summary for an Individual Channel

Bit No.	Register Address												
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1	2 DLAB = 1
	Receiver Buffer Register (Read Only)	**Transmitter Holding Register (Write Only)**	**Interrupt Enable Register**	**Interrupt Ident. Register (Read Only)**	**FIFO Control Register (Write Only)**	**Line Control Register**	**MODEM Control Register**	**Line Status Register**	**MODEM Status Register**	**Scratch Reg-ister**	**Divisor Latch (LS)**	**Divisor Latch (MS)**	**Alternate Function Register**
	RBR	**THR**	**IER**	**IIR**	**FCR**	**LCR**	**MCR**	**LSR**	**MSR**	**SCR**	**DLL**	**DLM**	**AFR**
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERDAI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8	Concurrent Write
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Interrupt ID Bit	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9	$\overline{\text{BAUDOUT}}$ Select
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1 (Note 3)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10	$\overline{\text{RXRDY}}$ Select
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EMSI)	Interrupt ID Bit (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11	0
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12	0
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13	0
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14	0
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15	0

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the 16450 Mode.

Note 3: This bit no longer has a pin associated with it.

8.0 Registers (Continued)

Two identical register sets, one for each channel, are in the DUART. All register descriptions in this section apply to the register sets in both channels.

8.1 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). This is a read and write register. Table II shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of data bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Data Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted with each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit data length is selected, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.

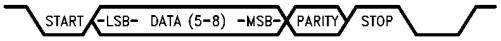
Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When parity is enabled and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When parity is enabled and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1 (Mark Parity). If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing state (logic 0). The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Composite Serial Data



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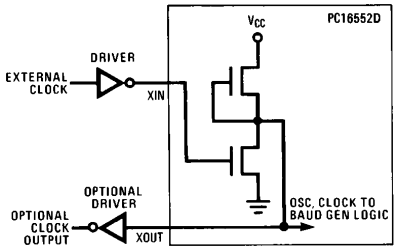
Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

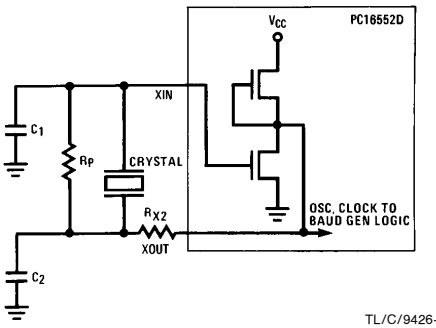
During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator or the Alternate Function Register during a Read or Write operation. It must be set low (logic 0) to access any other register.

8.2 TYPICAL CLOCK CIRCUITS



TL/C/9426–18



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Typical Crystal Oscillator Network (Note)

Crystal	R_P	R_{X2}	C_1	C_2
3.1 MHz	1 MΩ	1.5k	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5k	10–30 pF	40–60 pF

Note: These R and C values are approximate and may vary 2 x depending on the crystal characteristics. All crystal circuits should be designed specifically for the system.

8.0 Registers (Continued)

TABLE III. DUART Reset Configuration

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification Register	Master Reset	00**00** 0001
FIFO Control	Master Reset	00**00** 0000
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**0000** 0000
Line Status Register	Master Reset	0110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
Alternate Function Register	Master Reset	000**0 0000**
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
RCVR FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low
XMIT FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low

Note 1: Boldface bits are permanently low.

Note 2: Bits 7–4 are driven by the input signals.

8.3 PROGRAMMABLE BAUD GENERATOR

The DUART contains two independently programmable Baud Generators. Each is capable of taking a common clock input from DC to 24.0 MHz and dividing it by any divisor from 1 to $2^{16} - 1$. The highest input clock frequency recommended with a divisor = 1 is 24 MHz. The output frequency of the Baud Generator is 16 × the baud rate, [divisor # = (frequency input) ÷ (baud rate × 16)]. The output of each Baud Generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded.

Table IV provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 18.432 MHz. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is **not** recommended.

8.4 LINE STATUS REGISTER

This register provides status information to the CPU concerning the data transfer. Table II shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that the next character received was transferred into the Receiver Buffer Register before the CPU could read the previously received character. This transfer destroys the previous character. The OE indicator is set to a logic 1 during the character stop bit time when the overrun condition exists. It is reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register can be overwritten, but it is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 during the character Stop bit time when the character has a parity error. It is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register or when the next character is loaded into the Receiver Buffer Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. The FE bit is set to a logic 1 when the serial channel detects a logic 0 during the first Stop bit time. The FE indicator is reset whenever the CPU reads the contents of the Line Status Register or when the next character is loaded into the Receiver Buffer Register. In the FIFO Mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The serial channel will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this ''start'' bit twice and then takes in the ''data''.

8.0 Registers (Continued)

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register or when the next valid character is loaded into the Receiver Buffer Register. In the FIFO Mode this condition is associated with the particular character in the FIFO it applies to. It is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. In the 16450 mode bit 5 indicates that the associated serial channel is ready to accept a new character for transmission. In addition, this bit causes the DUART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the 16450 Mode this is a 0. In the FIFO Mode LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing. In the FIFO mode the user must load a data byte into the Rx FIFO in order to write to LSR2–4. LSR0 and LSR7 cannot be written to in the FIFO mode.

8.5 FIFO CONTROL REGISTER

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs.

When changing from FIFO Mode to 16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Writing a 1 to FCR3 causes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ operations to change from mode 0 to mode 1 if FCR0 = 1.

RXRDY Mode 0: When in the 16450 Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 0) and there is at least 1 character in the RCVR FIFO or RCVR Buffer Register, the $\overline{\text{RXRDY}}$ pin will go low active. Once active the $\overline{\text{RXRDY}}$ pin will go inactive when there are no more characters in the FIFO or Buffer Register.

TABLE IV. Baud Rates, Divisors and Crystals

Baud Rate	1.8432 MHz Crystal		3.072 MHz Crystal		18.432 MHz Crystal	
	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error
50	2304	—	3840	—	23040	—
75	1536	—	2560	—	15360	—
110	1047	0.026	1745	0.026	10473	—
134.5	857	0.058	1428	0.034	8565	—
150	768	—	1280	—	7680	—
300	384	—	640	—	3840	—
600	192	—	320	—	1920	—
1200	96	—	160	—	920	—
1800	64	—	107	0.312	640	—
2000	58	0.69	96	—	576	—
2400	48	—	80	—	480	—
3600	32	—	53	0.628	320	—
4800	24	—	40	—	240	—
7200	16	—	27	1.23	160	—
9600	12	—	20	—	120	—
19200	6	—	10	—	60	—
38400	3	—	5	—	30	—
56000	2	2.86	—	—	21	2.04
128000	—	—	—	—	9	—

Note: For baud rates of 250k, 300k, 375k, 500k, 750k and 1.5M using a 24 MHz crystal causes minimal error.

8.0 Registers (Continued)

RXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when the FCR3 = 1 and the trigger level or the timeout has been reached, the $\overline{\text{RXRDY}}$ pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO.

TXRDY Mode 0: In the 16450 Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 0) when there are no characters in the XMIT FIFO or XMIT Holding Register, the $\overline{\text{TXRDY}}$ pin will go low active. Once active the $\overline{\text{TXRDY}}$ pin will go inactive after the first character is loaded into the XMIT FIFO or Holding Register.

TXRDY Mode 1: In the FIFO Mode (FCR0 = 1, FCR3 = 1) and when there are no characters in the XMIT FIFO, the $\overline{\text{TXRDY}}$ pin will go low active. This pin will become inactive when the XMIT FIFO is completely full.

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to designate the interrupt trigger level. When the number of bytes in the RCVR FIFO equals the designated interrupt trigger level, a Received Data Available Interrupt is activated. This interrupt must be enabled by setting IER0.

FCR Bits 7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

8.6 INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, each serial channel of the DUART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU reads the IIR, the associated DUART serial channel freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the associated DUART serial channel records new interrupts, but does not change its current indication until the access is complete. Table II shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR identify the highest priority interrupt pending from those shown in Table V.

Bit 3: In the 16450 Mode this bit is 0. In the FIFO Mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5: These two bits of the IIR are always logic 0.

Bits 6 and 7: These two bits are set when FCR0 = 1. (FIFO Mode enabled.)

TABLE V. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed from or Input to the RCVR FIFO During the Last 4 Char. Times and There is at Least 1 Char. in it During This Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

8.0 Registers (Continued)

8.7 INTERRUPT ENABLE REGISTER

This register enables five types of interrupts for the associated serial channel. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table II shows the contents of the IER. Details on each bit follow:

Bit 0: When set to logic 1 this bit enables the Received Data Available Interrupt and Timeout Interrupt in the FIFO Mode.

Bit 1: When set to logic 1 this bit enables the Transmitter Holding Register Empty Interrupt.

Bit 2: When set to logic 1 this bit enables the Receiver Line Status Interrupt.

Bit 3: When set to logic 1 this bit enables the MODEM Status Interrupt.

Bits 4 through 7: These four bits are always logic 0.

8.8 MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described below:

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit is the $\overline{OUT\ 1}$ bit. It does **not** have an output pin associated with it. It can be written to and read by the CPU. In Local Loopback Mode this bit controls bit 2 of the Modem Status Register.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ pin in a manner identical to that described above for bit 0.

The function of this bit is multiplexed on a single output pin with two other functions: $\overline{BAUDOUT}$ and $\overline{RXRDY}$. The $\overline{OUT\ 2}$ function is the default function of the pin after a master reset. See Section 8.10 for more information about selecting one of these 3 pin functions.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the associated serial channel. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is ''looped back'' into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs; and the MODEM Control output pins are forced to their inactive state (high). In this diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify transmit and receive data paths of the DUART.

In this diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

8.9 MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. The latter bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table II and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

8.10 ALTERNATE FUNCTION REGISTER

This is a read/write register used to select specific modes of operation. It is located at address 010 when the DLAB bit is set.

Bit 0: When this bit is set the CPU can write concurrently to the same register in both register sets. This function is intended to reduce the DUART initialization time. It can be used by a CPU when both channels are initialized to the same state. The CPU can set or clear this bit by accessing either register set. When this bit is set the channel select pin still selects the channel to be accessed during read operations. Setting or clearing this bit has **no** effect on read operations.

The user should ensure that the DLAB bit (LCR7) of both channels are in the same state before executing a concurrent write to register addresses 0, 1 and 2.

8.0 Registers (Continued)

Bits 1 and 2: These select the output signal that will be present on the multi-function pin, $\overline{MF}$. These bits are individually programmable for each channel, so that different signals can be selected on each channel. Table VI associates the signal present at the multi-function pin with the bit code.

TABLE VI

AFR Bit Code Bit 2	Bit 1		Multi-Function Pin Signal	
0	0	(Note 1)	$\overline{OUT\ 2}$	
0	1		$\overline{BAUDOUT}$	
1	0		$\overline{RXRDY}$	
1	1		Reserved	(Note 2)

Note 1: This is the state after power-up or master reset.

Note 2: Output is forced high.

Bits 3 through 7: These bits are permanently set to a logic 0.

8.11 SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the serial channel in any way. It is intended as a Scratchpad Register to be used by the programmer to hold data temporarily.

9.0 FIFO Mode Operation

Each serial channel has two 16-byte FIFOs associated with it. The operational description that follows is applicable to the FIFOs of both channels.

9.1 FIFO INTERRUPT OPERATION

When the RCVR FIFO and receiver interrupt are enabled (FCR0 = 1, IER0 = 1) Receive Data Available Interrupts will occur as follows:

A. The Receive Data Available Interrupt will be issued to the CPU when the number of bytes in the RCVR FIFO equals the programmed trigger level; it will be cleared as soon as the number of bytes in the RCVR FIFO drops below its programmed trigger level.

B. The IIR Receive Data Available Indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The Receiver Line Status Interrupt (IIR = 06), as before, has higher priority than the Received Data Available (IIR = 04) Interrupt.

D. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the RCVR FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A RCVR FIFO Timeout Interrupt will occur, if the following conditions exist:

— at least one character is in the RCVR FIFO

— the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).

— the most recent CPU read of the RCVR FIFO was longer than 4 continuous character times ago.

The maximum time between a received character and a timeout interrupt will be 160 ms at 300 baud with a 12-bit receive character (i.e. 1 START, 8 DATA, 1 PARITY and 2 STOP BITS).

B. Character times are calculated by using the $\overline{BAUDOUT}$ signal as a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When the timeout interrupt indication is inactive the timeout indication timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO interrupts are enabled (FCR0 = 1, IER1 = 1), XMIT interrupts will occur as follows:

A. The Transmitter Holding Register Empty Interrupt occurs when the XMIT FIFO is empty. It is cleared as soon as the Transmitter Holding Register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last Stop bit time whenever the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE = 1. The first Transmitter Holding Register Empty Interrupt after changing FCR0 will be immediate, if it is enabled.

This delay prevents the DUART from issuing a second Transmitter Holding Register Empty Interrupt as soon as it transfers the first character into the Transmitter Shift Register.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO Empty has the same priority as the current Transmitter Holding Register Empty Interrupt.

9.2 FIFO POLLED OPERATION

With FCR0 = 1 resetting IER0, IER1, IER2, IER3 or all to zero puts the associated serial channel in the FIFO Polled Mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check receiver and transmitter status via the LSR. As stated in Section 8.4:

LSR0 will be set as long as there is one byte in the RCVR FIFO.

LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as in the interrupt mode.

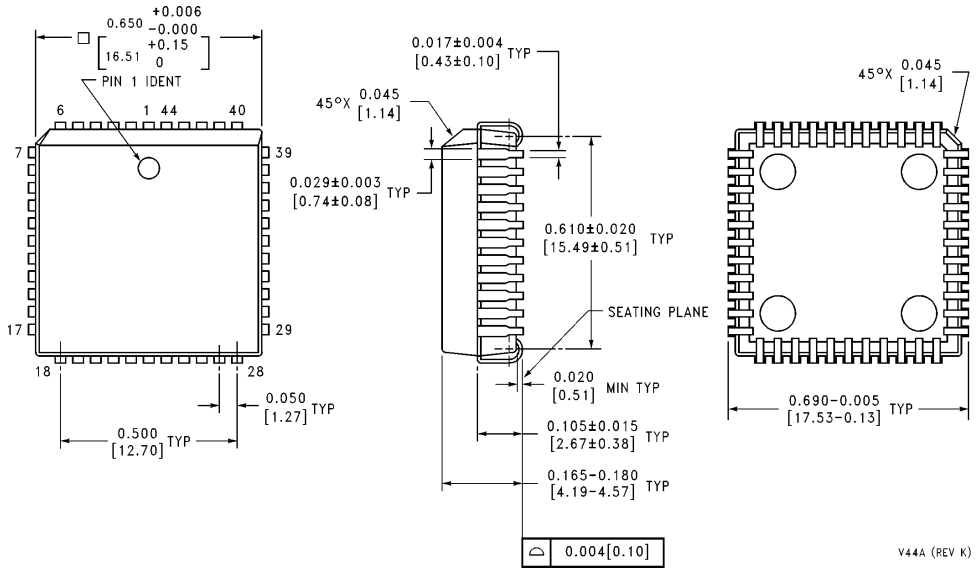
LSR5 will indicate when the XMIT FIFO is empty.

LSR6 will indicate that both the XMIT FIFO and shift register are empty.

LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are otherwise functional.

Physical Dimensions inches (millimeters)



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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

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