ML6698*

100BASE-TX Physical Layer with 5-Bit Interface

GENERAL DESCRIPTION

The ML6698 is a high-speed physical layer transceiver that provides a 5-bit (or symbol) interface to unshielded twisted pair cable media. The ML6698 is well suited for adapter card applications using the DEC 21143, the Macronix MX98713, or equivalent Media Access Controllers (MACs). The ML6698 may be used in other 100BASE-TX applications requiring the 5-bit interface as well as FDDI-over-copper applications.

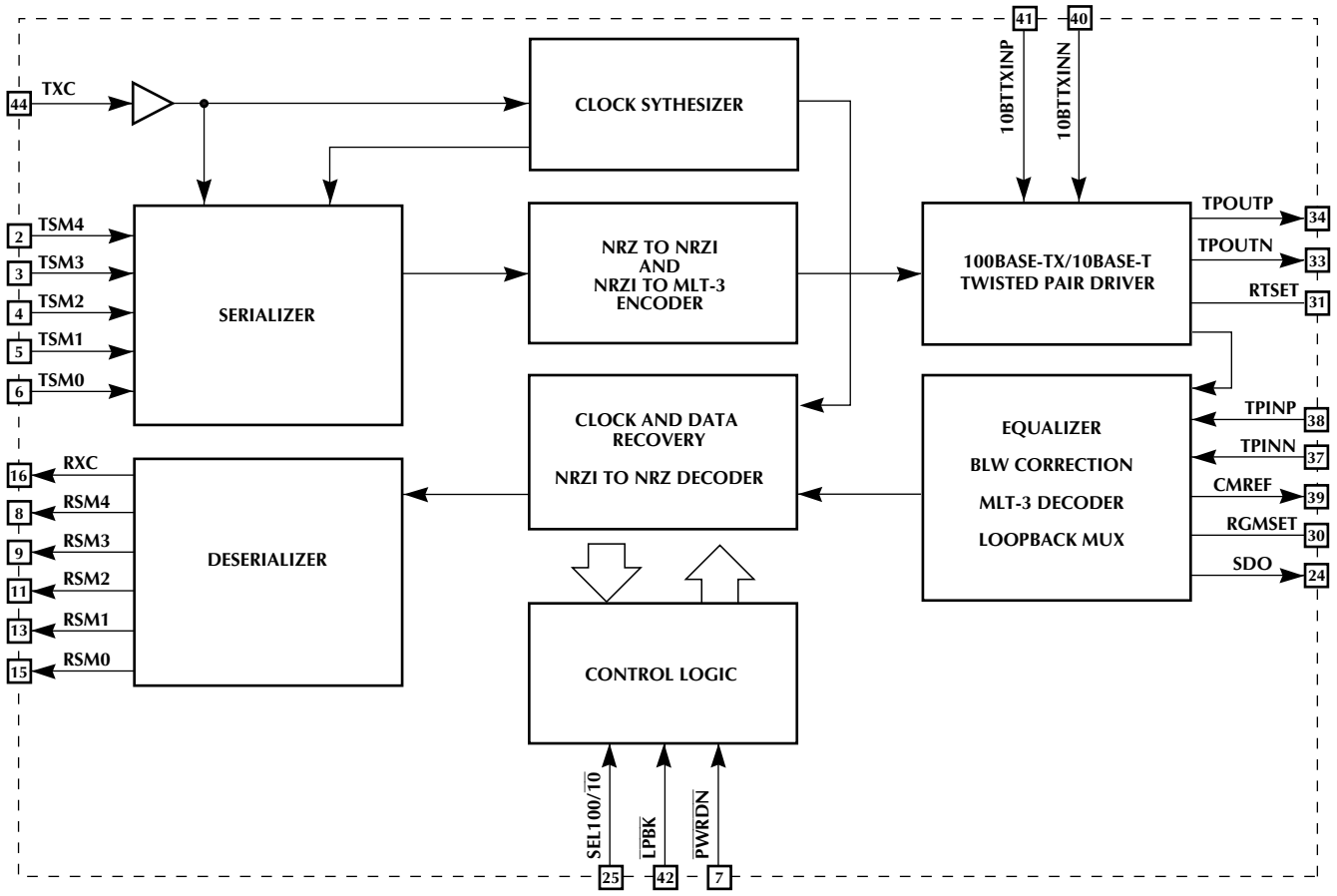
The ML6698 integrates 125MHz clock recovery/ generation, receive adaptive equalization, baseline wander correction and MLT-3/10BASE-T transmitter.

FEATURES

- 5-bit (or symbol) parallel interface
- Compliant to IEEE 802.3u 100BASE-TX standard
- Compliant to ANSI X3T12 TP-PMD (FDDI) standard
- Single-jack 10BASE-T/100BASE-TX solution when used with external 10Mbps PHY
- 125MHz receive clock recovery/generation
- Baseline wander correction
- Adaptive equalization and MLT-3 encoding/decoding
- Supports full-duplex operation

*Some Packages Are End Of Life As Of August 1, 2000

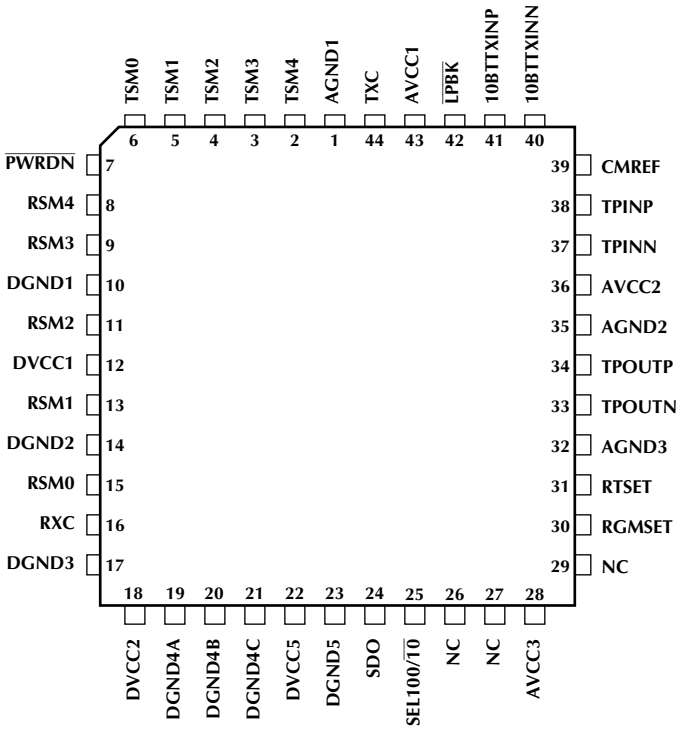
BLOCK DIAGRAM (PLCC Pin Configuration)



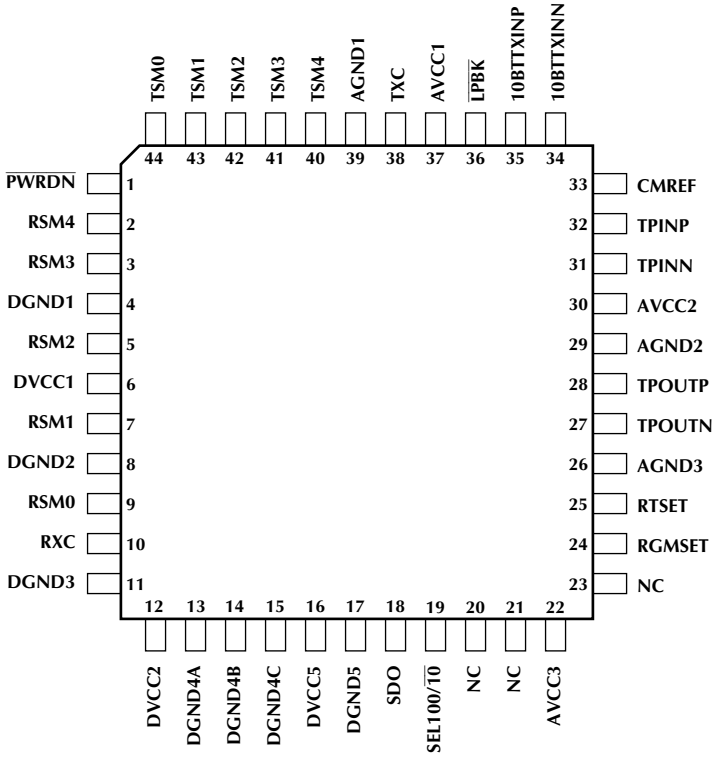
This datasheet has been downloaded from http://www.digchip.com at this page

PIN CONFIGURATION

ML6698
44-Pin PLCC (Q44)



ML6698
44-Pin TQFP (H44-10)



PIN DESCRIPTION (Pin numbers for TQFP package in parentheses)

PIN		NAME	DESCRIPTION
1	(39)	AGND1	Analog ground.
2-6	(40-44)	TSM<4:0>	Transmit data TTL inputs. TSM<4:0> inputs accept TX data symbols. Data appearing at TSM<4:0> are clocked into the ML6698 on the rising edge of TXC.
7	(1)	$\overline{\text{PWRDN}}$	Device power down input. A low signal powers down all ciruits of the ML6698, and dissipates less than 20mA.
8,9, 11,13, 15	(2, 3, 5, 7, 9)	RSM<4:0>	Receive data TTL outputs. RSM<4:0> outputs may be sampled synchronously with RXC's rising edge.
10	(4)	DGND1	Digital ground.
12	(6)	DVCC1	Digital +5V power supply.
14	(8)	DGND2	Digital ground.
16	(10)	RXC	Recovered receive symbol clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz bit clock recovered from the signal received at TPINP/N when data is present. Receive data at RSM<4:0> change on the falling edges and should be sampled on the rising edges of this clock. RXC is phase aligned to TXC when 100BASE-TX signal is not present at TPINP/N
17	(11)	DGND3	Digital ground.
18	(12)	DVCC2	Digital +5V power supply.
19	(13)	DGND4A	Digital ground.
20	(14)	DGND4B	Digital ground.
21	(15)	DGND4C	Digital ground.
22	(16)	DVCC5	Digital +5V power supply.
23	(17)	DGND5	Digital ground.
24	(18)	SD0	Signal detect TTL output. A high output level indicates 100BASE-TX activity at TPINP/N with an amplitude exceeding the preset threshold. The signal detect function is always active independent of the configuration of the SEL100/$\overline{10}$ pin.
25	(19)	SEL100/$\overline{10}$	Speed select TTL input. Driving this pin low disables 100BASE-TX transmit and receive functions, and enables the 10BASE-T transmit path from 10BTTXINP/N to TPOUTP/N. A high signal on SEL100/$\overline{10}$ disables the 10BTTXINP/N inputs and enables 100BASE-TX operation.
28	(22)	AVCC3	Analog positive power supply.
30	(24)	RGMSET	Equalizer bias resistor input. An external 9.53ký, 1% resistor connected between RGMSET and AGND3 sets internal time constants controlling the receive equalizer transfer function.
31	(25)	RTSET	Transmit level bias resistor input. An external 2.49ký, 1% resistor connected between RTSET and AGND3 sets a precision constant bias current for the twisted pair transmit level.
32	(26)	AGND3	Analog ground.
33,34	(27,28)	TPOUTN/P	Transmit twisted pair outputs. This differential current output pair drives MLT-3 waveforms into the network coupling transformer in 100BASE-TX mode, and 10BASE-T or FLP waveforms in 10BASE-T mode.
35	(29)	AGND2	Analog ground.
36	(30)	AVCC2	Analog +5V power supply.
37,38	(31, 32)	TPINN/P	Receive twisted pair inputs. This differential input pair receives 100BASE-TX signals from the network.

PIN DESCRIPTION (Continued)

PIN		NAME	DESCRIPTION
39	(33)	CMREF	Receiver common-mode reference output. This pin provides a common-mode bias point for the twisted-pair media line receiver. A typical value for CMREF is (VCC–1.26)V.
40,41	(34,35)	10BTTXINN/P	10BASE-T transmit waveform inputs. The ML6698 presents a linear copy of the input at 10BTTXINN/P to the TPOUTN/P outputs when the ML6698 functions in 10BASE-T mode. Signals presented to these pins must be centered at $V_{CC}/2$ with a single ended amplitude of ± 0.25V.
42	(36)	$\overline{\text{LPBK}}$	Loopback TTL input pin. Tying this pin to ground places the part in loopback mode; data at RSM<4:0> are serialized, MLT-3 encoded, equalized then sent to the receive PLL for clock recovery and sent to the RSM<4:0> outputs. Floating this pin or tying it to V_{CC} places the part in its normal mode of operation.
43	(37)	AVCC1	Analog +5V power supply.
44	(38)	TXC	Transmit clock TTL input. This 25MHz clock is the frequency reference for the internal transmit PLL clock multiplier. This pin should be driven by an external 25MHz clock at TTL or CMOS levels.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} Supply Voltage Range ..... GND –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... GND –0.3V to V_{CC} + 0.3V
  TPINP, TPINN, 10BTTXINP,
    10BTTXINN ..... GND –0.3V to V_{CC} + 0.3V
Output Current
  TPOUTP, TPOUTN 60mA
  All other outputs 10mA

Junction Temperature ..... 150°C
Storage Temperature ....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

V_{CC} Supply Voltage ..... 5V ± 5%
All V_{CC} supply pins *must* be within 0.1V of each other.
All GND pins *must* be within 0.1V of each other.
T_A, Ambient temperature .....0°C to 70°C
RGMSET ..... 9.53ký ± 1%
RTSET ..... 2.49ký ± 1%
Receive transformer insertion loss..... <–0.5dB

DC ELECTRICAL CHARACTERISTICS

Over full range of operating conditions unless otherwise specified (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TTL Inputs (TSM<4:0>, TXC, SEL100/$\overline{10}$, $\overline{PWRDN}$, $\overline{LPBK}$)						
V_{IL}	Input Low Voltage	I_{IL} = –400µA			0.8	V
V_{IH}	Input High Voltage	I_{IH} = 100µA	2.0			V
I_{IL}	Input Low Current	V_{IN} = 0.4V	–200			µA
I_{IH}	Input High Current	V_{IN} = 2.7V			100	µA
TTL Outputs (RSM<4:0>, RXC, SDO)						
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4			V
Receiver						
V_{ICM}	TPINP/N Input Common-Mode Voltage	100ý Termination across TPINP/N		V_{CC} – 1.26		V
V_{ID}	TPINP-TPINN Differential Input Voltage Range		–3.0		3.0	V
R_{IDR}	TPINP-TPINN Differential Input Resistance		10.0k			ý
I_{ICM}	TPINP/N Common-Mode Input Current				+10	µA
I_{RGM}	RGMSET Input Current	RGMSET = 9.53ký		130		µA
I_{RT}	RTSET Input Current	RTSET = 2.49ký		500		µA
Transmitter						
I_{TD100}	TPOUTP/N 100BASE-TX Mode Differential Output Current	Note 2, 3	±19		±21	mA
I_{TD10}	TPOUTP/N 10BASE-T Mode Differential Output Current		±55	±60	±65	mA
I_{TOFF}	TPOUTP/N Off-State Output	R_L = 200, 1%	0		1.5	mA
I_{TXI}	TPOUTP/N Differential Output Current Imbalance	R_L = 200, 1%			500	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter (Continued)						
X_{ERR}	TPOUTP/N Differential Output Current Error	$V_{OUT} = V_{CC}$; Note 3	–5.0		+5.0	%
X_{CMP100}	TPOUTP/N 100BASE-X Output Current Compliance Error	$V_{OUT} = V_{CC} \pm 2.2V$; referred to I_{OUT} at V_{CC}	–2.0		+2.0	%
V_{OCM10}	TPOUTP/N 10BASE-T Output Voltage Compliance Range	I_{TD10} remains within specified values	$V_{CC} – 2.7$		$V_{CC} + 2.7$	V
V_{ICM10}	10BTTXNN/P Input Common-Mode Voltage Range		$V_{CC}/2 – 0.3$		$V_{CC}/2 + 0.3$	V
Power Supply Current						
I_{CC100}	Supply Current, 100BASE-TX Operation, Transmitting	Current into all V_{CC} pins, $V_{CC} = 5.25V$ (Note 2)		195	260	mA
I_{CC10}	Supply Current, 10BASE-T Mode			155	175	mA
I_{CCOFF}	Supply Current Power Down Mode	$\overline{PWRDN}$			20	mA

AC ELECTRICAL CHARACTERISTICS

Over full range of operating conditions unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{TR/F}$	TPOUTP-TPOUTN Differential Rise/Fall Time	Notes 5, 6; for any legal code sequence	3.0		5.0	ns
t_{TM}	TPOUTP-TPOUTN Differential Rise/Fall Time Mismatch	Notes 5, 6; for any legal code sequence	–0.5		0.5	ns
t_{TDC}	TPOUTP-TPOUTN Differential Output Duty Cycle Distortion	Notes 4, 6	–0.5		0.5	ns
t_{TJT}	TPOUTP-TPOUTN Differential Output Peak-to-Peak Jitter	Note 6		300	1400	ps
X_{OST}	TPOUTP-TPOUTN Differential Output Voltage Overshoot	Notes 6, 7			5	%
t_{TXP}	Transmit Bit Delay	Note 8			10.5	Bit Times
t_{RXDC}	Receive Bit Delay	Note 9			15.5	Bit Times

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MII (Media-Independent Interface)						
X_{BTOL}	TX Output Clock Frequency Tolerance	25MHz frequency	–100		+100	ppm
t_{TPWH}	TXC pulse width HIGH		14			ns
t_{TPWL}	TXC pulse width LOW		14			ns
t_{RPWH}	RXC pulse width HIGH		14			ns
t_{RPWL}	RXC pulse width LOW		14			ns
t_{TPS}	Setup time, TSM<4:0> Data Valid to TXC Rising Edge (1.4V point)		12			ns
t_{TPH}	Hold Time, TSM<4:0> Data Valid After TXC Rising Edge (1.4V point)		3			ns
t_{RCS}	Time that RSM<4:0> Data are Valid Before RXC Rising Edge (1.4V point)		10			ns
t_{RCH}	Time that RSM<4:0> Data are Valid After RXC Rising Edge (1.4V point)		10			ns
t_{RPCR}	RXC 10% – 90% Rise Time				6	ns
t_{RPCF}	RXC 90%-10% Fall Time				6	ns

Note 1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.
Note 2. Measured using the test circuit shown in Fig. 1, under the following conditions:
R_{LP} = 200ý, R_{LS} = 49.9ý, R_{TSET} = 2.49ký.
All resistors are 1% tolerance.
Note 3. Output current amplitude is I_{OUT} = 40 3 1.25V/RTSET.
Note 4. Measured relative to ideal negative and positive signal 50% points, using the four successive MLT-3 transitions for the 01010101 bit sequence.
Note 5. Time difference between 10% and 90% levels of the transition from the baseline voltage (nominally zero) to either the positive or negative peak signal voltage. The times specified here correlate to the transition times defined in the ANSI X3T9.5 TP-PMD Rev 2.0 working draft, section 9.1.6, which include the effects of the external network coupling transformer and EMI/RFI emissions filter.
Note 6. Differential test load is shown in fig. 1 (see note 3).
Note 7. Defined as the percentage excursion of the differential signal transition beyond its final adjusted value during the symbol interval following the transition. The adjusted value is obtained by doing a straight line best-fit to an output waveform containing 14 bit-times of no transition preceded by a transition from zero to either a positive or negative signal peak; the adjusted value is the point at which the straight line fit meets the rising or falling signal edge.
Note 8. Symbol /J/ at TSM <4:0> sampled by TXC to first bit of /J/ at MDI.
Note 9. First bit of /J/ at MDI to first rising edge of RXC after the last part of the /J/ appears at RSM <4:0>.

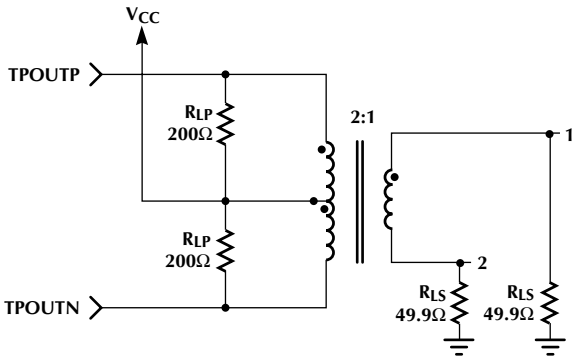


Figure 1. Test Circuit

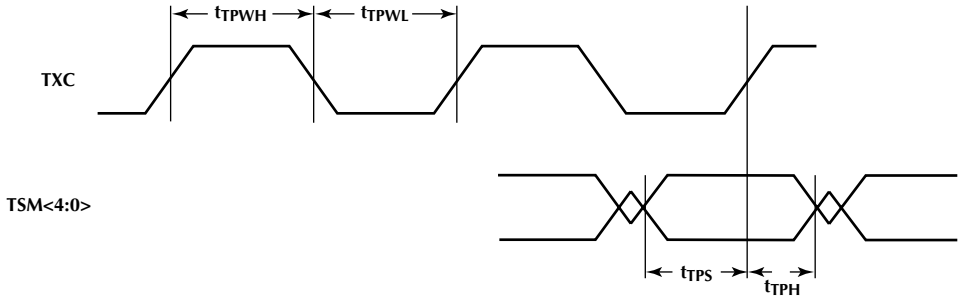


Figure 2.

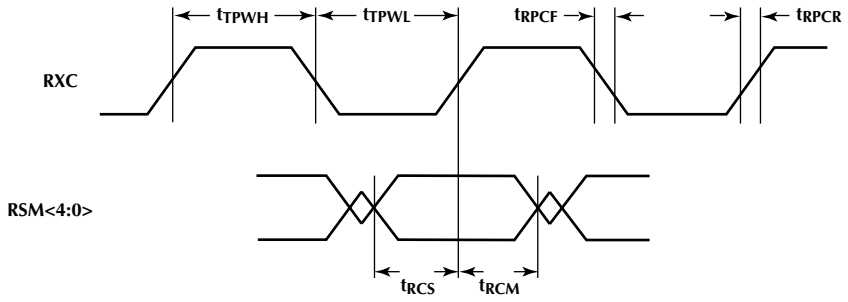


Figure 3.

FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

100BASE-TX Operation

The transmitter accepts scrambled 5-bit symbols clocked in at 25MHz and outputs MLT-3 signals onto the twisted-pair media at 100Mbps. The on-chip transmit PLL converts a 25MHz TTL-level clock at TXC to an internal 125MHz bit clock. TXC from the ML6698 clocks scrambled transmit symbols from the MAC into the ML6698's TSM<4:0> input pins. Symbols from the TSM<4:0> inputs are converted from parallel to serial form at the 125MHz clock rate. The serial transmit data is converted to MLT-3 3-level code and driven differentialy out of the TPOUTP and TPOUTN pins at nominal ± 2V levels with the proper loads. The transmitter is designed to drive a center-tapped transformer with a 2:1 winding ratio, so a differential 400 ohm load is used on the transformer primary to properly terminate the 100 ohm cable and termination on the secondary. The transformer's center tap must be tied to V_{CC}. A 2:1 transformer allows using a ±20mA output current in 100BASE-TX mode. Using a 1:1 transformer would have required twice the output current and increased the on-chip power dissipation. An external 2.49kΩ, 1% resistor at the RTSET pin creates the correct output levels at TPOUP/N.

10BASE-T

In 10BASE-T mode, the transmitter acts as a linear buffer with a gain of 10. 10BASE-T inputs (Manchester data and normal link pulses) at 10BTTXINP/N appear as full-swing signals at TPOUTP/N in this mode. Inputs to the 10BTTXINP/N pins should have a nominal ±0.25V differential amplitude and a common-mode voltage of $V_{CC}/2$, and should also be waveshaped or filtered to meet the 10BASE-T harmonic content requirements. The ML6698 does not provide any 10BASE-T transmit filtering.

RECEIVE SECTION

The receiver converts 3-level MLT-3 signals from the twisted-pair media to 5-bit scrambled symbols at RSM<4:0> with extracted clock at RXC. The adaptive equalizer compensates for the distortion of up to 140m of cable and attenuates cable-induced jitter, corrects for DC baseline wander, and converts the MLT-3 signal to 2-level NRZ. The receive PLL extracts clock from the equalized signal, providing additional jitter attenuation, and clocks the signal through the serial to parallel converter. The resulting 5-bit symbols appear at RSM<4:0>. The extracted clock appears at RXC. Resistor RGMSET sets internal time constants controlling the adaptive equalizer's transfer function. RGMSET must be set to 9.53k (1%).

LOOPBACK

Tying $\overline{LPBK}$ pin low places the part in loopback mode. Data at TXD<4:0> are serialized, MLT-3 encoded, equalized, then sent to receive PLL for clock recovery and sent to the RXD<4:0> outputs.

In this mode, data at TXD<4:0> has to be valid 5-bit symbol data.

ML6698 SCHEMATIC

Figure 2 shows a general design where the 5-bit and other control signals interface to the controller. TXC is connected to a 25MHz, 100ppm clock oscillator.

Inductors L1 and L2 are for the purpose of improving return loss.

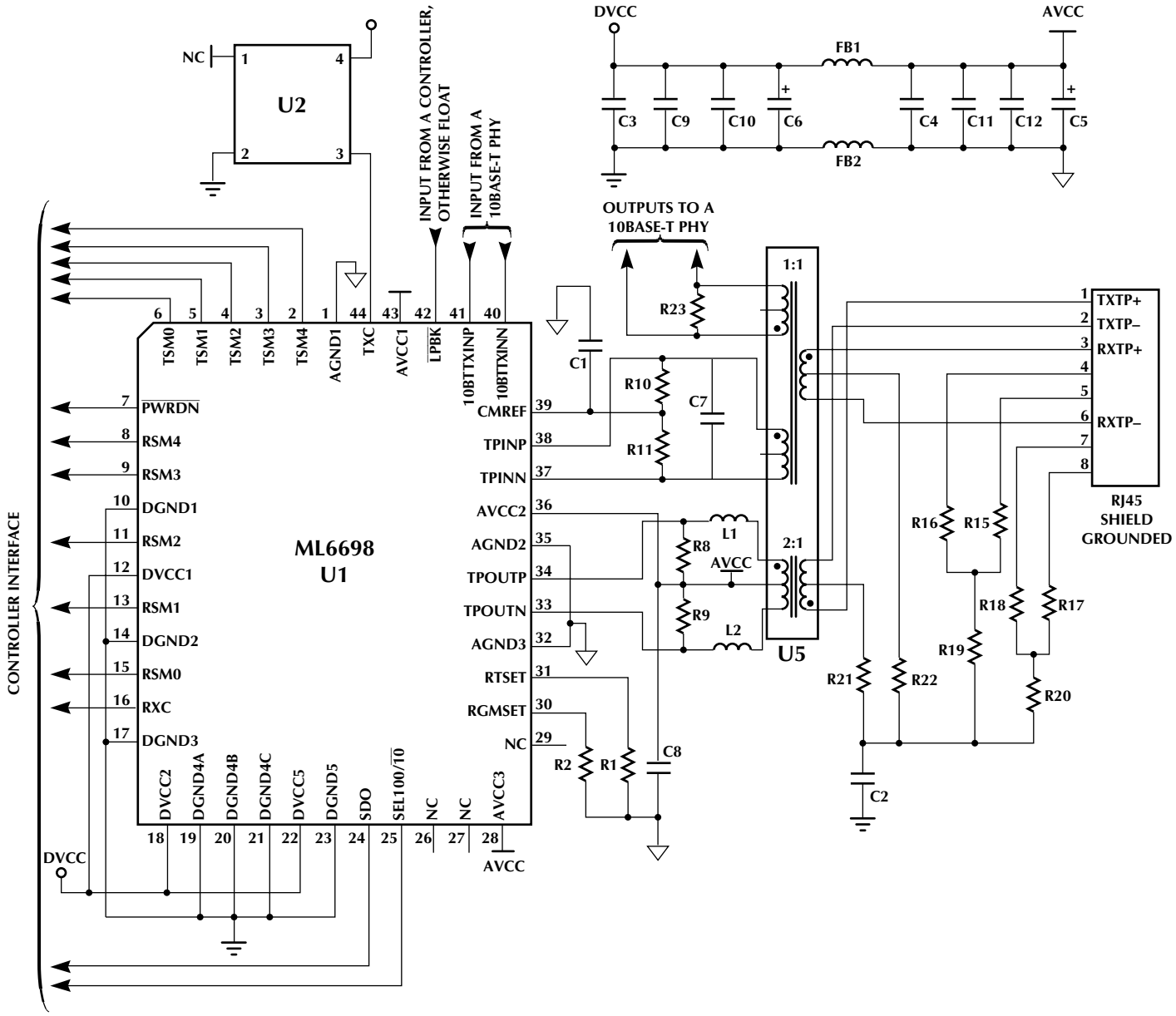
Capacitor C7 is recommended. It decouples some noise at the inputs of the ML6698 and improves the Bit Error Rate (BER) performance of the board.

It is recommended having a 0.1µF capacitor on every V_{CC} pin as indicated by C3, 4, 9-12. Also, it is recommended to split the A_{VCC} and D_{VCC}, AGND and DGND. It is recommended that AGND and DGND planes are large enough for low inductance. If splitting the two grounds and keeping the ground planes large enough is not possible due to board space, you could join them into one larger ground plane.

DIFFERENCES BETWEEN THE ML6694 AND ML6698

Both parts are pin to pin compatible and perform the same functions. The only differences are:

1. SDO: The ML6694 has SDO (Signal Detect Output) active in 100BASE-TX mode only, while the ML6698 has it active in both 10BASE-T and 100BASE-TX modes.
2. SEL10/$\overline{100}$ or SEL100/$\overline{10}$: The ML6694 has the 100BASE-TX mode active low and the 10BASE-T mode active high (SEL10/$\overline{100}$). The ML6698 has the opposite polarity where the 100BASE-TX mode is active high and the 10BASE-T mode is active low (SEL100/$\overline{10}$).

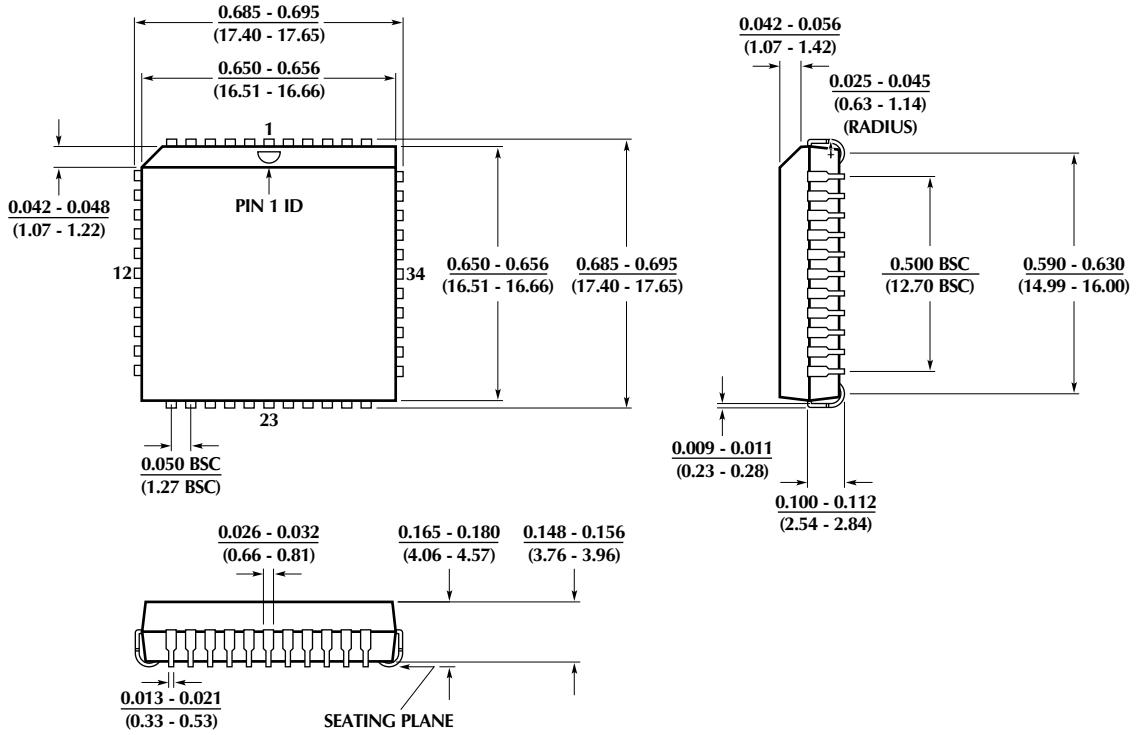


R1	2.49kΩ 1%, 1/8W Surface Mount
R2	9.53kΩ 1%, 1/8W Surface Mount
R8, R9, R23	200Ω 1%, 1/8W Surface Mount
R10, R11	100Ω 1%, 1/8W Surface Mount
R15-R20	49.9Ω 5%, 1/8W Surface Mount
R21-R22	75Ω 5%, 1/8W Surface Mount
C1, C3, C4, C8-C12	0.1µF Ceramic Chip Cap
C5, C6	10µF Tantalum Cap
C7	10pF Cap
C2	Board Layer Cap (2kV rated)
U1	ML6698 44-PLCC Surface Mount
U2	Clock Oscillator, 25MHz 4-Pin Surface Mount
U5	Bel Transformer Module S558-1287-02, XFMRS Inc. XF6692TX, or Valor ST6129 (not pin compatible)
FB1, FB2	Fair-Rite SM Bead P/N 2775019447
L1, L2	130nH Inductors rated at 50MHz

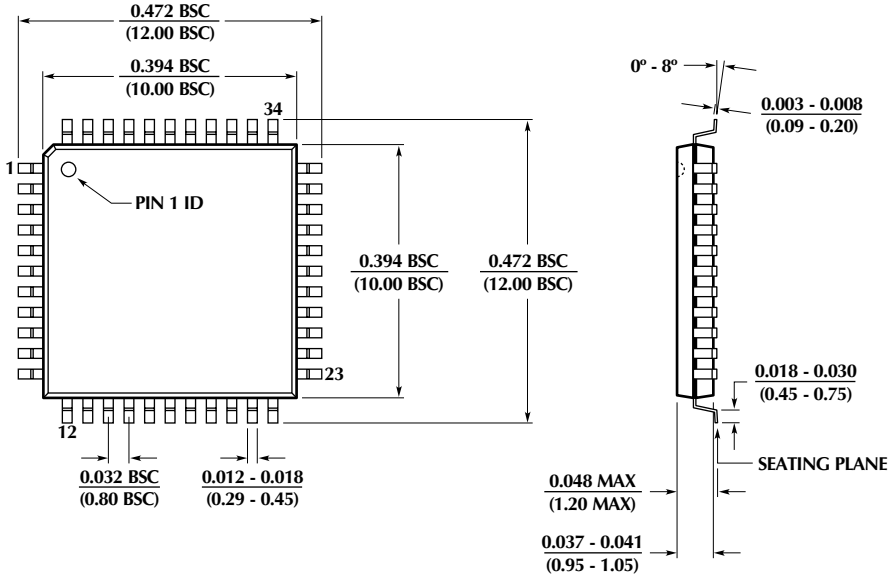
Figure 2. ML6698 Typical Applications Circuit

PHYSICAL DIMENSIONS inches (millimeters)

Package: Q44
44-Pin PLCC



Package: H44-10
44-Pin (10 x 10 x 1mm) TQFP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6698CQ (End Of Life)	0°C to 70°C	44-PIN PLCC (Q44)
ML6698CH	0°C to 70°C	44-PIN TQFP (H44-10)

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