Hardware Reference Booklet (CRAY T3E™ Series)

HRQ-366-A

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Record of Revision

Each time this booklet is revised and reprinted, all changes issued against the previous version are incorporated into the new version, and the new version is assigned an alphabetic level, which is indicated in the publication number on each page of the booklet.

Changes to part of a page are indicated by a change bar in the margin directly opposite the change. A change bar in the footer indicates that most, if not all, of the page is new. If the booklet is rewritten, the revision level changes but the booklet does not contain change bars.

Revision	Description
	October 1996. Original printing.
A	June 1997. This revision changes the printed circuit board (PCB) diagrams so that they more clearly depict which components are visible when the PCB is mounted to the coldplate; all components that are not visible are outlined with a dashed line (grayed). This revision also adds a table that lists the I option memory-mapped registers that you can access via the GigaRing channel.

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CRAY T3E Hardware Reference Booklet

t3ems Standard Locations

Variable	Location	Description
_excl_use_secs	80080	Bit mask that indicates which section(s) need exclusive use of the system to execute properly
_whoami	80090	Logical PE number
_config_array	80088	Address of the configuration array that shows how the network is configured
_sbes	800B0	Number of single-bit errors that occurred
_sbe_last	800B8	Last single-bit error logged in the sbe_table
_sbe_table	80500 – 806F8	List of single-bit errors
_start	80000	Starting address for the diagnostic
_pe_mask	802C0 – 803D8	Bit mask that indicates which PEs are running the test
_r_pe_mask	803F0 – 804F8	Bit mask that indicates which PEs have memory available for the test to use
_r_base	803E0	Remote base address
_r_limit	803E8	Remote limit address
_secs	80020	Bit mask that indicates which sections are enabled
_timeout	80038	Amount of time to wait for an event to occur before timing out
_clmask	80040 – 80078	Bit mask for cacheline size: 0 = disable (ignore bits that are 0)
_addrmask	80030	Bit mask for address: 0 = disable (ignore address bits that are 0)
_estop	80028	Error stop flag: 0 = continue, 1 = stop
_seed	80280	Random-number generator seed
_param 0 – 31	80700 – 807F8	Parameters that are unique to a test
_base	80270	Base memory address

t3ems Standard Locations (continued)

Variable	Location	Description
_limit	80278	Limit memory address
_pass_cnt	80098	Pass count
_fail_cnt	800A0	Fail count
_life	800A8	Life count
_sec_pass	800C0 – 80138	Section pass count
_sec_fail	80140 – 801B8	Section fail count
_ecode	801C0	Error code
_sec	801C8	Current test section
_cond	801D0	Current test condition
_exp	801D8	Expected data
_act	801E0	Actual data
_diff	801E8	Difference between the actual and expected data
_info0 – 15	801F0 – 80268	Failing information for a test

The following error codes may be displayed by a failing diagnostic; however, the failure actually occurred while executing the PAL code. The registers listed in the table, with the exception of error code 40030000, are internal to the microprocessor.

PAL Error Codes

Error Code	Description
40000080	Indicates that an I-stream violation occurred. _info10 contains the contents of the exception address register
40000100	Indicates that internal microprocessor interrupt occurred. _info10 contains the contents of the exception address register
40000280	Indicates that a unexpected data translation interrupt occurred while executing the PAL code. _info10 contains the contents of the exception address register
40000300	Indicates that an unaligned reference error occurred. _info10 contains the contents of the exception address register _info11 contains the contents of the faulting virtual address register _info12 contains the contents of the Dstream memory management fault status register
40000380	Indicates that a data fault occurred. _info10 contains the contents of the exception address register _info11 contains the contents of the faulting virtual address register _info12 contains the contents of the Dstream memory management fault status register
40000400	Indicates that a machine check occurred.
40000480	Indicates that an illegal DEC instruction issued. _info10 contains the contents of the exception address register

PAL Error Codes (continued)

Error Code	Description
40000500	Indicates that an unexpected arithmetic interrupt occurred. _info10 contains the contents of the exception address register _info11 contains the contents of the exception summary register
40000580	Indicates that a floating-point error occurred. _info10 contains the contents of the exception address register _info11 contains the contents of the Ibox control and status register
40030000	Indicates that an unexpected interrupt occurred from the support circuitry. _info10 contains the execution address where the interrupt was encountered _info11contains the address of the error memory-mapped register (MMR) thar contains the error (M_ERR0, C_ERR0, I_ERR0, and R_ERR0) _info12 contains the contents of x_ERR0 (x is the interrupting option) _info13 contains the contents of x_ERR1 _info14 contains the contents of x_ERR2 _info15 contains the contents of x_ERR3

lmem.pgm and rmem.pgm log the error information shown in the following table in location 80500.

Decode of sbe_table

Bits	Description
<63: 32>	Byte address
<31: 24>	Bit in error; aa indicates a multiple-bit error; ff indicates a double-bit error
<22 : 16>	Syndrome (Refer to the following table)
<15 : 0>	Counter

Syndrome Codes

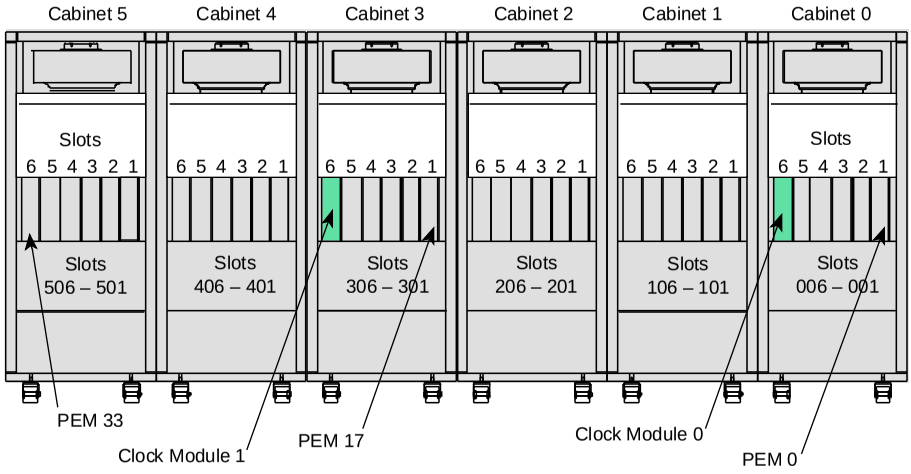
Bit	Syndrome Code
0	4f
1	4a
2	52
3	54
4	57
5	58
6	5B
7	5D
8	23
9	25
10	26
11	29
12	2a
13	2c
14	31
15	34
16	0e

Syndrome Code	Bit
01	CB 0
02	CB 1
04	CB 2
08	CB 3
0b	17
0e	16
10	CB 4
13	18
15	19
16	20
19	21
1a	22
1c	23
20	CB 5
23	8
25	9
26	10

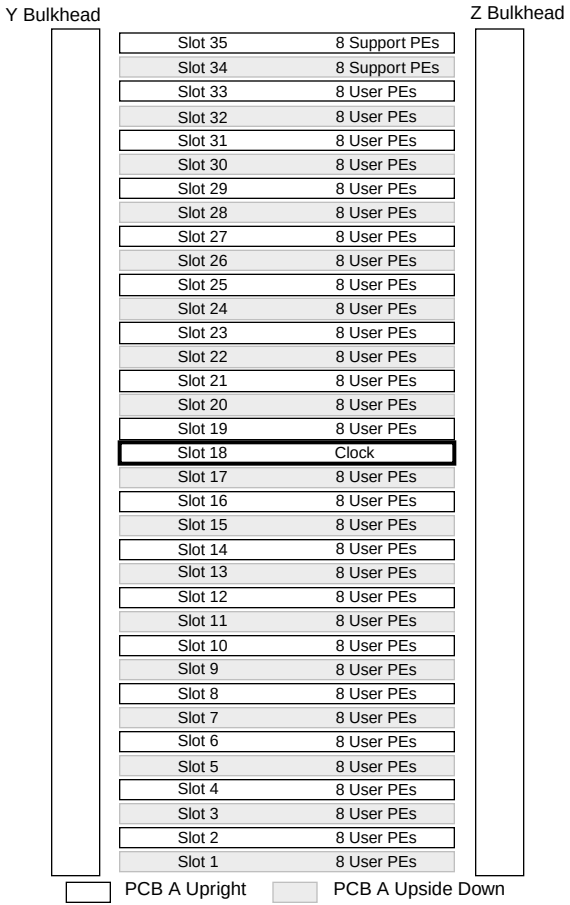
Syndrome Codes (continued)

Bit	Syndrome Code
17	0b
18	13
19	15
20	16
21	19
22	1a
23	1c
24	62
25	64
26	67
27	68
28	6b
29	6d
30	70
31	75
CB 0	01
CB 1	02
CB 2	04
CB 3	08
CB 4	10
CB 5	20
CB 6	40

Syndrome Code	Bit
29	11
2a	12
2c	13
31	14
34	15
40	CB 6
4a	1
4f	0
52	2
54	3
57	4
58	5
5b	6
5d	7
62	24
64	25
67	26
68	27
6b	28
6d	29
70	30
75	31

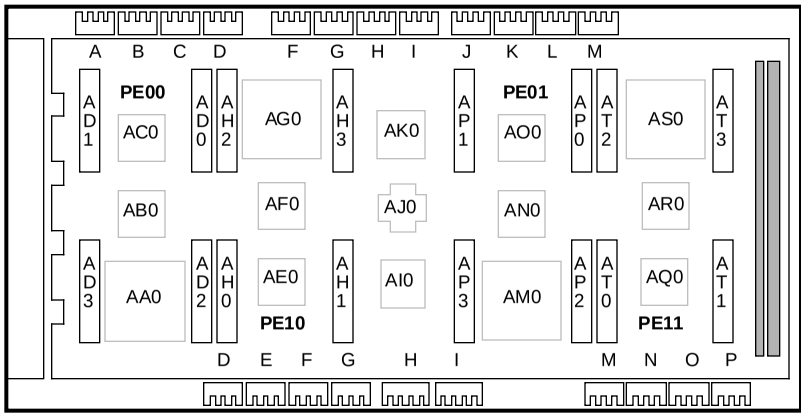


Air-cooled Chassis, Module Insertion End



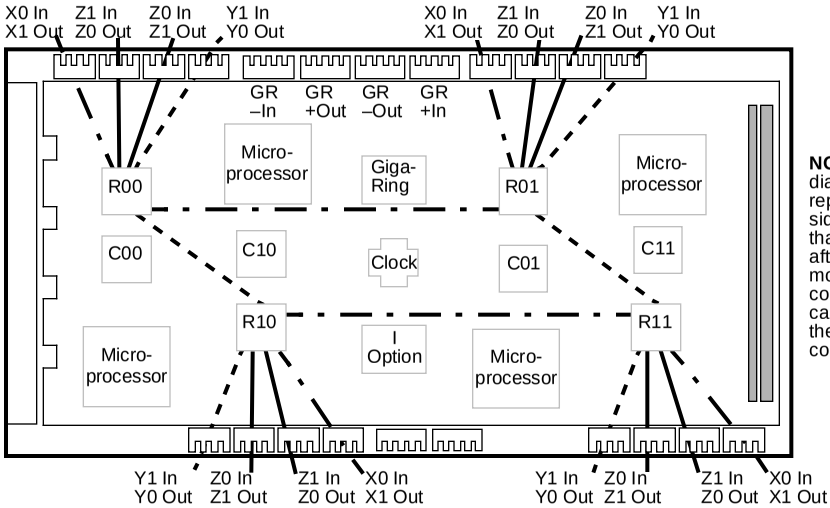
Liquid-cooled Chassis, Module Insertion End

Logical Option and Connector Locations



NOTE: This diagram represents the side of the PCB that is visible after it is mounted to the coldplate with the daughter cards removed; you can not see the “grayed” components.

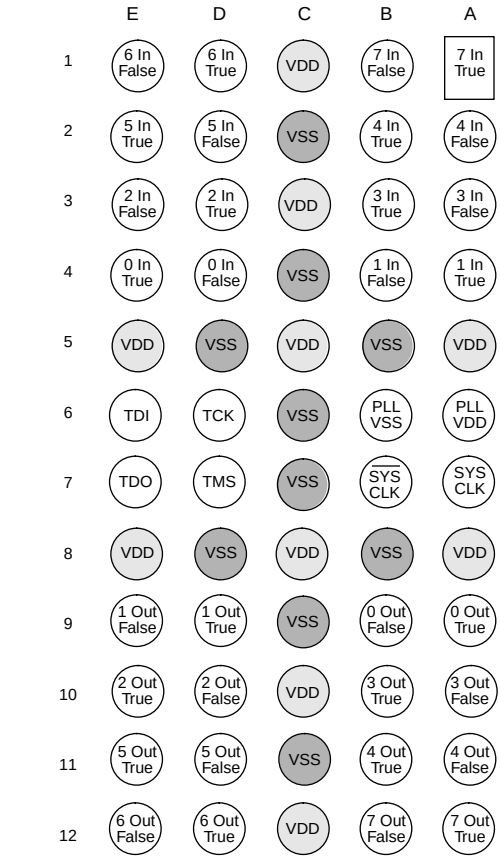
Physical Option and Connector Locations



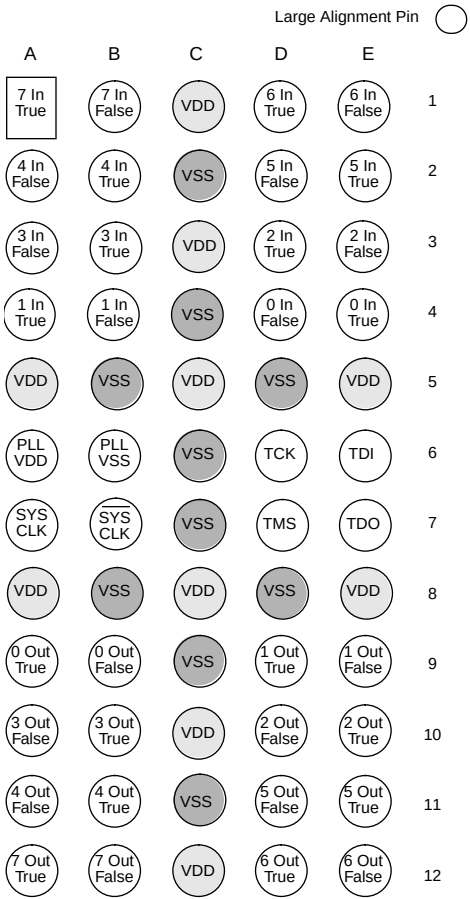
NOTE: This diagram represents the side of the PCB that is visible after it is mounted to the coldplate; you can not see the “grayed” components.

Layout of the Interconnect Network on a PCB

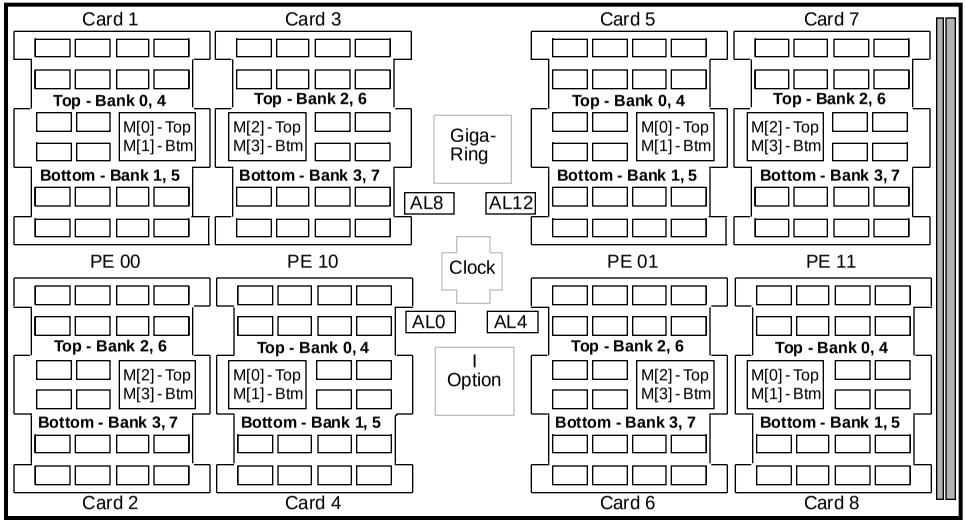
Module Testpoints



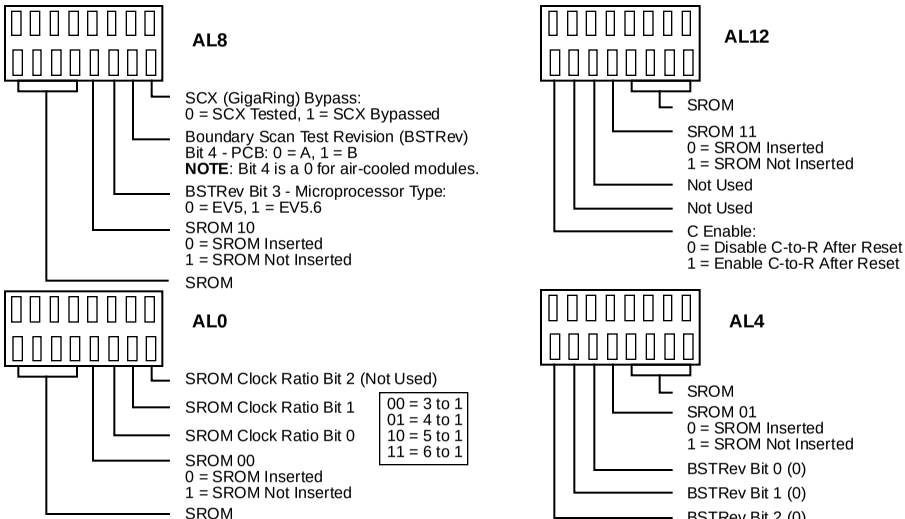
Pin Assignment for Daughter-card Jumper Pins



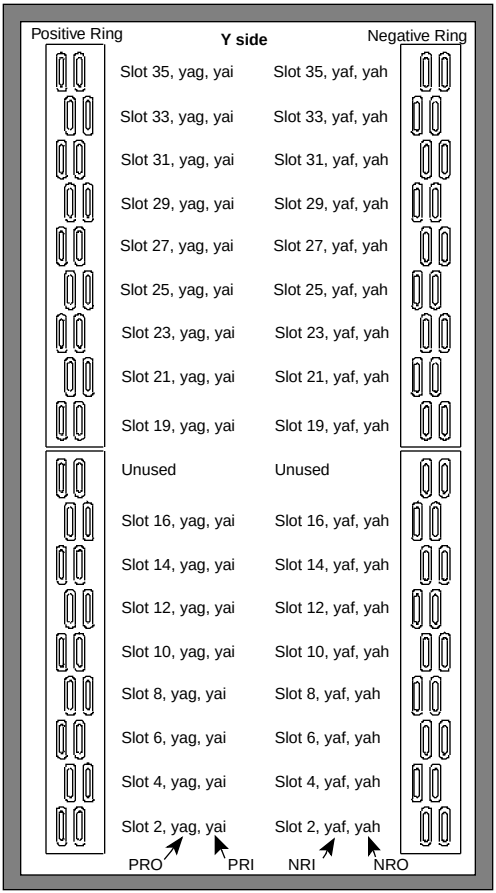
Pin Assignment for Daughter-card Jumper Pins (con't)



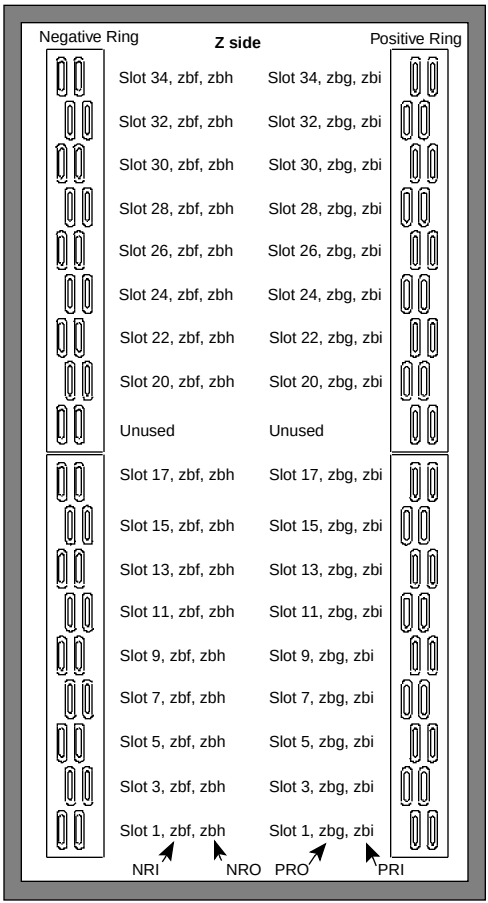
Daughter Card Locations



Pin Assignment of Jumper Blocks

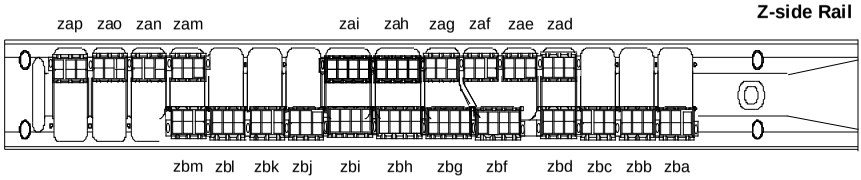


Liquid-cooled Cabinet Bulkhead, Y Side



Liquid-cooled Cabinet Bulkhead, Z Side

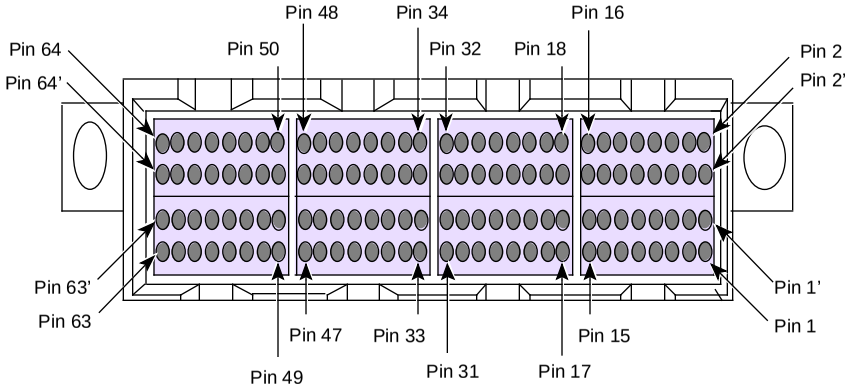
Air-cooled Cabinet Bulkhead



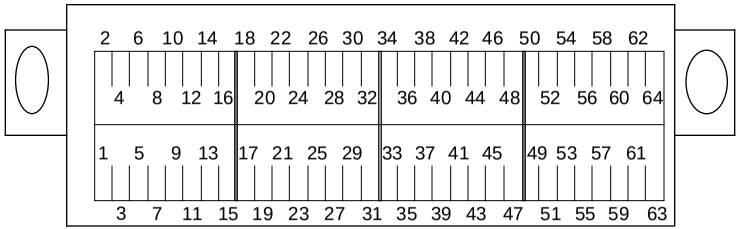
Liquid-cooled PE Module Rails

Liquid-cooled Clock Rails

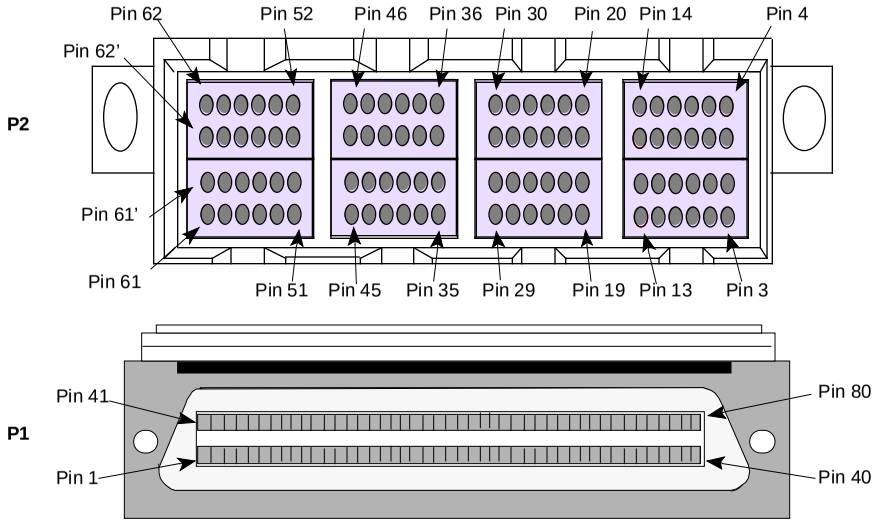
Air-cooled PE and Clock Rails



Four-shuttle Clock and Boundary Scan Connector, View from Module



Four-shuttle Clock and Boundary Scan Connector, View from Wire-insertion End

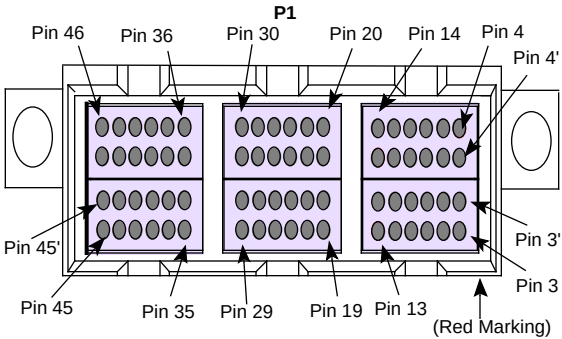


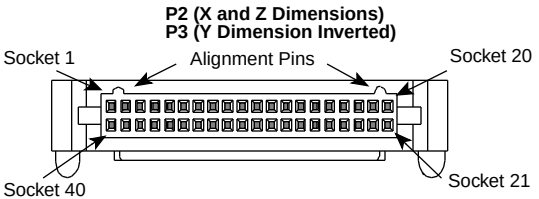
Four-shuttle GigaRing Connector (P2) and GigaRing Bulkhead Connector (P1)

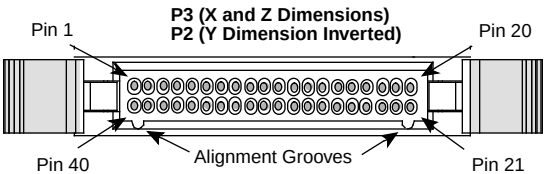
Pin Assignments for the Bulkhead to Rail Connections

Source	Destination		Source	Destination		Source	Destination
P1–1	P2–56		P1–28	P2–39		P1–55	P2–24’
P1–2	P2–56’		P1–29	P2–39’		P1–56	Ground
P1–3	P2–52		P1–30	P2–35		P1–57	P2–14
P1–4	P2–52’		P1–31	P2–35’		P1–58	P2–14’
P1–5	P2–44		P1–32	Ground		P1–59	P2–57
P1–6	P2–44’		P1–33	P2–25		P1–60	P2–57’
P1–7	P2–40		P1–34	P2–25’		P1–61	P2–53
P1–8	P2–40’		P1–35	P2–23		P1–62	P2–53’
P1–9	Ground		P1–36	P2–23’		P1–63	P2–45
P1–10	P2–30		P1–37	P2–19		P1–64	P2–45’
P1–11	P2–30’		P1–38	P2–19’		P1–65	Ground
P1–12	P2–26		P1–39	P2–11		P1–66	P2–41
P1–13	P2–26’		P1–40	P2–11’		P1–67	P2–41’
P1–14	P2–22		P1–41	Ground		P1–68	P2–37
P1–15	P2–22’		P1–42	P2–54		P1–69	P2–37’
P1–16	P2–20		P1–43	P2–54’		P1–70	P2–29
P1–17	P2–20’		P1–44	P2–46		P1–71	P2–29’
P1–18	P2–12		P1–45	P2–46’		P1–72	P2–27
P1–19	P2–12’		P1–46	P2–42		P1–73	P2–27’
P1–20	P2–8*		P1–47	P2–42’		P1–74	P2–21
P1–21	P2–8’*		P1–48	P2–38		P1–75	P2–21’
P1–22	P2–55		P1–49	P2–38’		P1–76	P2–13
P1–23	P2–55’		P1–50	P2–36		P1–77	P2–13’
P1–24	P2–51		P1–51	P2–36’		P1–78	P2–9
P1–25	P2–51’		P1–52	P2–28		P1–79	P2–9’
P1–26	P2–43		P1–53	P2–28’		P1–80	Ground
P1–27	P2–43’		P1–54	P2–24			

* GigaRing Clock







Cable Connector Color Code:

X Dimension – Grey
Y Dimension – Green
Z Dimension – Blue
Y Dimension Inverted – Red

Torus Cables (P1, P2, and P3)

Pin Assignments for Torus Cables

Source	Destination	Source	Destination	Source	Destination
P1–3	P3–39	P1–19	P3–33	P1–35	P3–27
P1–3’	P3–2	P1–19’	P3–8	P1–35’	P3–14
P1–4	P2–2	P1–20	P2–8	P1–36	P2–14
P1–4’	P2–39	P1–20’	P2–33	P1–36’	P2–27
P1–5	P3–38	P1–21	P3–32	P1–37	P3–26
P1–5’	P3–3	P1–21’	P3–9	P1–37’	P3–15
P1–6	P2–3	P1–22	P2–9	P1–38	P2–15
P1–6’	P2–38	P1–22’	P2–32	P1–38’	P2–26
P1–7	P3–37	P1–23	P3–31	P1–39	P3–25
P1–7’	P3–4	P1–23’	P3–10	P1–39’	P3–16
P1–8	P2–4	P1–24	P2–10	P1–40	P2–16
P1–8’	P2–37	P1–24’	P2–31	P1–40’	P2–25
P1–9	P3–36	P1–25	P3–30	P1–41	P3–24
P1–9’	P3–5	P1–25’	P3–11	P1–41’	P3–17
P1–10	P2–5	P1–26	P2–11	P1–42	P2–17
P1–10’	P2–36	P1–26’	P2–30	P1–42’	P2–24
P1–11	P3–35	P1–27	P3–29	P1–43	P3–23
P1–11’	P3–6	P1–27’	P3–12	P1–43’	P3–18
P1–12	P2–6	P1–28	P2–12	P1–44	P2–18
P1–12’	P2–35	P1–28’	P2–29	P1–44’	P2–23
P1–13	P3–34	P1–29	P3–28	P1–45	P3–22
P1–13’	P3–7	P1–29’	P3–13	P1–45’	P3–19
P1–14	P2–7	P1–30	P2–13	P1–46	P2–19
P1–14’	P2–37	P1–30’	P2–28	P1–46’	P2–22

Decimal to Hexadecimal Conversion

Dec	Hex	Dec	Hex	Ck Bit	Dec	Hex	Ck Bit
0		28	1c		56	38	
1		29	1d		57	39	
2		30	1e		58	3a	
3		31	1f		59	3b	
4		32	20		60	3c	
5		33	21		61	3d	
6		34	22		62	3e	
7		35	23		63	3f	
8		36	24		64	40	
9		37	25		65	41	
10	a	38	26		66	42	
11	b	39	27		67	43	
12	c	40	28		68	44	
13	d	41	29		69	45	
14	e	42	2a		70	46	
15	f	43	2b		71	47	
16	10	44	2c		72	48	
17	11	45	2d		73	49	
18	12	46	2e		74	4a	
19	13	47	2f		75	4b	
20	14	48	30		76	4c	
21	15	49	31		77	4d	
22	16	50	32		78	4e	
23	17	51	33		79	4f	
24	18	52	34		80	50	
25	19	53	35		81	51	
26	1a	54	36		82	52	
27	1b	55	37		83	53	

Decimal to Hexadecimal Conversion (continued)

Bit	Hex	Dec	Hex	Ck Bit	Dec	Hex	Ck Bit
84	54	108	6c		132	84	4
85	55	109	6d		133	85	5
86	56	110	6e		134	86	6
87	57	111	6f		135	87	7
88	58	112	70		136	88	8
89	59	113	71		137	89	9
90	5a	114	72		138	8a	10
91	5b	115	73		139	8b	11
92	5c	116	74		140	8c	12
93	5d	117	75		141	8d	13
94	5e	118	76		142	8e	14
95	5f	119	77		143	8f	15
96	60	120	78		144	90	16
97	61	121	79		145	91	17
98	62	122	7a		146	92	18
99	63	123	7b		147	93	19
100	64	124	7c		148	94	20
101	65	125	7d		149	95	21
102	66	126	7e		150	96	22
103	67	127	7f		151	97	23
104	68	128	80	0	152	98	24
105	69	129	81	1	153	99	25
106	6a	130	82	2	154	9a	26
107	6b	131	83	3	155	9b	27

The following table lists the I option memory-mapped registers (MMRs) that you can access via the GigaRing channel.

I Option MMRs Accessed from the GigaRing Channel

GigaRing Address	I Option MMR	Description
0x0001	I_REV or SCX_CLIENT_ID	Contains the I option revision information
0x0010	SCX_PKT_LIMIT	Holds NodeLs and NodeLc values for client congestion control
0x0011	SCX_FLOW	Holds Tc, Ts, Rc, and Rs values for client congestion control
0x0100	I_MON0	Hardware error monitor
0x101	I_MON1	Hardware error monitor
0x102	I_MON2	Hardware error monitor
0x103	I_MON3	Hardware error monitor
0x0110	I_ERR0	Access SCX option
0x0111	I_ERR1	Error monitor
0x0112	I_STATUS	General I/O status and control register

Notes