Clock and Boundary Scan

HMM-360-A.1
CRAY T3E Series Systems
Last Modified: December 1997

Record of Revision

October 1996

Original printing.

Revision A: July 1997

This revision includes the following changes to the existing information; no new information has been added.

- Changed the speed of the XCLK from 6.67 ns to 8.0 ns.
- Changed the title of Figure 7 from “Reading the Identification Register” to “Reading the Instruction Register.”
- Changed the titles of Figure 26 and Figure 34 from “Boundary Scan Options Window” to “T3EMS Scan Tool Options Window.” In addition, changed all of the text references of the Boundary Scan Options window to T3EMS Scan Tool Options window.
- Removed the Mode field from Figure 26 and Figure 34.
- Changed the orientation of the printed circuit board in Figure 32.
- Changed the name of the t3etap window from “T3E TAP Debugger” to “T3E TAP Tool.” In addition, changed all of the text references of the T3E TAP Debugger window to T3E TAP Tool window.
- Updated the boundary scan snaps.
- Removed the following figures and their associated text:
  - Z-side Fanout
  - Y-side Fanout
  - Hexadecimal to Binary Conversion
  - Test Pattern
  - Boundary Scan Test Locations within a PCB

Revision A.1: December 1997

This revision updates the screen snaps so that they are current with the SWS-ION 3.6 system release. This revision also adds a description of how to interpret the PCB identifier in the physical boundary scan failure information for an air-cooled system, a description of the new boundary scan tests, and diagrams illustrating the fanout of the test data, test clock, and test mode select signals.

Introduction

This document describes the components of the clock module. Specifically, you will learn:

- How many clocks the CRAY T3E™ system uses
- The speeds of the clocks
- How the clock signals are fanned out

This document also describes the boundary scan feature and how it is implemented in the CRAY T3E system. Specifically, you will learn:

- The function of each boundary scan component
- The path of the test data through the cabinet
- The functions of the boundary scan test
- How to initiate the boundary scan test
- How to interpret the error information

Terms

You will need to know how the following terms are used in this document to fully understand the material discussed in this document:

Processing element (PE) - A PE contains a microprocessor, local memory, and support circuitry.

Control option (C option) - The C option is part of the support circuitry; it is the interface between the microprocessor, the interconnect network, and memory.

Network router option (R option) - The R option is the interface between the PE and the interconnect network.

I option - The I option performs I/O transfers between the nodes in the CRAY T3E system and the GigaRing™ option.

GigaRing option - The GigaRing option is the interface between the I option and the GigaRing channel.

Memory option (M option) - The support circuitry contains four M options; each M option controls the reads and writes for two banks of memory.

Clock Circuitry

The CRAY T3E system uses three clocks: the system functional clock (NCLK), the boundary scan clock (TCLK), and the GigaRing clock (XCLK). The NCLK provides a 13.3-nanosecond (ns) clock signal to the options with the exception of the GigaRing options. The TCLK provides a variable clock signal (determined by a parameter of the boundary scan test) to the boundary scan logic that is located within the options. The XCLK provides an 8.0-ns clock signal to the GigaRing options.

The air-cooled system and the liquid-cooled system use the same clock module; this module consists of one printed circuit board (PCB) that contains master clock circuitry (refer to the circuitry above the dotted line in Figure 2) and slave circuitry. The master clock circuitry consists of four oscillators (slow, normal, fast, and GigaRing) and fanout circuitry. The slave clock circuitry consists of fanout circuitry.

For a liquid-cooled system that contains eight cabinets, the master clock circuitry performs a 1-to-8 fanout of the clock signals to itself (cabinet 0) and to the other cabinets within the system (refer to Figure 1). The slave clock circuitry receives the clock signals from the master clock circuitry and performs a 1-to-68 fanout of the clock signal to all of the PCBs within the cabinet.

For an air-cooled system that contains six cabinets, the master clock circuitry also performs a 1-to-8 fanout of the clock signals. Using 2 of the 8 copies, the master clock circuitry sends the clock signal to itself (cabinet 0) and to cabinet 3. The slave clock circuitry of cabinet 0 receives the clock signal from the master clock circuitry and performs a fanout of the clock signal to all of the PCBs within cabinets 0 through 2. The slave clock circuitry of cabinet 3 receives the clock signal from the master clock circuitry and performs a fanout of the clock signal to all of the PCBs within cabinets 3 through 5.

Figure 1. Clock Distribution

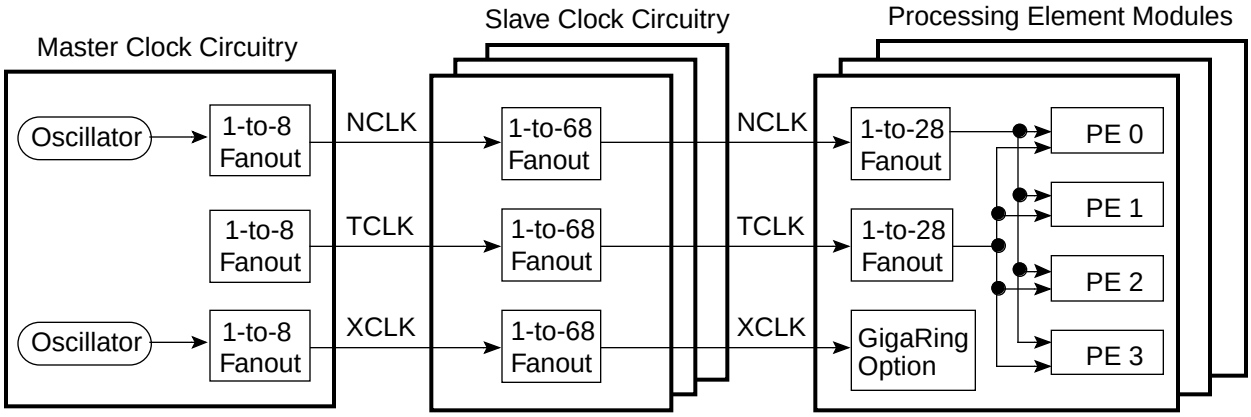
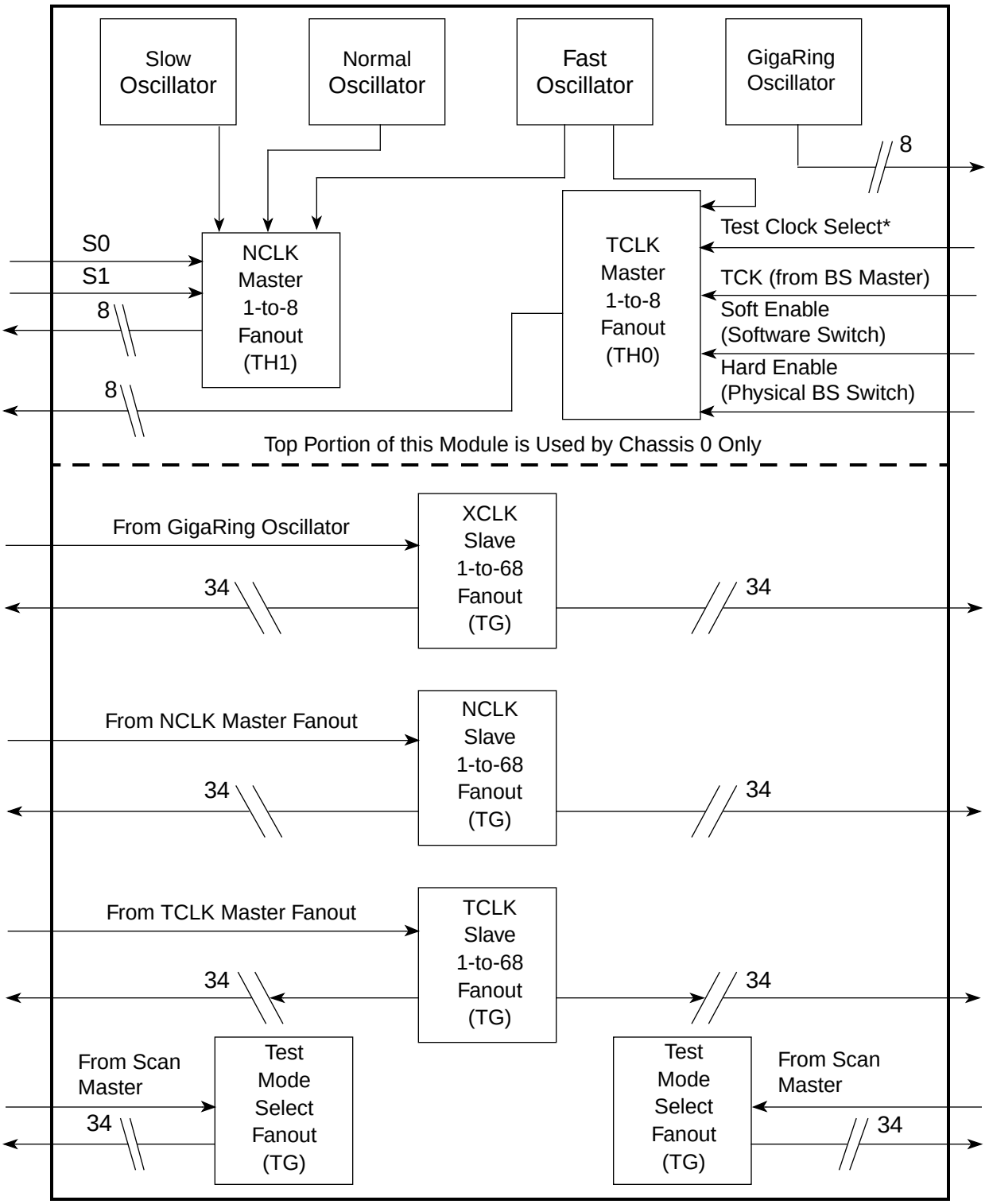


Figure 2. Clock Module

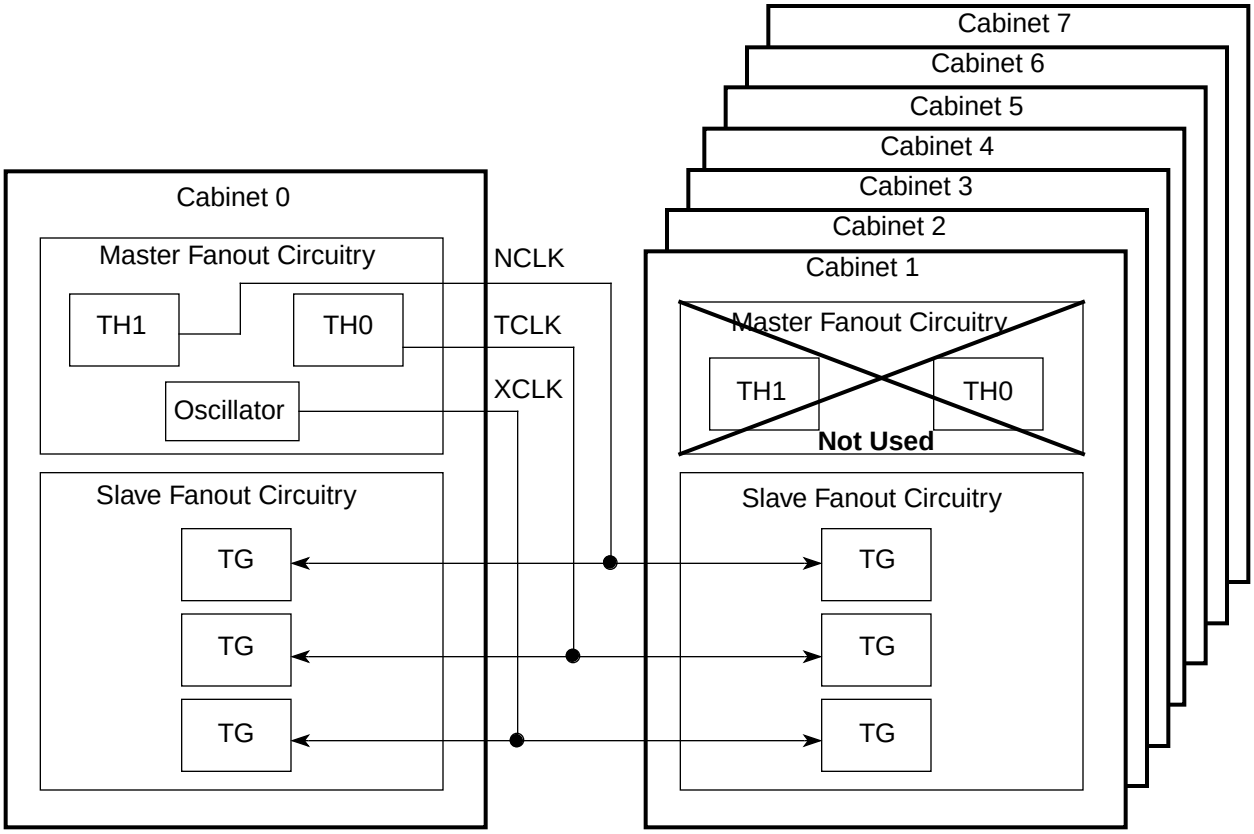


*The Test Clock Select signal selects either the test clock from the boundary scan master or the fast oscillator.

In a liquid-cooled system, each cabinet contains one clock module. Cabinet 0 uses both the master clock circuitry and the slave clock circuitry of the clock module (refer to Figure 3). All of the other cabinets within the system use only the slave clock circuitry.

In an air-cooled system, cabinets 0 and 3 contain the clock module. Cabinet 0 uses both the master clock circuitry and the slave clock circuitry of the clock module. Cabinet 3 uses only the slave clock circuitry.

Figure 3. Master and Slave Fanout Circuitry



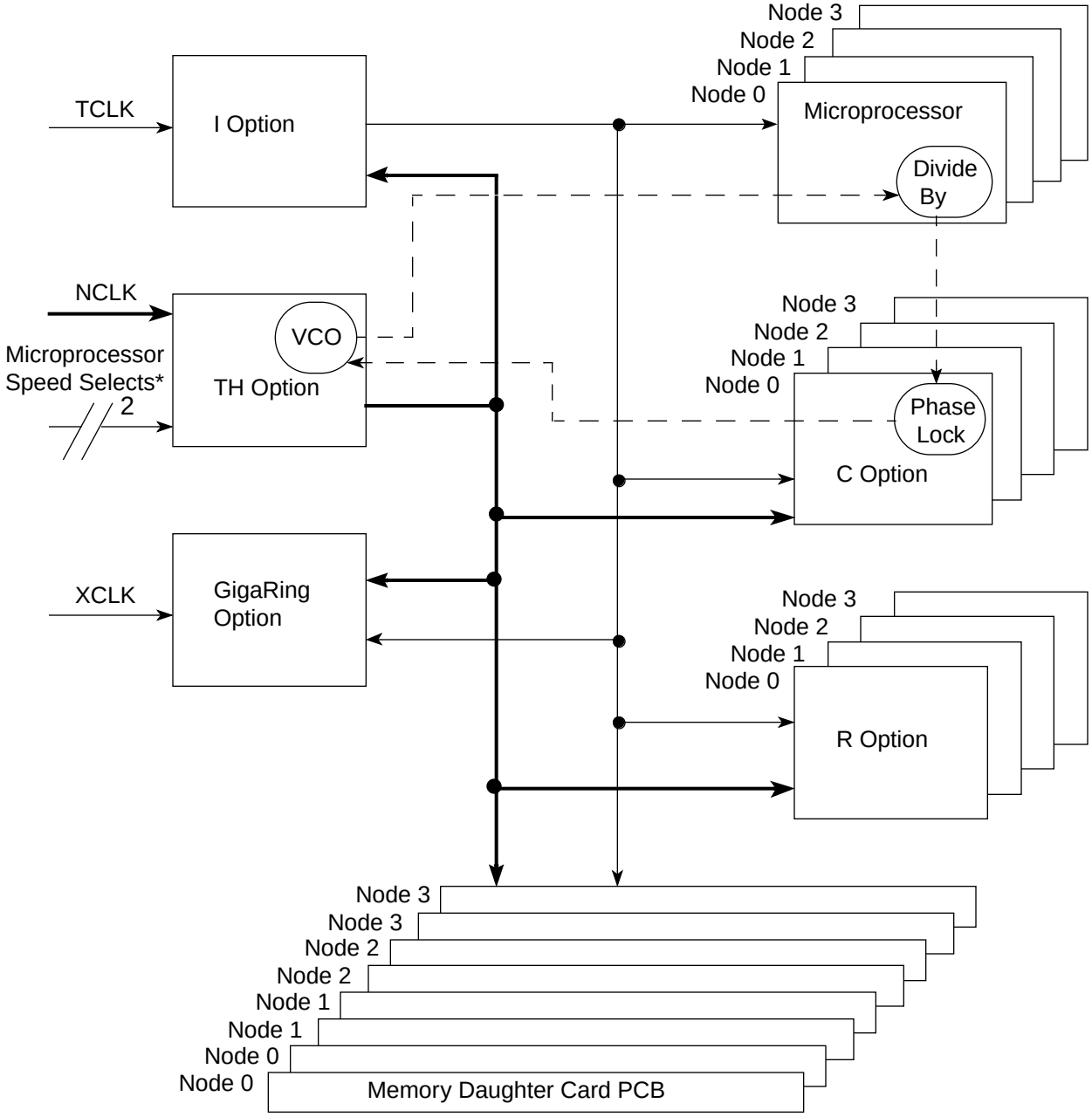
On the PCB, the I option fans out the TCLK (refer to Figure 4).

NOTE: The TCLK is only present when the CRAY T3E system is performing boundary scan operations.

The TH option fans out the NCLK to the C, R, I, and M options. The TH option also provides a clock signal (VCO) to the microprocessors. The microprocessors have a divide circuit (divide by 1 or divide by 2) that produces a clock, which the microprocessor uses internally. Each microprocessor sends a copy of its internal clock signal to its local C option. The C options phase lock the clock signals and send the signals to the TH option.

The GigaRing option receives the XCLK signal.

Figure 4. Clock Distribution on a Printed Circuit Board



* The Microprocessor Speed Select signals come from the PCB jumper blocks.

Boundary Scan

Boundary scan verifies the connections between cabinets, modules, and options in the CRAY T3E system. You may run the boundary scan test to verify the integrity of the system after a failure that caused the operating system to fail, or after you complete a repair procedure. You can initiate the boundary scan test by using command line syntax or t3ems. Boundary scan requires control of the system; therefore, you cannot run the boundary scan test simultaneously with the operating system.

An external device (usually the system workstation) initiates the boundary scan test by sending a write-scan request packet to the scan master I/O controller. There is only one scan master I/O controller per CRAY T3E system. The scan master is located in slot 1 of chassis 0. (For liquid-cooled systems, the scan master is located on PCB A, which is seated in the lower position of the module slot.)

The write-scan request packet contains a command and data. The command instructs the I/O controller to use the data from the packet as test vectors for the boundary scan test. The I/O controller sends the data from the packet to the boundary scan logic one bit at a time. The data bits are propagated through the boundary scan logic, where they test for continuity between the options and the modules. When the I/O controller sends the last bit to the boundary scan logic, the I/O controller sends a write-scan response packet to the external device.

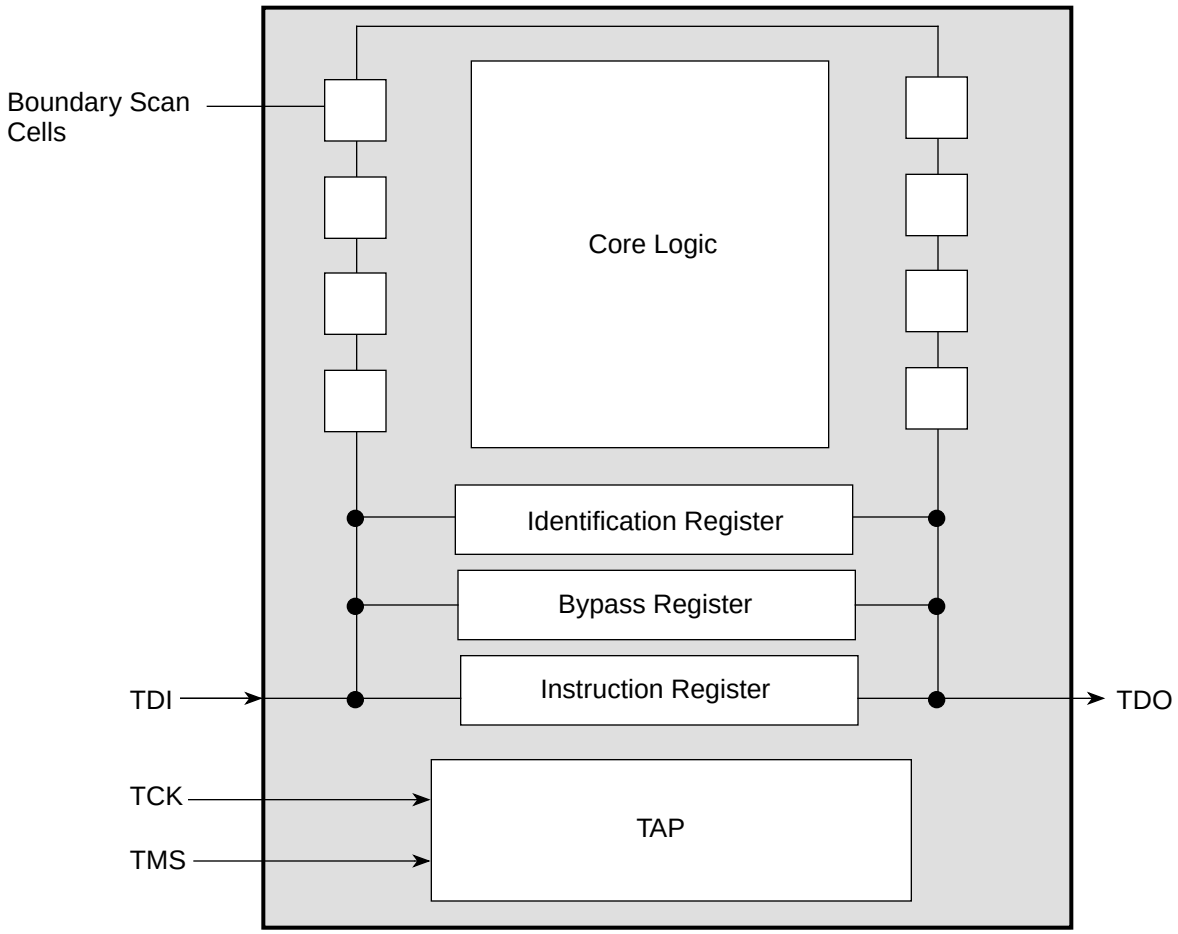
The scan master I/O controller buffers the results of the boundary scan test. To view the results, the external device sends a read-scan request packet to the scan master I/O controller. After receiving the request, the scan master I/O controller retrieves the test results from the buffer, places the results in a read-scan response packet, and sends the read-scan response packet to the external device.

Components

Each option in the CRAY T3E system contains boundary scan logic. This logic consists of the test access port (TAP), an instruction register, a bypass register, an identification register, and boundary scan cells (refer to Figure 5).

The boundary scan logic requires four signal pins: test data input (TDI), test data output (TDO), test clock (TCK), and test mode select (TMS). The TDI pin inputs data serially. The TDO pin outputs data serially. The TCK pin inputs a clock signal that clocks the TAP and the internal scan chains during a scan operation. The TMS pin controls the state of the TAP.

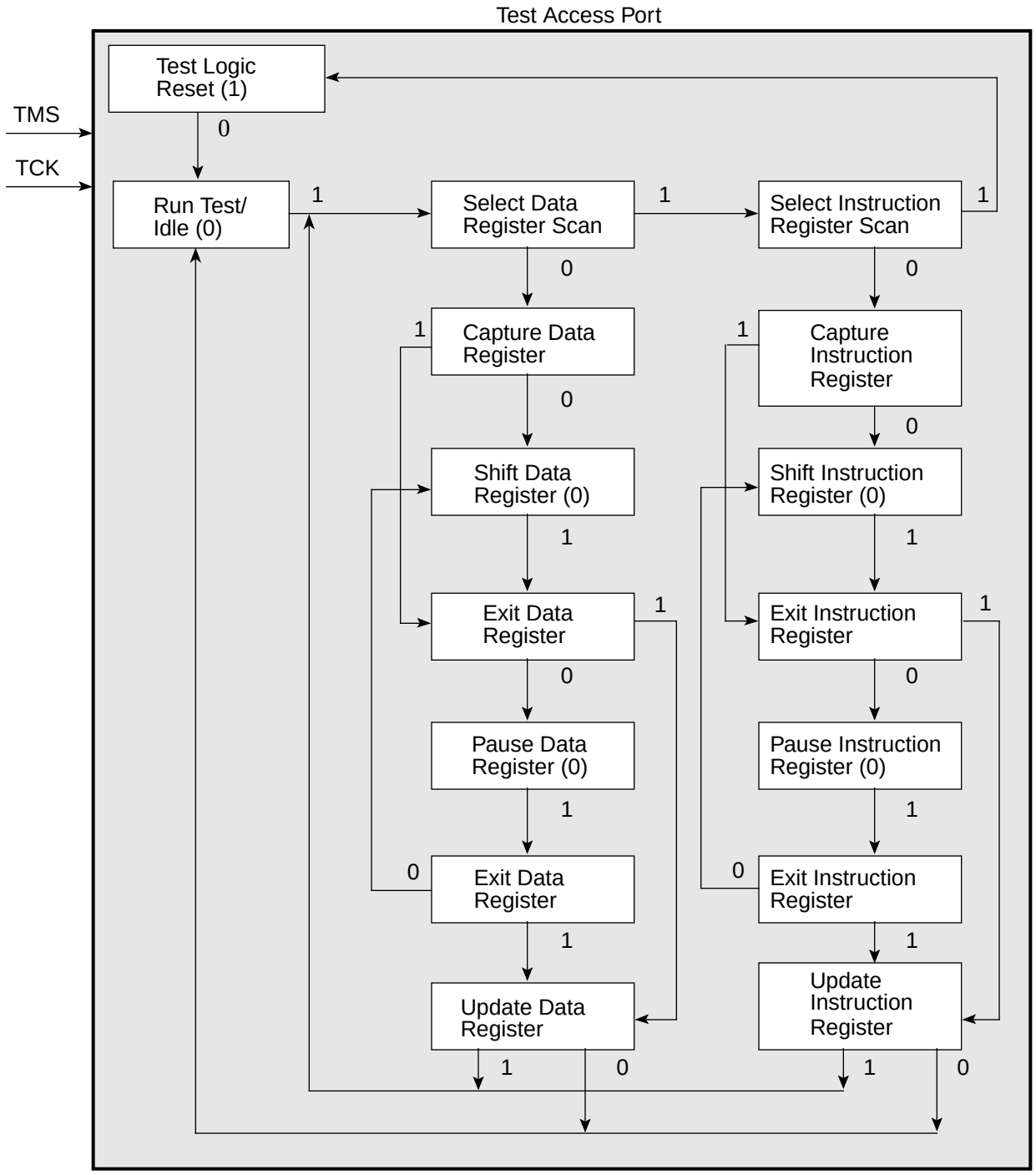
Figure 5. Boundary Scan Logic



Test Access Port (TAP)

The TAP controls the instruction register, the bypass register, the identification register, and the boundary scan cells. The TAP can be in 1 of 16 states (refer to Figure 6): idle, reset, data scan (requires 7 states), and instruction scan (requires 7 states). The boundary scan test changes the state of the TAP using the TMS and the TCK signals; the TAP changes state during the falling edge of the TCK signal.

Figure 6. States of the TAP

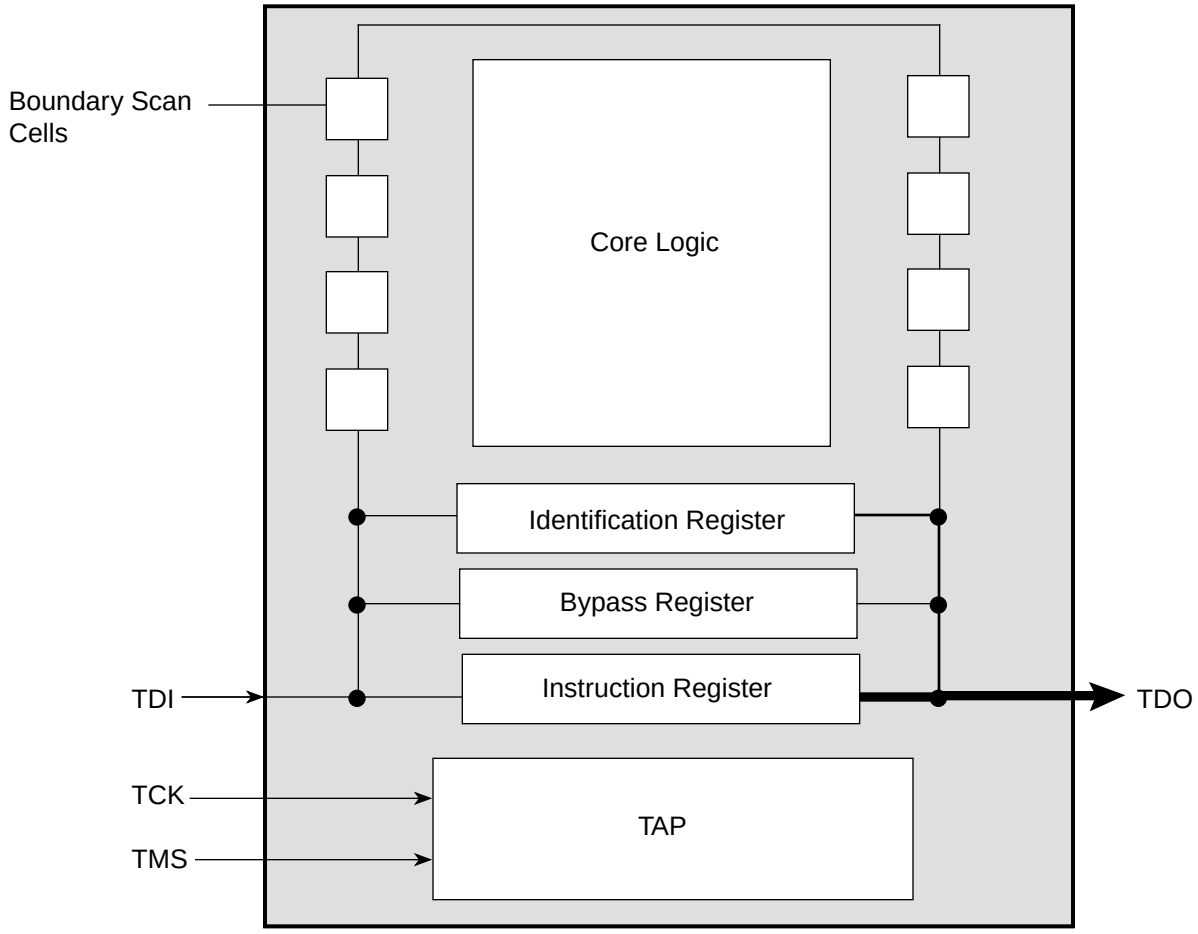


NOTE: The value(s) shown adjacent to each box represents the TMS signal level at the time of a falling edge of the TCK signal.

Instruction Register

The instruction register receives, holds, and decodes boundary scan instructions. The instructions indicate how the registers are connected to the TDI and TDO pins. For example, when the boundary scan test instructs the boundary scan logic to read the instruction register, the TDO pin receives data from the instruction register rather than from the boundary scan cells, the identification register, or the bypass register (refer to Figure 7).

Figure 7. Reading the Instruction Register

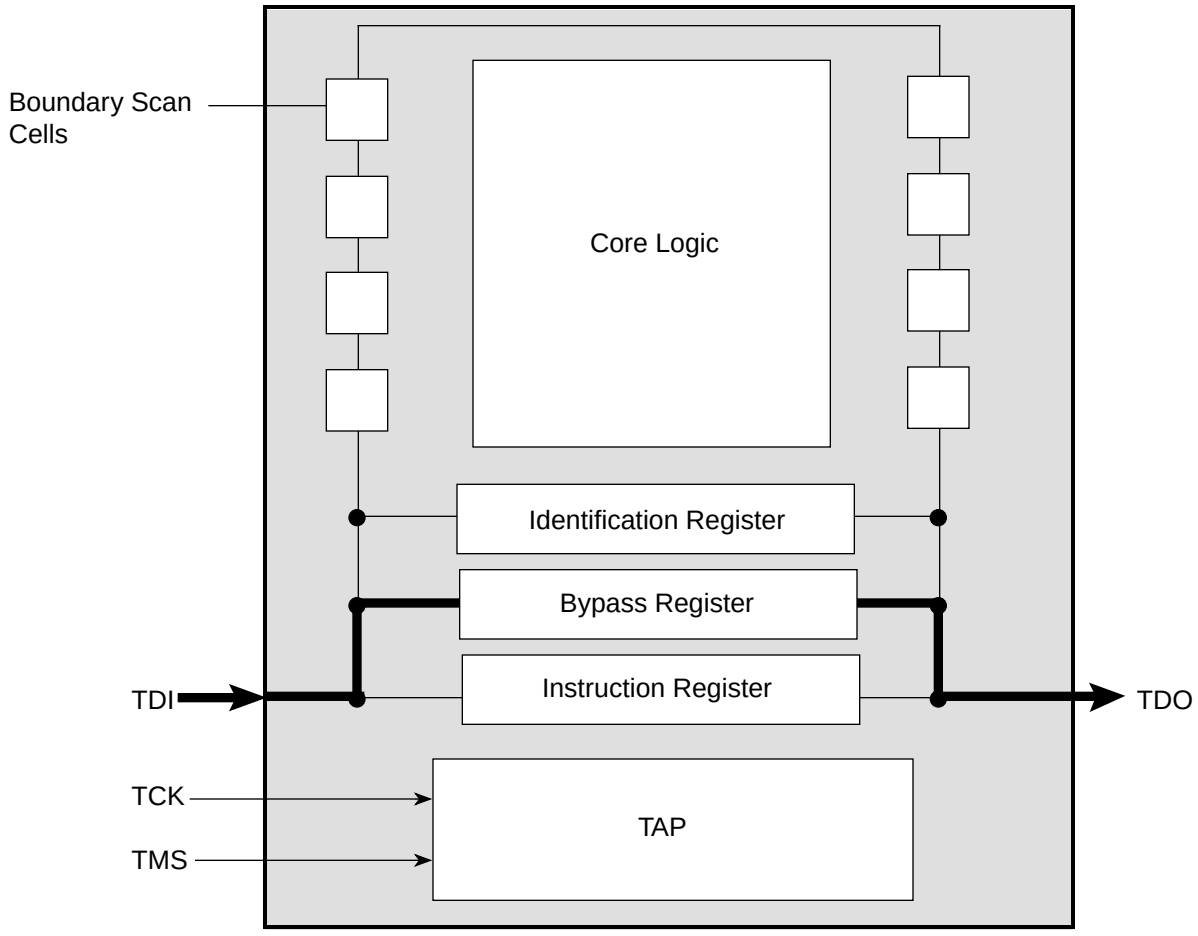


The options of the CRAY T3E system have a 5-bit instruction register; the GigaRing option has a 10-bit instruction register. When the boundary scan test is initiated, it first tests the scan chain by reading the pattern from the instruction register. For CRAY T3E options, this pattern is 10000. For the GigaRing option, the pattern is 1000000100.

Bypass Register

The bypass register routes signals from the TDI pin to the TDO pin; the signals do not flow through the boundary scan cells (refer to Figure 8).

Figure 8. Boundary Scan Path Using the Bypass Register

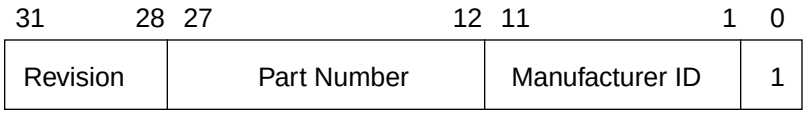


Identification Register

The identification register holds 32 bits of information that specifies the manufacturer of the option, the part number of the option, and the revision of the option (refer to Figure 9). The least significant bit must be a 1.

The identification register can also be used to shift in and shift out user-defined information.

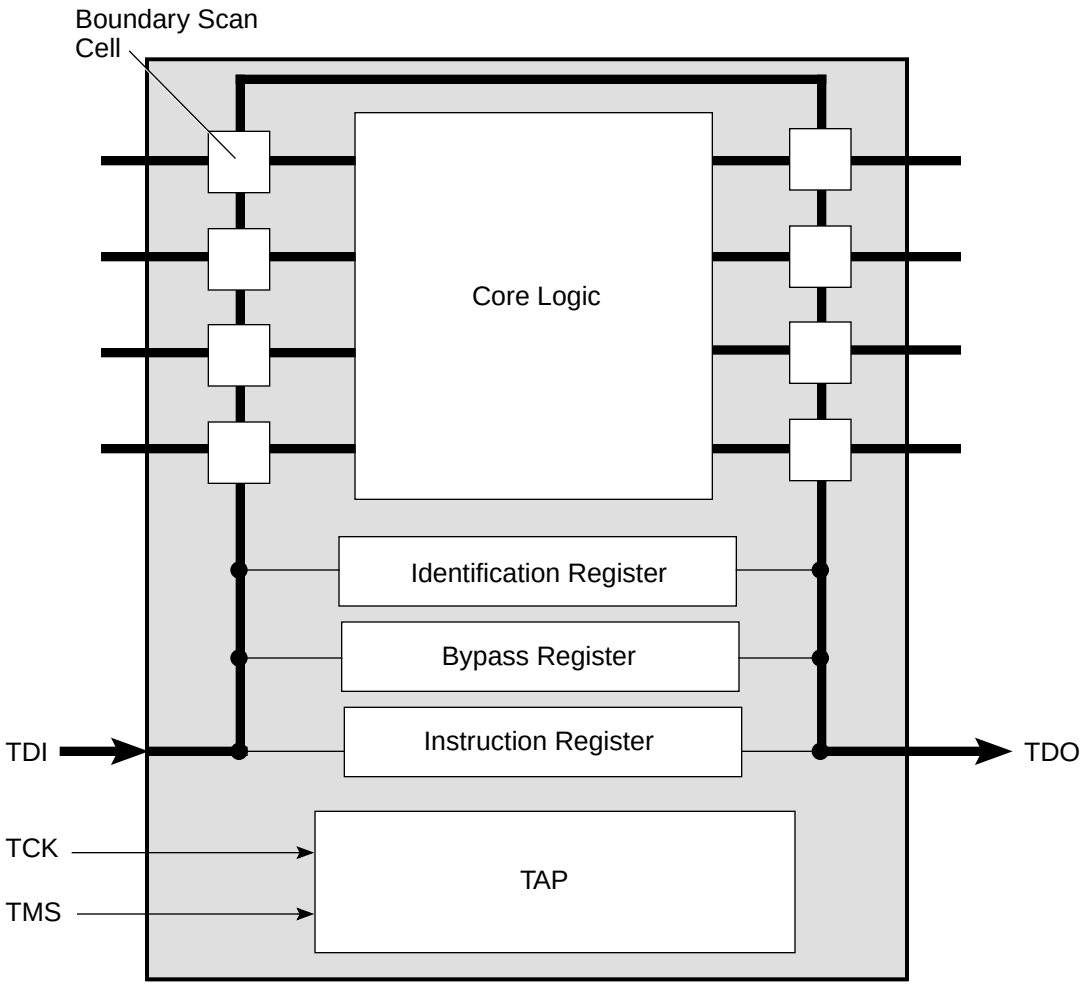
Figure 9. Identification Register



Boundary Scan Cells

The boundary scan cells capture data from the TDI pin, the option pins, and the core logic (refer to Figure 10). Likewise, the boundary scan cells transfer data to the TDO pin, the option pins, and the core logic. There is one boundary scan cell per input/output option pin.

Figure 10. Boundary Scan Cell Path



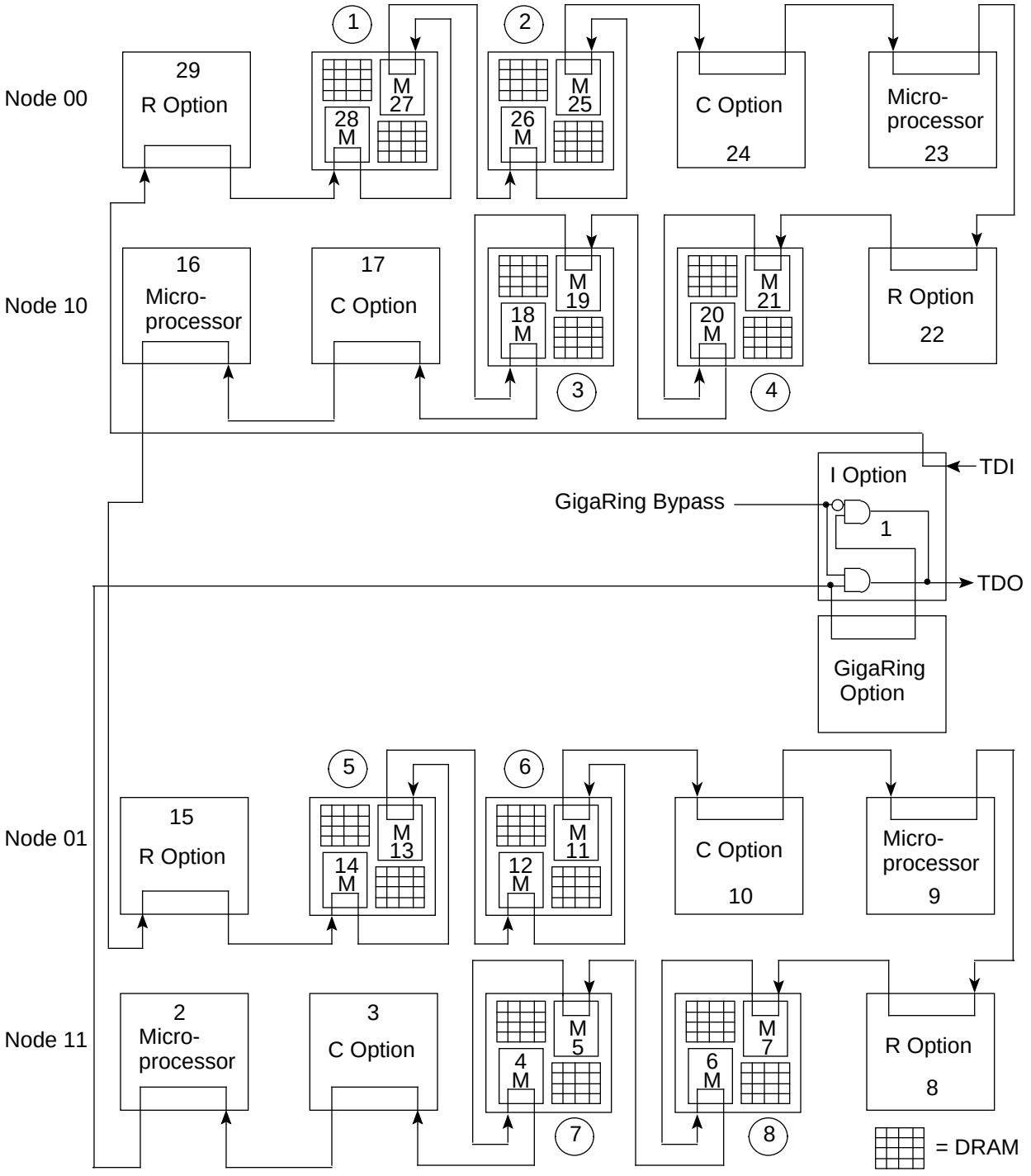
Scan Chain

A scan chain is the path that the test data takes through a cabinet. Within each PCB, the scan chain connects the boundary scan logic of the four PEs that reside on the PCB (refer to Figure 11 and Figure 12).

When the PCB receives the boundary scan signal, the boundary scan signal enters the I option via the TDI pin and passes through a single gate that is not part of the boundary scan logic. From this gate, the signal leaves the I option and enters the R option of node 0 via the TDI pin. The signal passes through the R option's boundary scan logic, leaves the R option via the TDO pin, and enters an M option via the TDI pin. The signal continues to transfer through the options in the order shown in Figure 11 and Figure 12.

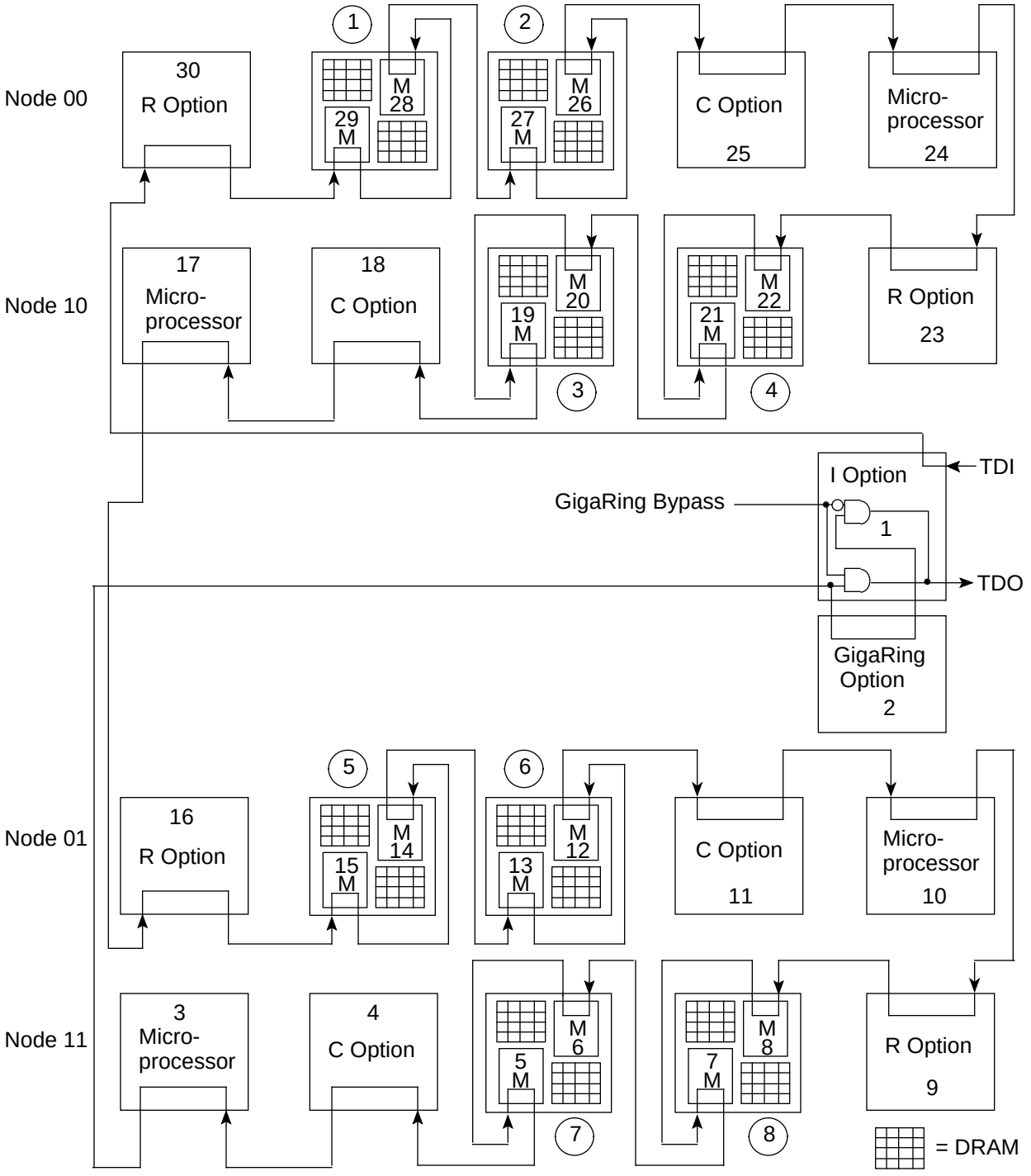
When the boundary scan signal has passed through all four of the PEs on the PCB (leaves the microprocessor of node 3 via the TDO pin), the signal enters the I option. The I option passes the signal to the GigaRing option. The I option also determines whether the GigaRing option is included in the scan chain by using a signal from a GigaRing bypass jumper; the GigaRing bypass jumper is inserted on the PCB to bypass the GigaRing option. When the GigaRing option is included in the scan chain, the I option outputs the boundary scan signal from the GigaRing option via the TDO pin. When the GigaRing option is not included in the scan chain, the I option outputs the boundary scan signal from the microprocessor of node 3. From the I option, the boundary scan signal leaves the PCB and transfers to the next PCB in the scan chain.

Figure 11. Scan Chain Within a PCB (GigaRing Bypass Jumper Installed)



NOTE: A number in a circle identifies a daughter card.

Figure 12. Scan Chain Within a PCB (GigaRing Bypass Jumper Removed)



NOTE: A number in a circle identifies a daughter card.

Boundary Scan Test Sequence

The CRAY T3E boundary scan test can perform the following functions:

1. Read the configuration file to determine the number of cabinets in the system, the number of modules per cabinet, and wiring data (X, Y, and Z connections).

2. Verify that the TAP circuitry on each board is operational. To do this, the boundary scan test reads the instruction registers and verifies that this information is correct.

3. Read the printed circuit board revisions from the jumper on each PCB.

4. Generate test vectors and reference files. The boundary scan test regenerates the test vectors when you add or remove a module and the new module has a different boundary scan revision. The boundary scan revision consists of the following information:

   - Board netlist revision
   - Microprocessor revision
   - GigaRing bypass jumper

   The boundary scan test also regenerates the test vectors when you replace a module with a module that contains a GigaRing option that is physically located on the opposite PCB. For example, when you remove a module that contains the GigaRing option on the upper PCB and replace it with a module that contains the GigaRing option on the lower PCB, the boundary scan test regenerates the test vectors.

5. Verify that the boundary scan registers are operational by scanning in and scanning out test patterns without updating the output pins.

   NOTE: At this point, the boundary scan cells are loaded with a test pattern.

6. Verify that the interconnects (cables, wires, connectors, and foils) between the cabinets, modules, and options are operational.

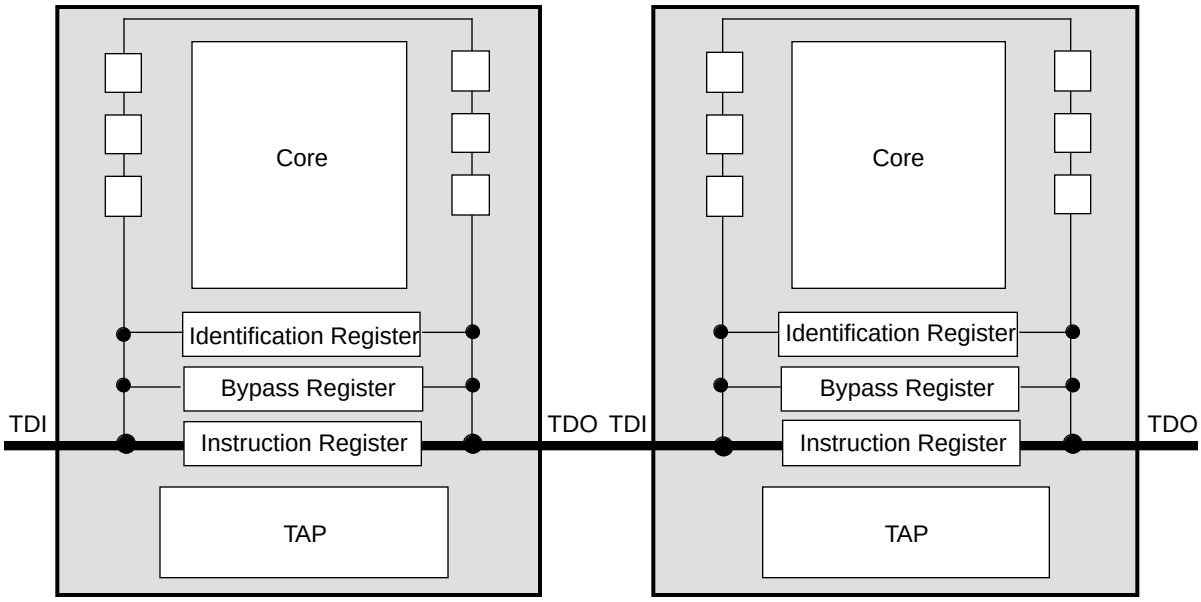
7. Verify the results of the scan. When there is an error, the test displays the error information (failing net).

NOTE: You select the functions that the boundary scan test performs when you initiate the boundary scan test (refer to the description of the `-t` command line option or the test select in the T3EMS Scan Tool Options window).

To verify that the interconnects between the cabinets, modules, and options are operational (Step 6), the boundary scan test uses the extest instruction that allows the boundary scan logic to scan in and scan out test patterns (refer to Figure 13 and Figure 14). The test patterns may include a 1's pattern, a 0's pattern, a bridging pattern, and a complemented bridging pattern.

Figure 13. extest Instruction

1. When the boundary scan test loads the extest instruction into the instruction register, the boundary scan logic enters the test mode.
   The extest instruction consists of three stages: capture, shift, and update.



2. The capture stage of the extest instruction causes all of the options within a scan chain to capture (latch) data from the input pins.

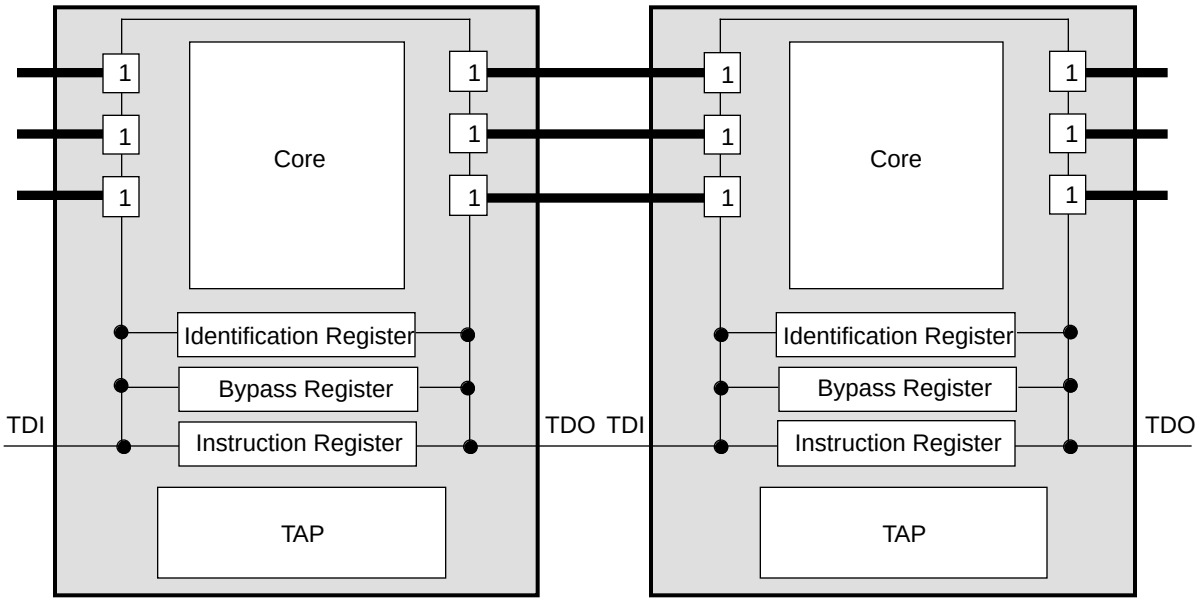
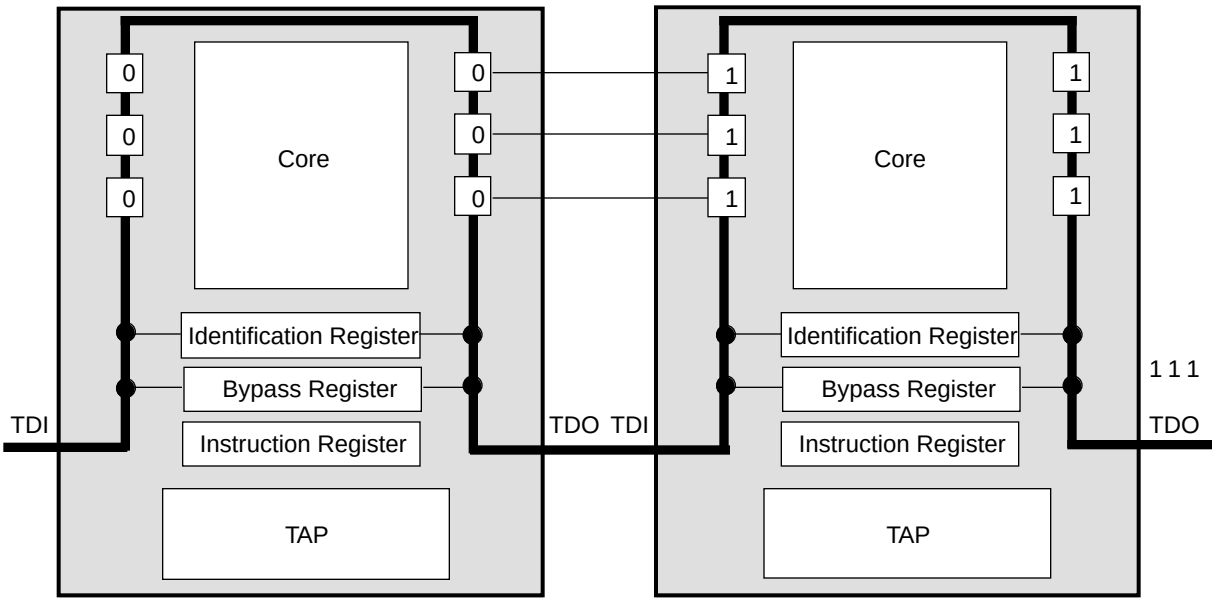


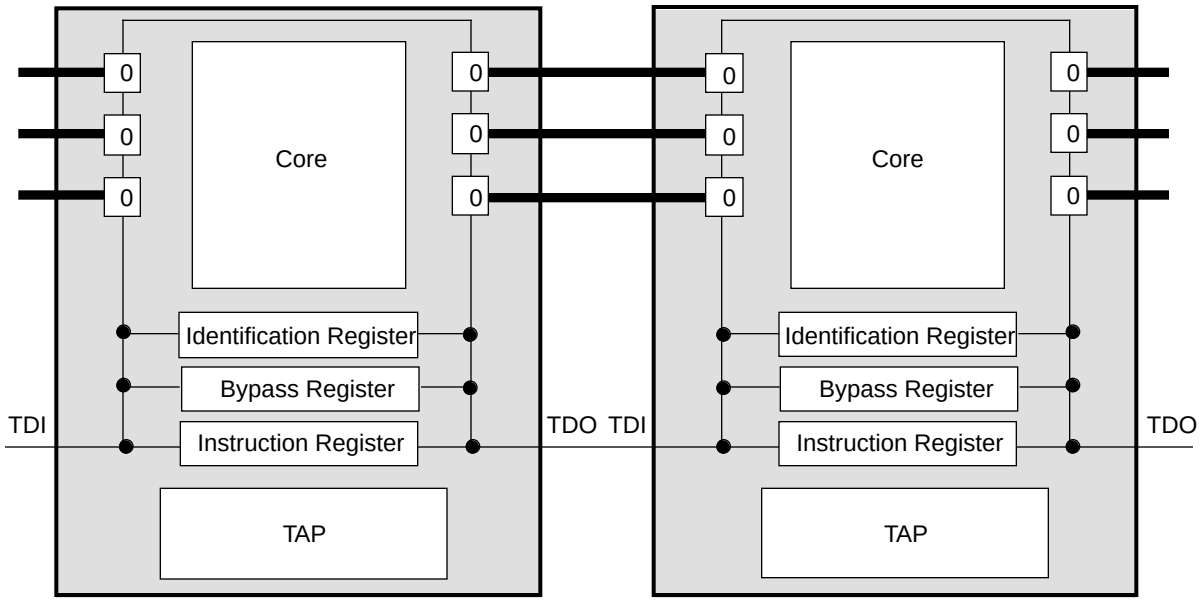
Figure 14. extest Instruction (continued)

3. The shift stage of the extest instruction causes the boundary scan logic to shift out the old test pattern through the entire scan chain and shift in a new test pattern.

   The scan master sends the old test pattern to the SWS. Software running on the SWS compares the test pattern to an expected test pattern to determine whether there are any errors.



4. Like the capture stage, the update stage of the extest instruction causes the options to latch in the new test pattern.



5. Repeat Steps 3 and 4 for all of the test patterns.

A liquid-cooled system has two scan chains per cabinet: scan chain N (N = 0, 2, 4, 6, 8, 10, 12, and 14) scans the upper PCBs within the cabinet and scan chain N+1 scans the lower PCBs (refer to Figure 15). The scan master starts the scan chain by using its TDIF pins to fan out the boundary scan signals; the TDIF0 pin fans out the signal to the TDIM pins on the upper PCB of the module in slot 1 and the TDIF1 pin fans out the signal to the TDIM pins on the lower PCB of the module in slot 1. The boundary scan signal passes through the PCBs and leaves via their TDOM pins. The TDOM pin of each upper or lower PCB connects to the TDIM pin of the PCB in the same position on the module directly above it (refer to Figure 16). This TDOM-to-TDIM connection creates a daisy chain from the module in slot 1 to the module in slot 35.

NOTE: The TDOM pin on the top PCB of each chain passes through a one-clock line driver (referred to as Repeat I and Repeat O in Figure 16) before returning to the TDOF pin of the scan master.

The scan master sends the test pattern back to the SWS. The boundary scan test executing on the SWS verifies the result. When an error occurs, the test displays the failing net.

When there is more than one cabinet in the system, the scan master sends the test data to the other cabinets (refer to Figure 17). Figure 18 illustrates how the test data from more than one cabinet returns to the scan master.

Figure 15. Scan Chains for a Liquid-cooled System

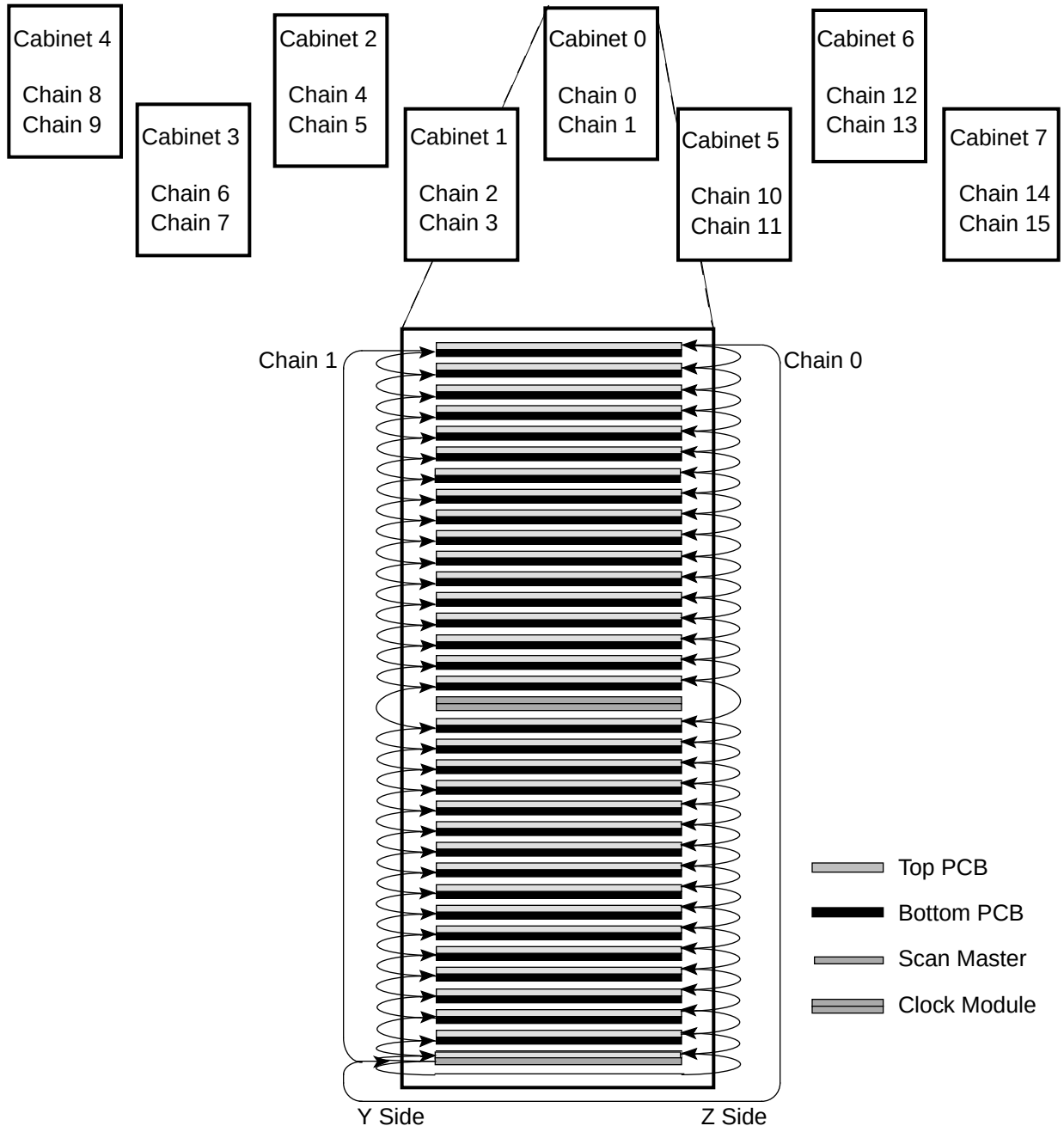
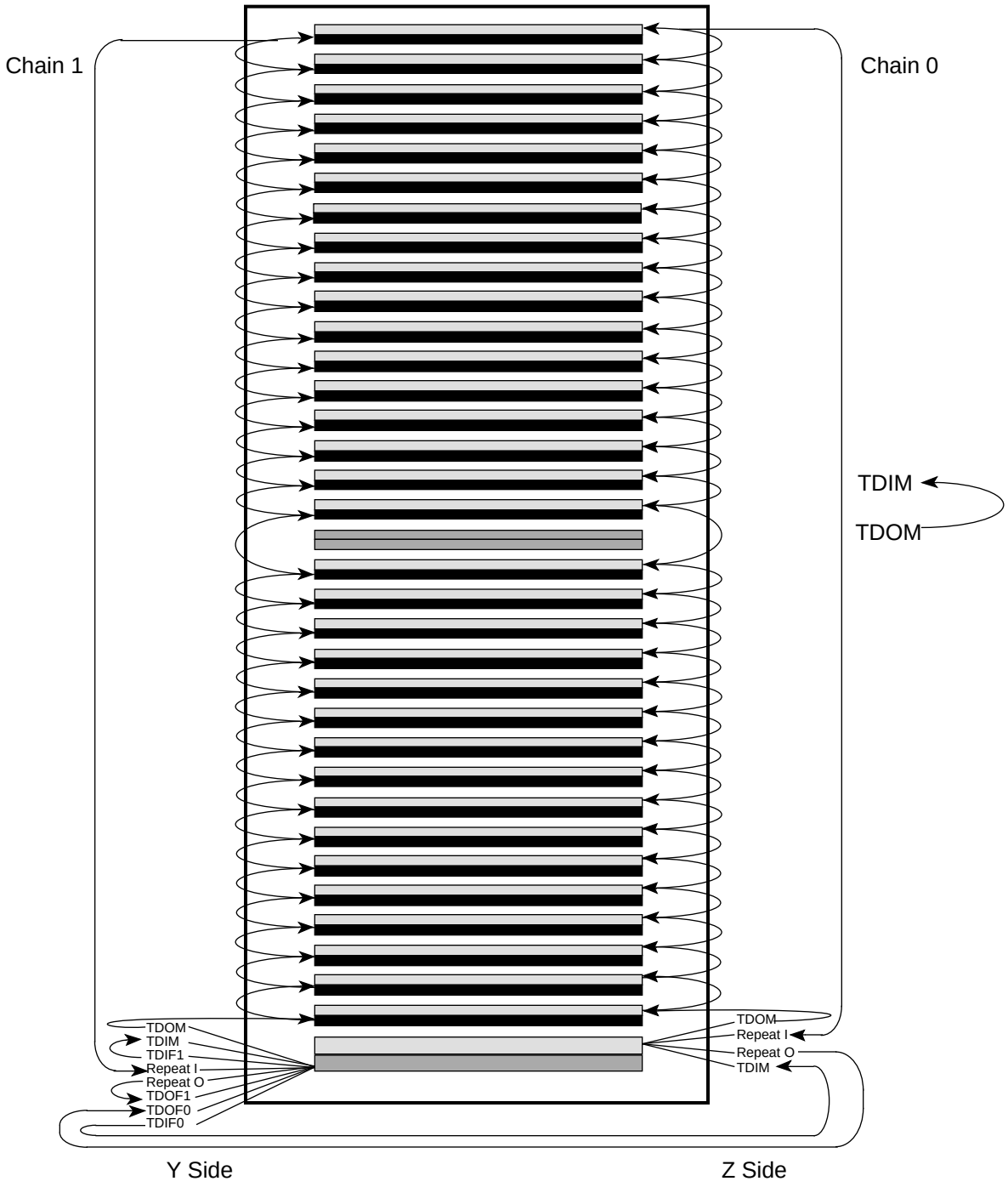


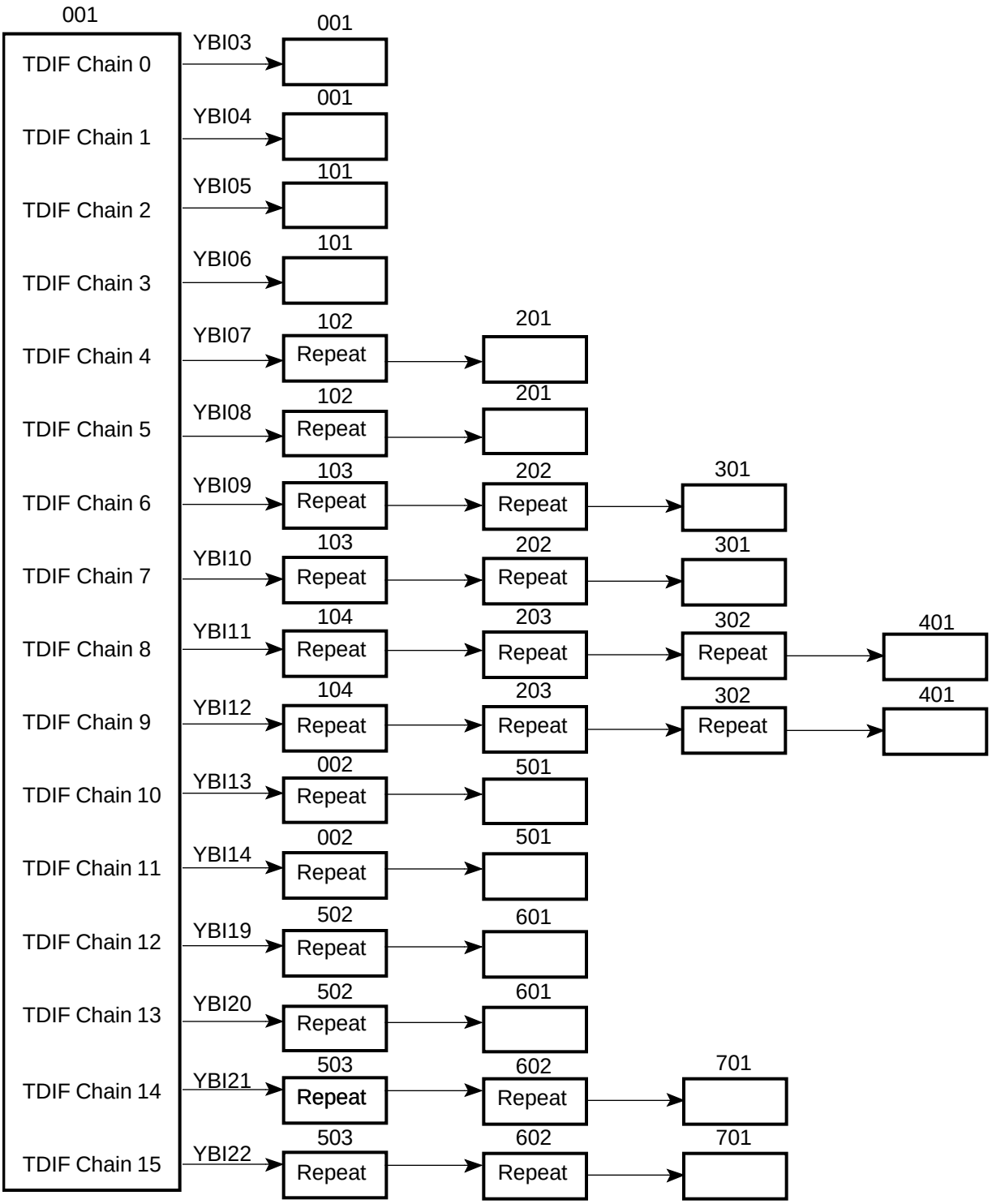
Figure 16. TDOM-to-TDIM Connection



TDOM = Test Data Out Module
TDIM = Test Data In Module
TDOF = Test Data Out Frame (Original Signal)
TDIF = Test Data In Frame

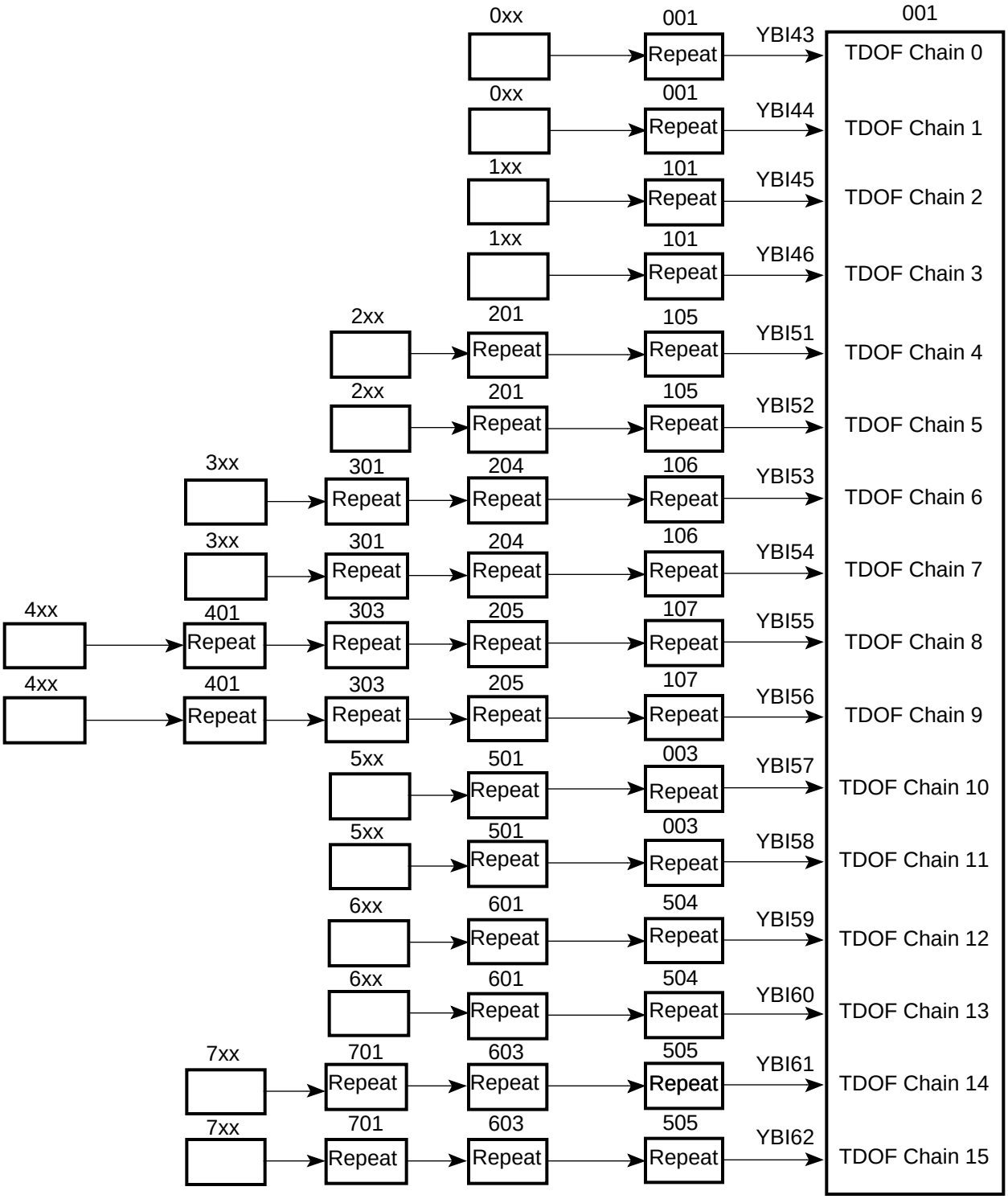
Upper PCB
Lower PCB
Scan Master
Clock Module

Figure 17. Distribution of Test Data In (TDIF) to the Cabinets within a System



NOTE: The three-digit number indicates the chassis and the slot. For example, 602 indicates chassis 6, slot 02. YBI*xx* indicates a connector.

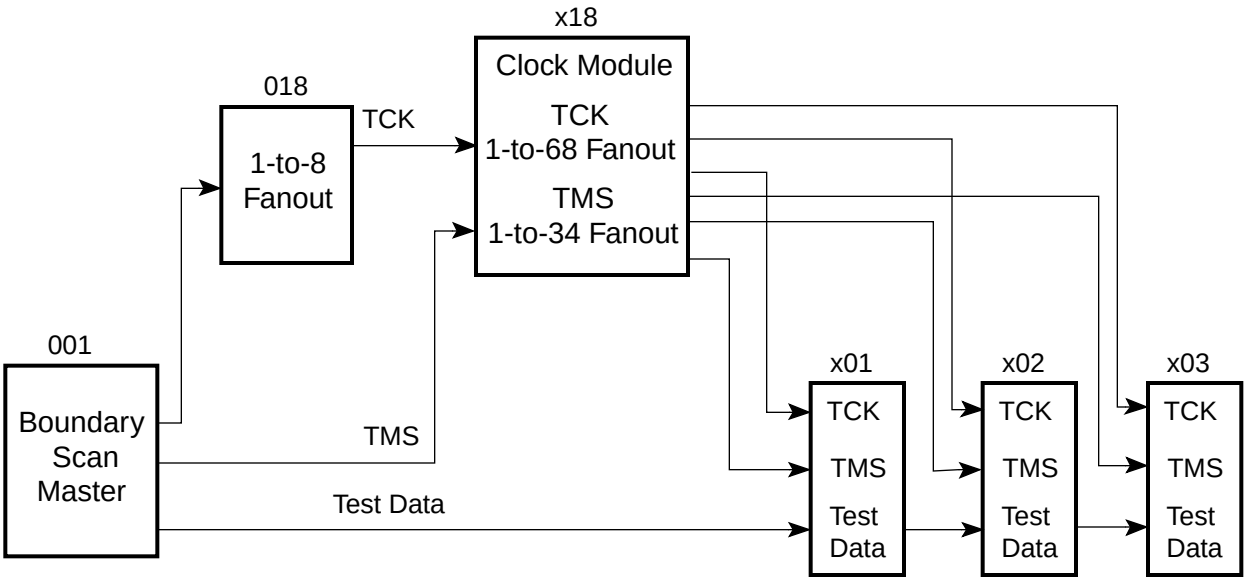
Figure 18. Distribution of Test Data Out to the Boundary Scan Master



NOTE: The three-digit number indicates the chassis and the slot. For example, 603 indicates chassis 6, slot 03. When the slot designator is *xx*, it designates the slot number of the top module in the cabinet. YB*Ixx* indicates a connector.

The scan master also starts the fanout of the test clock signal (TCK) and the test mode select signal (TMS) (refer to Figure 19).

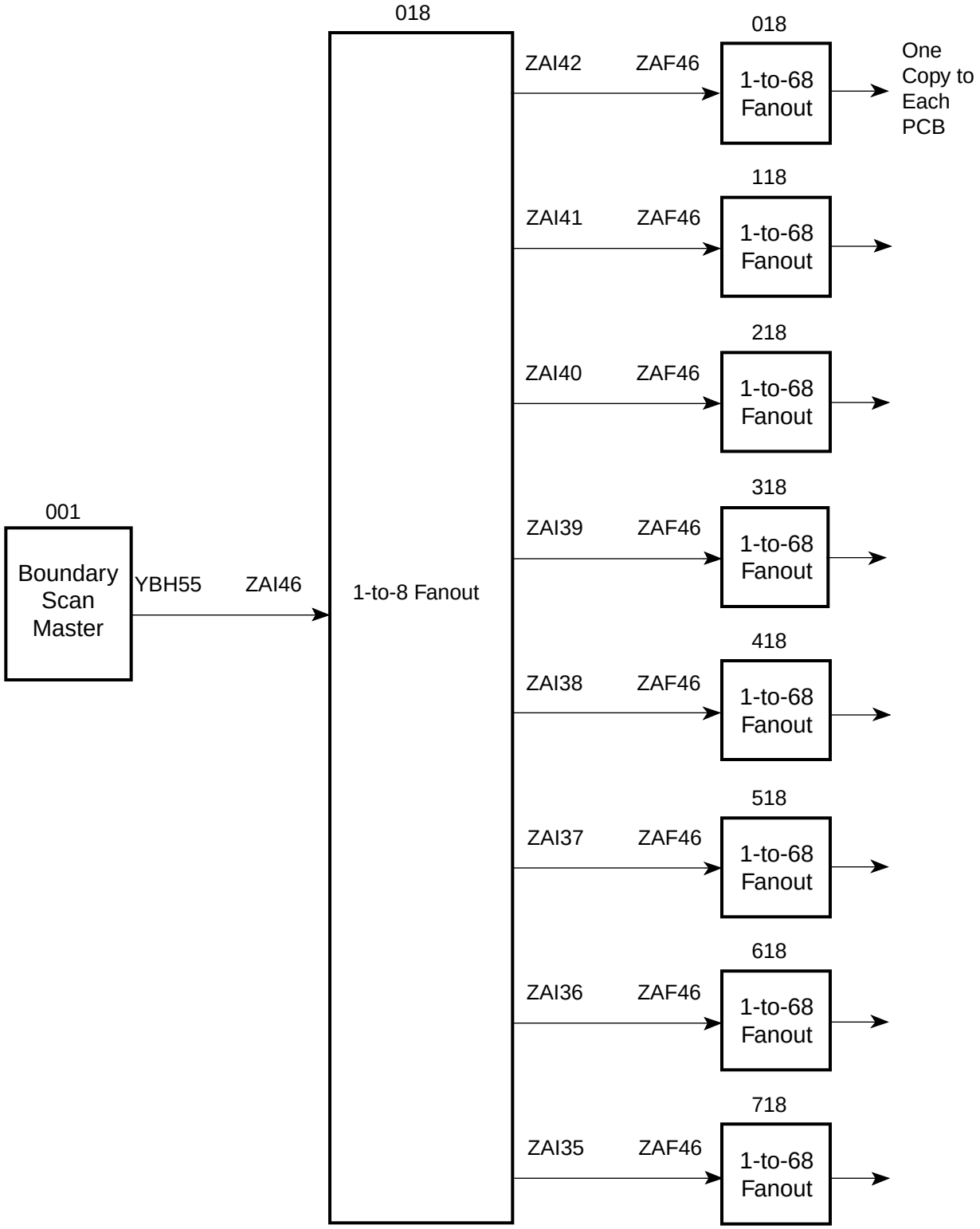
Figure 19. Distribution of the TCK and TMS Signals



NOTE: The three-digit number indicates the chassis and the slot. For example, 001 indicates chassis 0, slot 01. When the chassis designator is *x*, it can be any chassis within the system.

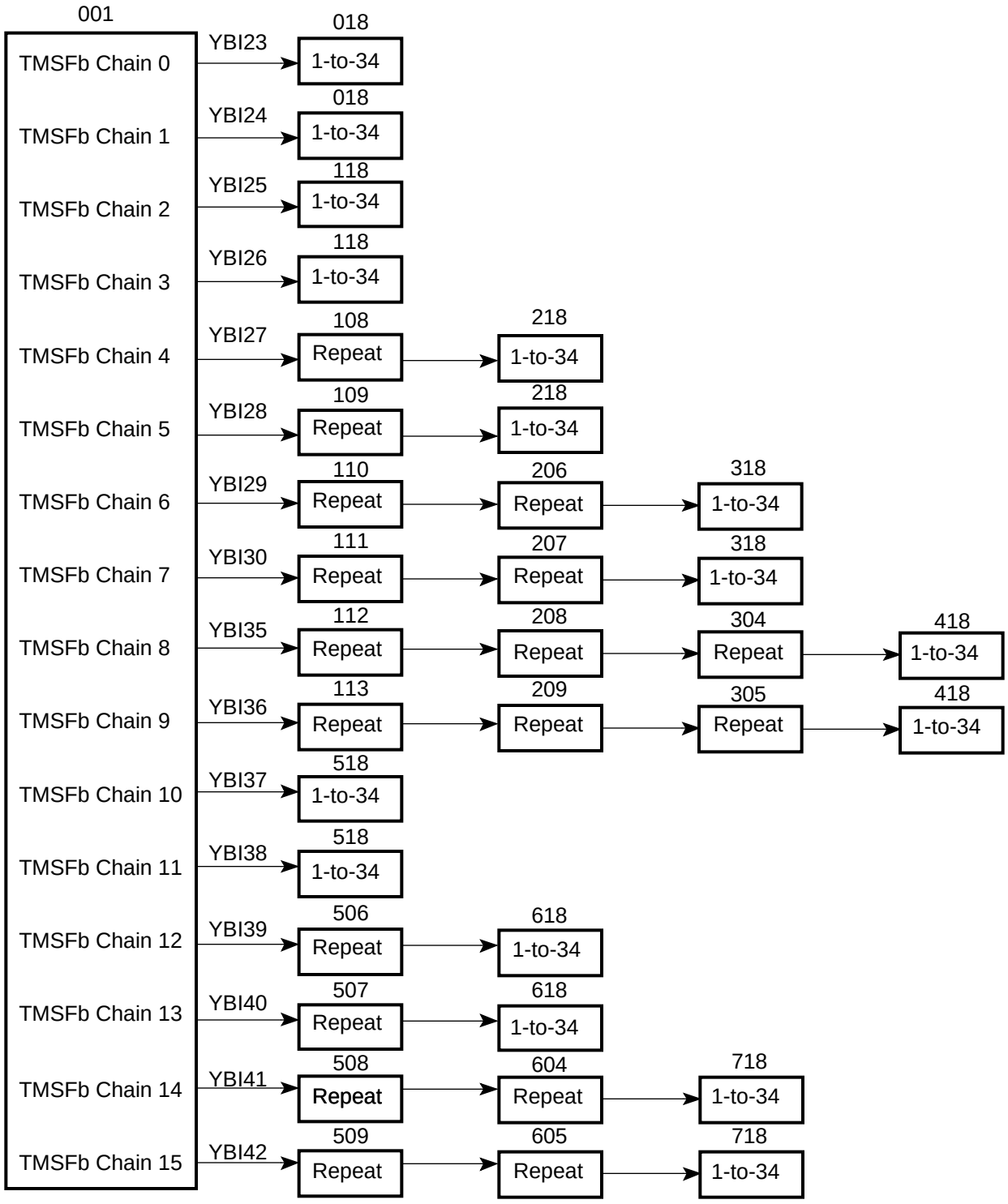
The scan master sends the TCK signal to the clock module of chassis 0. The clock module performs a 1-to-8 fanout of the TCK signal and sends a copy of the signal to the clock module in each cabinet (including itself) (refer to Figure 20). Each clock module performs a 1-to-68 fanout of the TCK signal and sends one copy of the signal to each PCB within the cabinet.

Figure 20. Test Clock (TCK) Fanout



The scan master sends two TMS signals to the clock module in each cabinet: one for scan chain N (upper PCBs) and one for scan chain N+1 (lower PCBs) (refer to Figure 21). For cabinets 2, 3, 4, 6, and 7, the TMS signal passes through a repeat circuit(s) before reaching the clock module. Once the clock module receives the TMS signal, the clock module performs a 1-to-34 fanout of the TMS signal and sends a copy of the signal to the upper PCBs (scan chain N) or lower PCBs (scan chain N+1) in the cabinet.

Figure 21. Test Mode Select (TMS) Fanout



NOTE: The three-digit number indicates the chassis and the slot. For example, 718 indicates chassis 7, slot 18. YBI*xx* indicates a connector.

The CRAY T3E air-cooled system may have one or two scan chains. A CRAY T3E air-cooled system that contains one to three cabinets has one scan chain (refer to Figure 22). An air-cooled system that contains four or more cabinets has two scan chains. For example, in a six-cabinet system, scan chain 0 scans cabinets 0, 1, and 2 and scan chain 1 scans cabinets 3, 4, and 5.

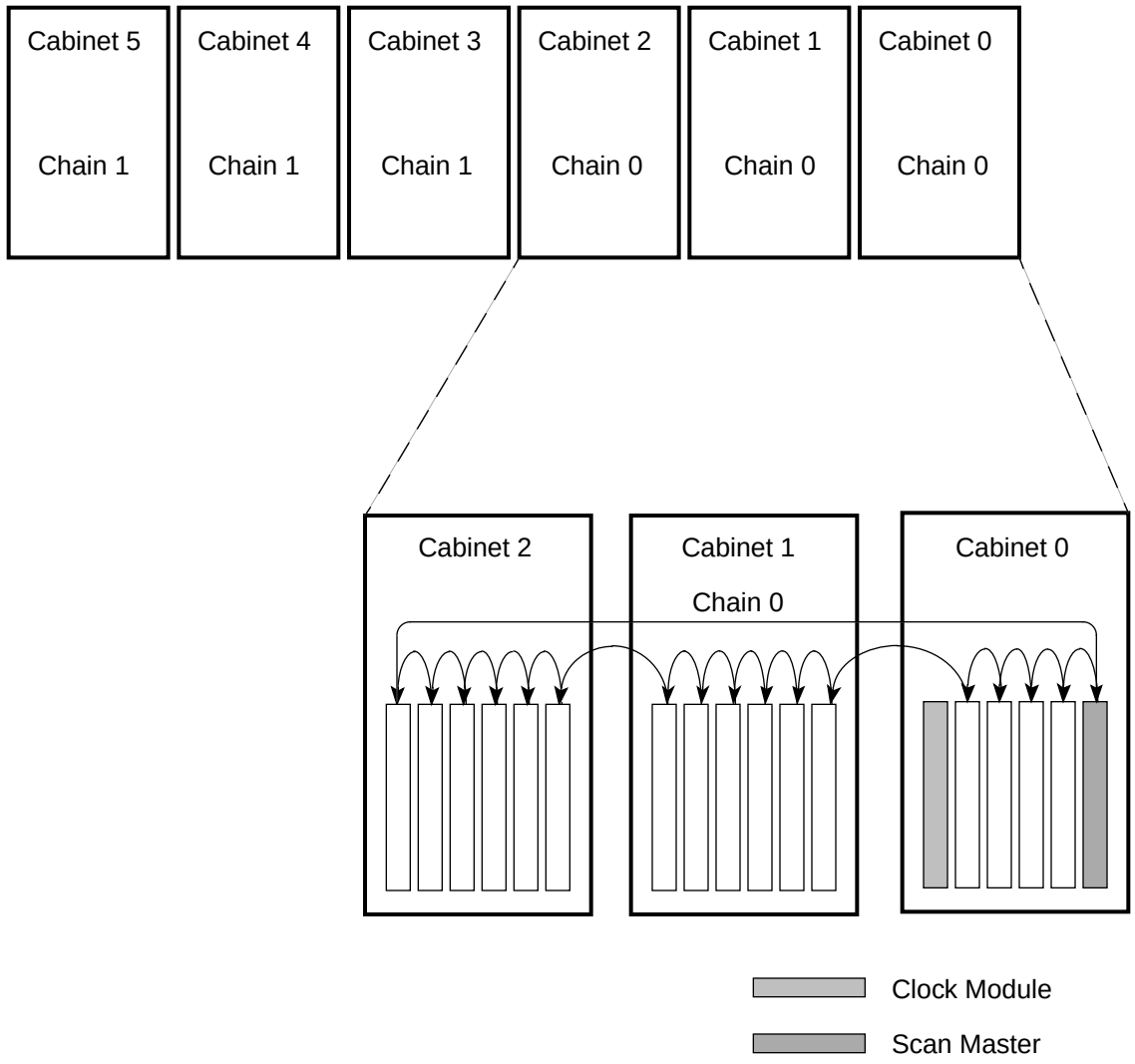
The boundary scan chain starts at the scan master, which is the PE module that resides in slot 1 of cabinet 0 (refer again to Figure 22).

The scan master starts the scan chain by using its TDIF pins to fan out the boundary scan signals; the TDIF0 pin fans out the signal to the TDIM pins of the module in slot 1 of chassis 0 and the TDIF1 pin fans out the signal to the TDIM pins of the module in slot 1 of chassis 3. The boundary scan signal passes through the modules and leaves via their TDOM pins. The TDOM signal of an air-cooled module connects to the TDIM signal of the module that is next to it in the cabinet, with the exception of slot 5 of cabinet 0 and cabinet 3. For example, in an air-cooled system that contains two scan chains, slot 5 of cabinet 0 connects to slot 1 of cabinet 1 (refer again to Figure 22) and slot 5 of cabinet 3 connects to slot 1 of cabinet 4.

NOTE: When an air-cooled system has two scan chains, the TDOM signal from the last processing element module in the scan chain passes through a one-clock line driver (referred to as Repeat I and Repeat O) before returning to the TDOF pin of the scan master. Scan chain 0 uses the driver that is located in slot 1 of cabinet 0 and scan chain 1 uses the driver that is located in slot 1 of cabinet 3.

The scan master sends the test pattern back to the SWS. The boundary scan test executing on the SWS verifies the result. When an error occurs, the test displays the failing net.

Figure 22. Scan Chains for an Air-cooled System



How to Initiate the Boundary Scan Test

You may run the boundary scan test to verify the integrity of the system after a failure that causes the operating system to fail, or after you complete a repair procedure.

Before you initiate the boundary scan test, perform the following steps:

1. Enable the boundary scan hardware switch.

   For a liquid-cooled system, the boundary scan hardware switch is located on the front side of chassis 0, above the WACS display.

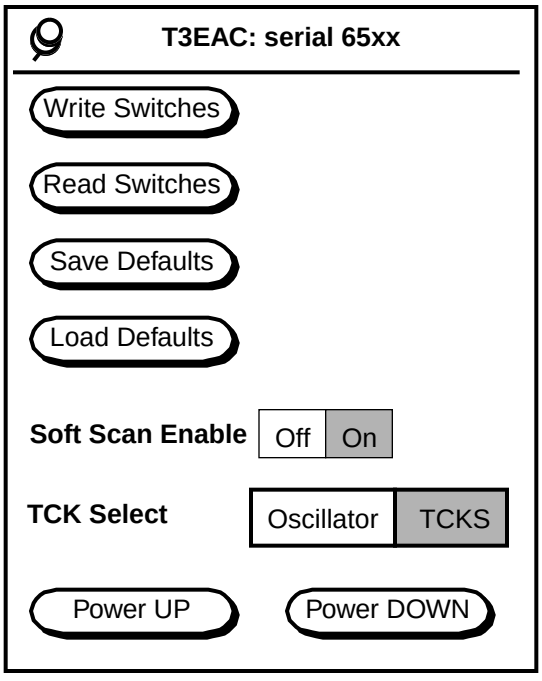
   For an air-cooled system, the boundary scan hardware switch is located on the rear side of chassis 0, above the clock module (slot 6).

2. Enable the boundary scan software switch and test clock.

   To enable the software switch and the test clock, bring up the nwacs display (`nwacsuser`), select On for the soft scan enable, select TCKS for the TCK select, and click on the Write Switches button (refer to Figure 23).

   To verify the settings of the software switches, click on the Read Switches button.

Figure 23. Boundary Scan Software Switch (Soft Scan Enable)



You can initiate the boundary scan test using t3ems or command line syntax.

Initiating the Boundary Scan Test by Using t3ems

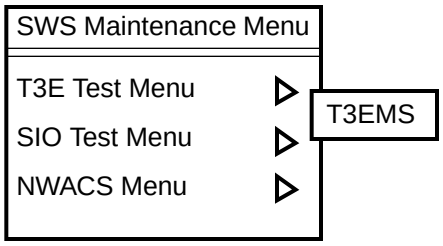
1. Bring up t3ems.

   To bring up t3ems, perform one of the following procedures:

   - Go to the root window and press the middle mouse button.

     Select T3EMS from the T3E Test Menu (refer to Figure 24).

   Figure 24. Selecting t3ems from a Menu

   or

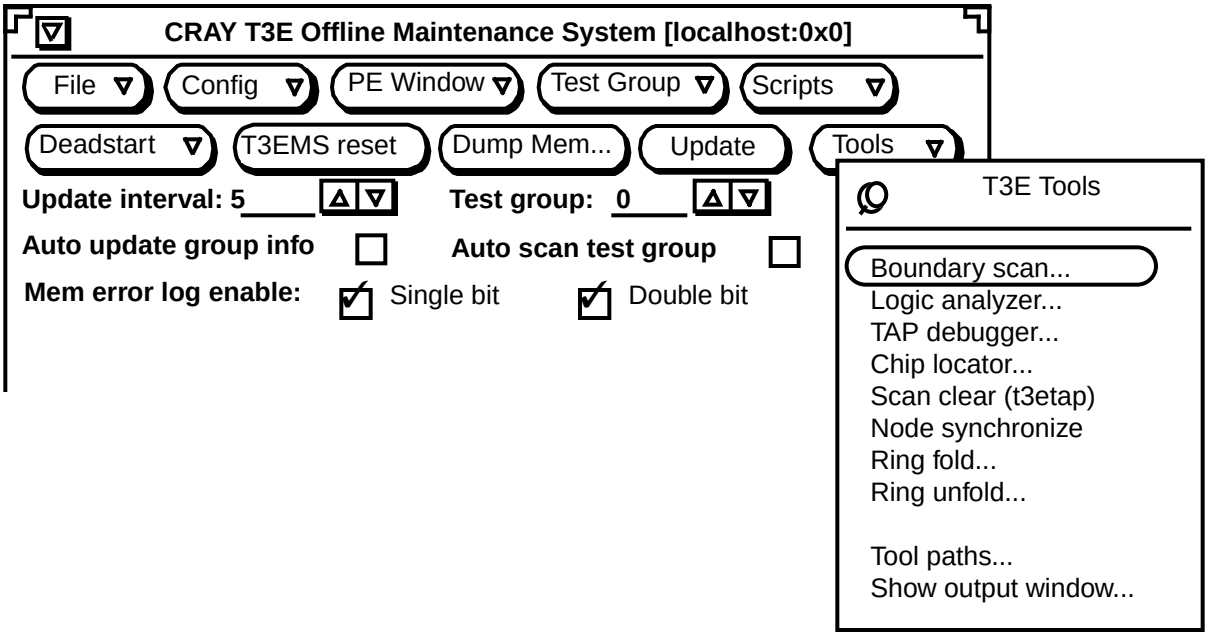
   - In a window, type the following syntax:

     t3ems &

   NOTE: t3ems is located in the /opt/CYRIdiag/t3e/bin directory.

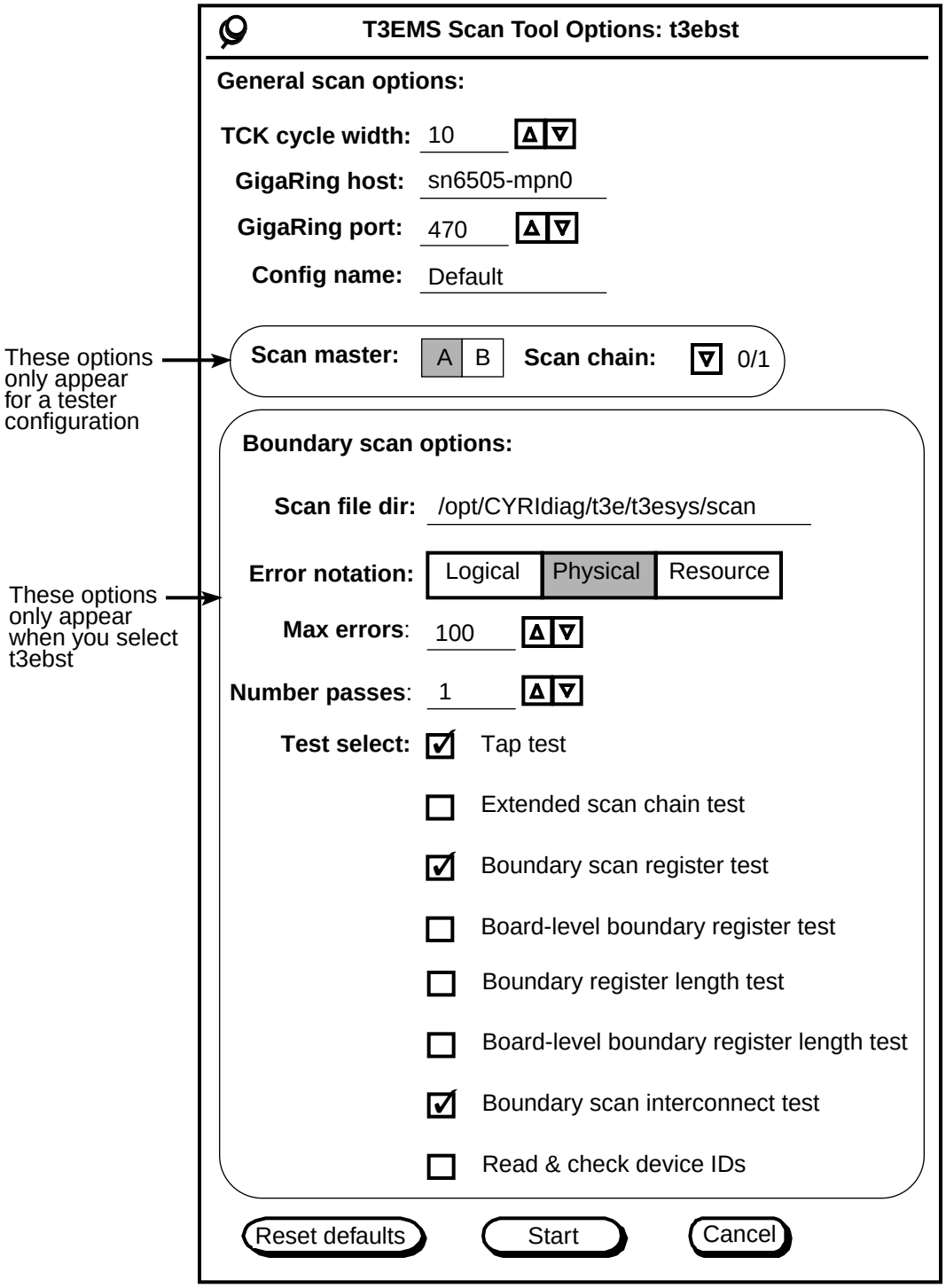
2. Select the boundary scan test from the Tools menu (refer to Figure 25).

Figure 25. Tools Menu



The T3EMS Scan Tool Options window appears on the screen (refer to Figure 26).

Figure 26. T3EMS Scan Tool Options Window



3. Select an error notation option.

   This option specifies whether the boundary scan test should display the error information using logical or physical component designators (refer to Figure 28 and Figure 29), or display the failing resources (refer to Figure 31). The default error notation is physical.

   The T3EMS Scan Tools Options window also lists the following user selectable options; however, the default selections of these options are based on the t3ems configuration information and do not need to be changed.

   TCK cycle width
   This option overrides the default TCK pulse width. This value can be any number between 3 and 60; the default value is 10.

   GigaRing host
   This option selects the host system.

   GigaRing port
   This option selects the I/O port.

   Config name
   This option specifies the configuration file that the boundary scan test will use; the default file name is Default.

   Scan master
   This option selects the scan master PCB and the scan chain for the A (top) PCB. This option is only available when you are running the boundary scan test on a module in a test vehicle.

   Scan file dir
   This option indicates the pathname of the scan files.

   Max errors
   This option specifies how many errors the boundary scan test displays to the user. This value can be any number between 1 and 100; the default value is 100.

   Number passes
   This option specifies how many passes the boundary scan test makes. This value can be any number between 1 and 100; the default value is 1.

   Test select
   This option specifies which tests the boundary scan test performs.

4. Click on Start to start the boundary scan test.

   Clicking on this button starts the selected boundary scan tests. t3ems directs the status and error information to the log window.

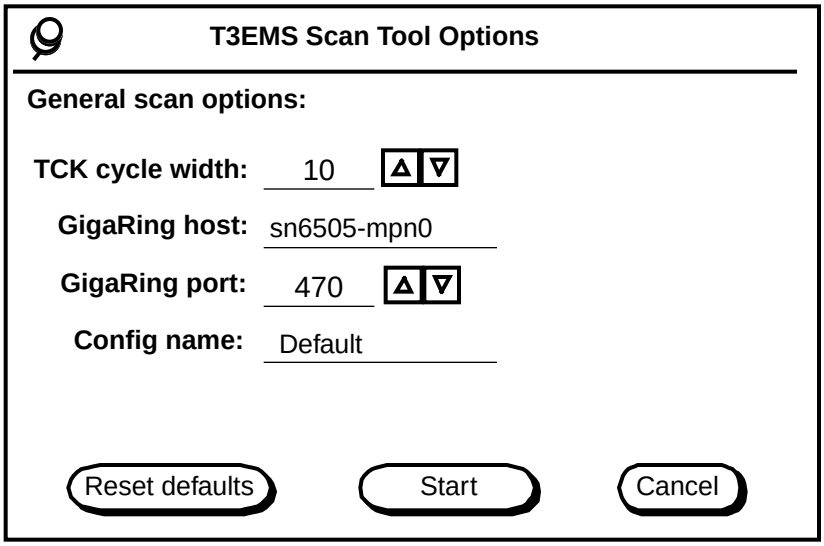
NOTE: After the boundary scan test completes, you must run Scan clear (t3etap). Scan clear (t3etap) resynchronizes the phase-locked loop between the microprocessor, the C option, and the TH option.

5. Select the Scan clear (t3etap) utility from the Tools menu (refer again to Figure 25).

   The T3EMS Scan Tool Options window appears on the screen (refer to Figure 27).

6. Click on Start to start the Scan clear (t3etap) utility.

Figure 27. T3EMS Scan Tool Options Window for Scan Clear



Scan clear (t3etap) displays the following status information:

```
=== Begin scan clear ===

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN
sn6505-mpn0:0470 done.

Performing TAP test:

    Chain 00...passed
        Detected from hardware: #chips=60 IR_length=310

Reading revisions from hardware and verifying configuration:
    Chain 00...done

Boundary-scan revisions from hardware (by scan chain):
    <GRC> = '+' if GigaRing chip in scan chain; ' ' if chip in bypass
    <BRD> = board on 'A' or 'B' side of coldplate
    <REV> = bits 2^3 - 2^0 of BSTREV (in hexadecimal)


          G B R
          R R E
    00    C D V
    - - - -  - - -
    002U  + A 0
    001U  + A 0


Sending CML_OVRD ON [all chips] (master)...
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending TAP reset...
Sending RAMBIST [all chips] (all)...
Call external clock adjust...
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending SDR [C+M+R] (master)...
Sending SDR (non-master)...
Sending CML_OVRD ON [I] (master)...
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending CML_OVRD ON [I+R] (master)...
```

```
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending SDR [C+M+R] (master)...
Sending SDR (non-master)...
Sending CML_OVRD ON [R] (non-master)...
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending SDR [C+M+R] (master)...
Sending SDR (non-master)...
Sending CML_OVRD ON [I+R] (non-master)...
Sending SDR [C+M+R] (master)...
Sending SDR (non-master)...
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending CML_OVRD ON [all chips] (non-master)...
Sending SDR [C+M+R] (master)...
Sending SDR (non-master)...
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending CML_OVRD ON [all chips] (master)...
Sending NDR...
NDR: TAP reset and move to TEST-LOGIC-RESET...
NDR: Performing NDR function...
NDR: TAP reset and move to RUN-TEST-IDLE...
Sending TAP reset...

=== End scan clear ===
```

Initiating the Boundary Scan Test by Using Command Line Syntax

1. Enter the `t3ebst` command with desired options.

   At the prompt, type:

   `t3ebst [-c <#>] [-d <path>] [-e <#>] [-g] [-h] [-p <#>] [-q] [-r <type>] [-s <def>] [-sim] [-G <spec>] [-C <cfg>] [-n <node_id>] [-t <test>]`

   t3ebst is located in the /opt/CYRIdiag/t3e/bin directory.

   The `t3ebst` command accepts the following options:

   `-c <#>`
   This option overrides the default TCK pulse width. This value can be any number between 3 and 60; the default value is 10.

   `-d <path>`
   This option specifies the test file directory for the system.

   `-e <#>`
   This option defines the maximum number of errors that the command will display to the user. This value can be any number between 1 and 10000; the default value is 100.

   `-g`
   This option generates boundary-scan test patterns and exits.

   `-h`
   This option displays the online option descriptions for this command.

   `-p <#>`
   This option specifies how many passes the boundary scan test makes. This value can be any number between 1 and 100; the default value is 1.

   `-q`
   This option specifies that t3ebst should run the short version of the boundary scan test.

`-r <type>`
This option defines the type of reference names that t3ebst uses to display errors. Valid types are:

- log - Display logical reference names
- phy - Display physical reference names
- res0 - Display the resiliency information to avoid a bad net
- res1 - Modify the configuration information to avoid a bad net

`-s <def>`
This option defines the scan master and the scan chains for a module that is being tested in a test vehicle.

`<def>` requires the following format:

```
<SM>+<top PCB chain#>
```

`<SM>` is the scan master board (A or B)

`<top PCB chain#>` is an even scan chain number (0, 2, ..., 14). The odd-numbered scan chain directly relates to the even-numbered chain. For example, when the `<def>` is `b+4`, the B PCB of slot 1 is scan master; the top PCBs use scan chain 4 and the bottom PCBs use scan chain 5.

The default format is `a+0`. (The A PCB of slot 1 is the scan master; the top PCBs use chain 0 and the bottom PCBs use chain 1.)

`-sim`
This option specifies that the boundary scan test should run in simulation mode. The program does communicate with real hardware.

`-G <spec>`
This option defines the host system and the I/O port for the GigaRing communications. `<spec>` requires the following format:

```
<host>:<port>
```

`-C <cfg>`
This option specifies the name of the configuration file that the `t3ebst` command uses.

`-n <node_id>`
This option specifies the GigaRing scan-node-identification (ID) number (in hexadecimal). This scan-node-ID number overrides the scan-node-ID number from the configuration file.

`-t <test>`
This option specifies which tests the boundary scan test performs. The boundary scan test can perform any number of tests. When you select more than one test, use a plus sign (+) to separate the test names. For example, the following option selects the tap, id, and bsr tests:

```
-t tap+id+bsr
```

You can list the tests in any order; however, certain tests require that other tests complete successfully. Selection of one test may cause the automatic selection of other tests.

The following tests are valid tests:

tap (TAP test)
Tests the basic integrity and configuration load for all of the TAPs in the system.

sct (Extended scan chain test)
Tests the TDI-to-TDO paths by shifting large patterns through each scan chain. All bypass registers are selected.

bsr (Boundary scan register test)
Tests all of the boundary scan registers. When you select the bsr test, the `t3ebst` command automatically selects the tap test.

bbsr (Board-level boundary register test)
Tests the boundary scan registers of one PCB so that a failure can be isolated to a specific PCB. To do this, the test selects the boundary scan registers of one PCB and the bypass registers of the other PCBs in the system.

bsl (Boundary register length test)
Verifies the length of the boundary scan chain. Use this test to determine whether an incorrect boundary scan revision (specifically, the GigaRing bypass jumper information) is causing the failure.

bbsl (Board-level boundary register length test)
Verifies the boundary scan chain length of one PCB so that a failure can be isolated to a specific PCB. To do this, the test selects the boundary scan registers of one PCB and the bypass registers of the other PCBs in the system.

bst (Boundary scan interconnect test)
Performs the boundary scan interconnect test. When you select the bst test, the `t3ebst` command automatically selects the tap test and

the bsr test.

id (Read and check device IDs)
Reads and displays the device ID registers. When you select the id test, the `t3ebst` command automatically selects the tap test.

The default test selection is bst, which is equivalent to tap+bsr+bst.

NOTE: When an error occurs during the boundary scan register test (bsr), use the following troubleshooting procedure to help identify the cause of the failure:

1. Execute the sct test to verify that the scan chain is shifting the data properly. When sct fails, use the tap test and the sct test to troubleshoot the failure.

2. Execute the bsl test to verify the length of the boundary register scan chain. When bsl determines the length, but the length does not match what is expected, go to Step 3. When bsl passes or it is unable to determine the chain length, go to Step 4.

3. Execute the bbsl test to isolate the failure to a specific PCB.

4. Execute the bbsr test to isolate the failure to a specific PCB.

Error Information

The following subsections contain examples of boundary scan failures.

NOTE: When the boundary scan test identifies a failure, run Scan clear (t3etap) before removing power from the module.

TAP Test Failure

The boundary scan test displays the following error information when the boundary-scan hardware switch or the boundary-scan software switch is not enabled. This type of failure can also be caused by an open wire between the top module in the chassis and the scan master, failing scan master logic, or failing logic in the top module in the cabinet.

```
=== Begin boundary scan test ===

T3E Boundary-Scan Test - t3ebst version 2.0

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN sn6505-mpn0:0470 done.

Performing TAP test:

    Chain 00...failed
    All 1's coming out of instruction register chain.
    Verify power and communications to module(s) in system.

Unable to continue due to TAP test errors.

=== End boundary scan test ===
```

TAP Test Vector = IR_TEST TDO Failure

When the boundary scan test detects a boundary scan chain test error, it calculates the physical location of the component that detected the error (refer to the following error information). For this example, the component that detected the error is an I option (physical name is AI0) that resides on the upper PCB in slot 1 of chassis 0.

```
=== Begin boundary scan test ===

T3E Boundary-Scan Test - t3ebst version 2.0

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN sn6505-mpn0:0470 done.

Performing TAP test:

    Chain 00...failed
        Invalid data shifted out of instruction register chain.
        Miscompare @ board 001U chip I (physical chip name AI0)
        Check component and JTAG signals to/from component.

VECTOR=ACTUAL IR TDO DATA
84090842 10842108 42108421 08421084 2108421F FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF


Unable to continue due to TAP test errors.

=== End boundary scan test ===
```

Interconnect Test Failure

The boundary scan test displays the following error information when it detects an interconnect failure.

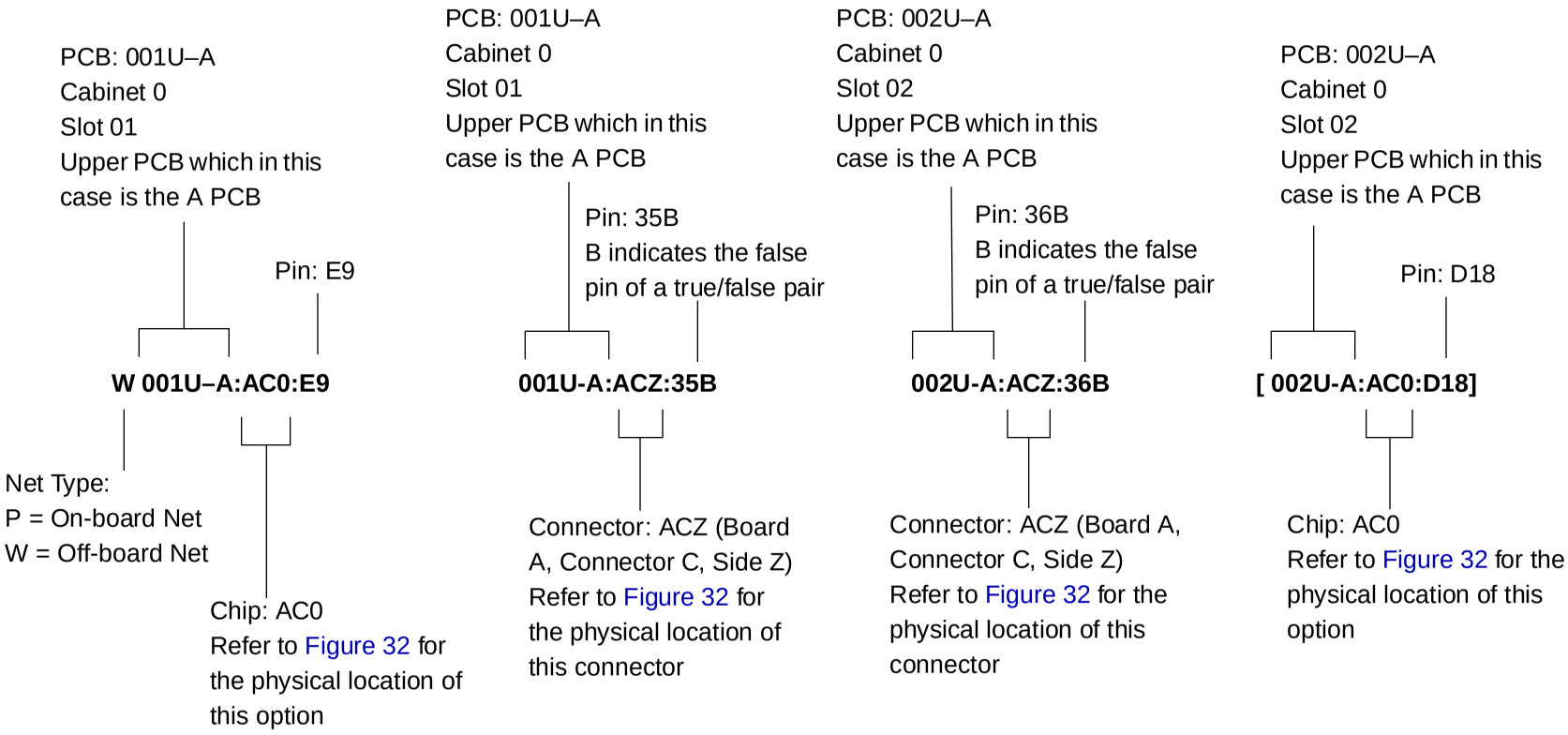
```
=== Begin boundary scan test ===

T3E Boundary-Scan Test - t3ebst version 2.0

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN sn6505-mpn0:0470 done.

Performing TAP test:

        Chain 00...passed
                Detected from hardware: #chips=60 IR_length=310

Reading revisions from hardware and verifying configuration:
        Chain 00...done

        Boundary-scan revisions from hardware (by scan chain):
        <GRC> = '+' if GigaRing chip in scan chain; ' ' if chip in bypass
        <BRD> = board on 'A' or 'B' side of coldplate
        <REV> = bits 2^3 - 2^0 of BSTREV (in hexidecimal)

              G B R
              R R E
        00    C D V
        - - - -  - - -
        002U  + A 0
        001U  + A 0
 Testing boundary-scan registers:
        Chain 00...passed
```

```
Performing boundary scan interconnect test (pass 1 of 1):

(30 patterns will be applied)

Pattern 00...done
Pattern 01...done
Pattern 02...done
Pattern 03...done
Pattern 04...done
Pattern 05...done
Pattern 06...done
Pattern 07...done
Pattern 08...done
Pattern 09...done
Pattern 10...done
Pattern 11...done
Pattern 12...done
Pattern 13...done
Pattern 14...done
Pattern 15...done
Pattern 16...done
Pattern 17...done
Pattern 18...done
Pattern 19...done
Pattern 20...done
Pattern 21...done
Pattern 22...done
Pattern 23...done
Pattern 24...done
Pattern 25...done
Pattern 26...done
Pattern 27...done
Pattern 28...done
Pattern 29...done
```

Following the pattern information, the boundary scan test lists the failure information. The boundary scan test logs the failing nets using logical names, physical names (refer to Figure 28 and Figure 29), or resource information (refer to Figure 31). You select how the boundary scan test logs the nets by clicking on the desired error notation in the T3EMS Scan Tool Options window (refer to Figure 26).

Figure 28. Physical Boundary Scan Failure Information (Off-board Net for a Liquid-cooled System)

CHAIN POSITION	EXPECT DATA	ACTUAL DATA	NET INFORMATION (net type: P=on-board net, W=off-board net) Format of each node: <board>:<chip>:<pin>
00–11753	10101001100110100101100110 0110	11111111111111111111111111111111	W 001U–A:AC0:E9 001U-A:ACZ:35B 002U-A:ACZ:36B [002U-A:AC0:D18]
00–11754	10101001100110101010011001 0110	00000000000000000000000000000000	W 001U–A:AC0:F10 001U-A:ACZ:35 002U-A:ACZ:36 [002U-A:AC0:C19]
00–11755	10101001100110100101011010 1010	11111111111111111111111111111111	W 001U–A:AC0:D8 001U-A:ACZ:37B 002U-A:ACZ:38B [002U-A:AC0:A21]
00–11756	10101001100110101010010101 1010	00000000000000000000000000000000	W 001U–A:AC0:C7 001U-A:ACZ:37 002U-A:ACZ:38 [002U-A:AC0:B20]



NOTE: Brackets surround the component that detected the error; the component detects an error when it inputs the signal.

Figure 29. Physical Boundary Scan Failure Information (On-board Net for a Liquid-cooled System)

```
CHAIN    EXPECT                              ACTUAL                              NET INFORMATION (net type: P=on-board net, W=off-board net)
POSITION DATA                                DATA                                Format of each node: <board>:<chip>:<pin>

00–006560 10010101100110010101100110101O  11111111111111111111111111111111  P 002U–A:AH2_M:15 [002U-A:AF0:T18] 002U-A:AH2:E12 002U-A:AH2_CN0:E12
                                             ^^ ^ ^  ^^  ^^ ^ ^  ^^  ^ ^ ^
```

t3ebst completed with 1 failures.

=== End boundary scan test ===

PCB: 002U–A
Cabinet 0
Slot 02
Upper PCB which in this case is the A PCB

Pin: 15

P 002U–A:AH2_M:15

Net Type:
P = On-board Net
W = Off-board Net

Chip: M option on daughter card AH2

PCB: 002U–A
Cabinet 0
Slot 02
Upper PCB which in this case is the A PCB

Pin: T18

[002U-A:AF0:T18]

Chip: C option at location AF0
Refer to Figure 32 for the physical location of this option

PCB: 002U–A
Cabinet 0
Slot 02
Upper PCB which in this case is the A PCB

Pin: E12

002U-A:AH2:E12

Chip: Mother board connector at location AH2
Refer to Figure 32 for the physical location of this connector

PCB: 002U–A
Cabinet 0
Slot 02
Upper PCB which in this case is the A PCB

Pin: E12

002U-A:AH2_CN0:E12

Chip: Daughter card connector at location AH2

NOTE: Brackets surround the component that detected the error; the component detects an error when it inputs the signal.

NOTE: The physical boundary scan failure information is the same for a liquid-cooled system and an air-cooled system, with the exception of how you interpret the PCB identifier. Figure 28 and Figure 29 describe how to interpret the physical boundary scan failure information for a liquid-cooled system, which includes a description of the PCB identifier; Figure 30 describes how to interpret the PCB identifier for an air-cooled system.

Figure 30. Description of the PCB Identifier for an Air-cooled System

Example 1:

W 011U–A:AC0:E9 001U-A:ACZ:35B 002U-A:ACZ:36B [002U-A:AC0:D18]

PCB: 011U
Boundary scan chain 0
Cabinet 1 of the scan chain (Cabinet 1)
Slot 1
Upper PCB
NOTE: All air-cooled PCBs are considered upper PCBs.

Example 2:

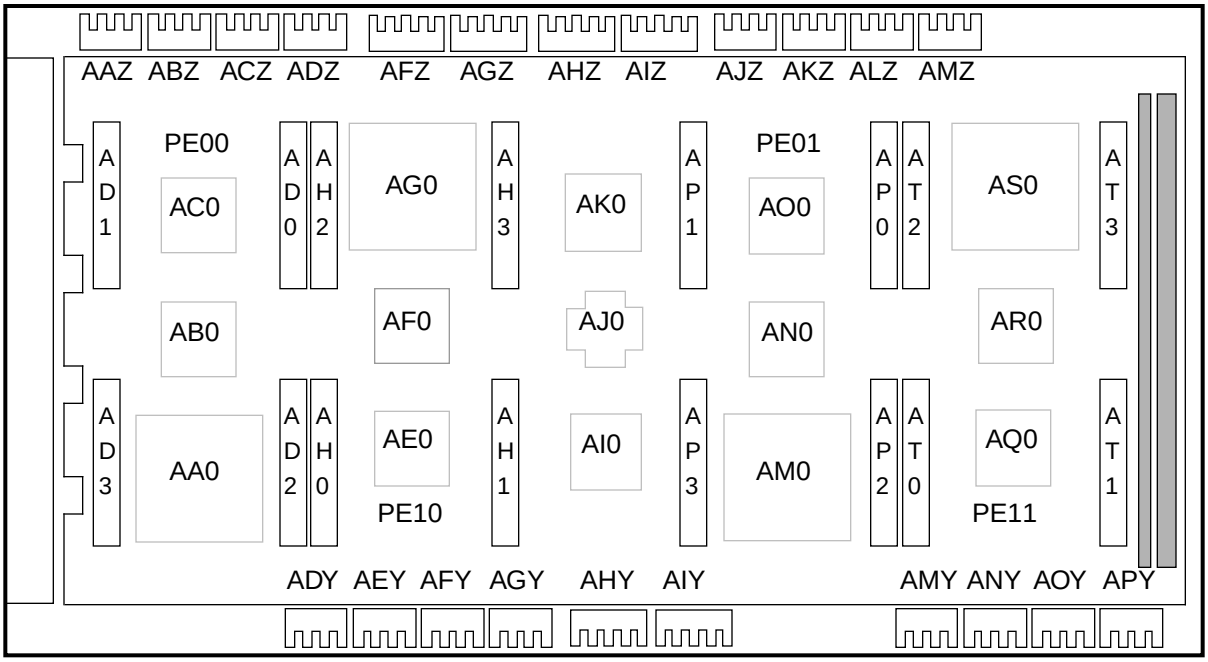
W 102U–A:AC0:E9 102U-A:ACZ:35B 103U-A:ACZ:36B [103U-A:AC0:D18]

PCB: 102U
Boundary scan chain 1
Cabinet 0 of the scan chain (Cabinet 3)
Slot 2
Upper PCB

Figure 31. Resource Boundary Scan Failure Information

```
Boundary scan errors detected!!!

Raw pin number                : 00-006560
Expected data                 : 10010101100110010101100110101O
Actual data                   : 11111111111111111111111111111111
FAILING BOARD                 : CHASSIS = 0  SLOT = 2  BOARD = Upper(A)
FAILING NET NAME              : CHIP = N10M2_M      PIN = MOUT13
RESILIENCY REQUIREMENT        : Disable the PE port on PWHO 100

t3ebst completed with 1 failures.

=== End boundary scan test ===
```

Figure 32. Physical Option and Connector Locations



NOTE: This diagram represents the side of the PCB that is visible after it is mounted to the coldplate with the daughter cards removed. You cannot see the “grayed” components.

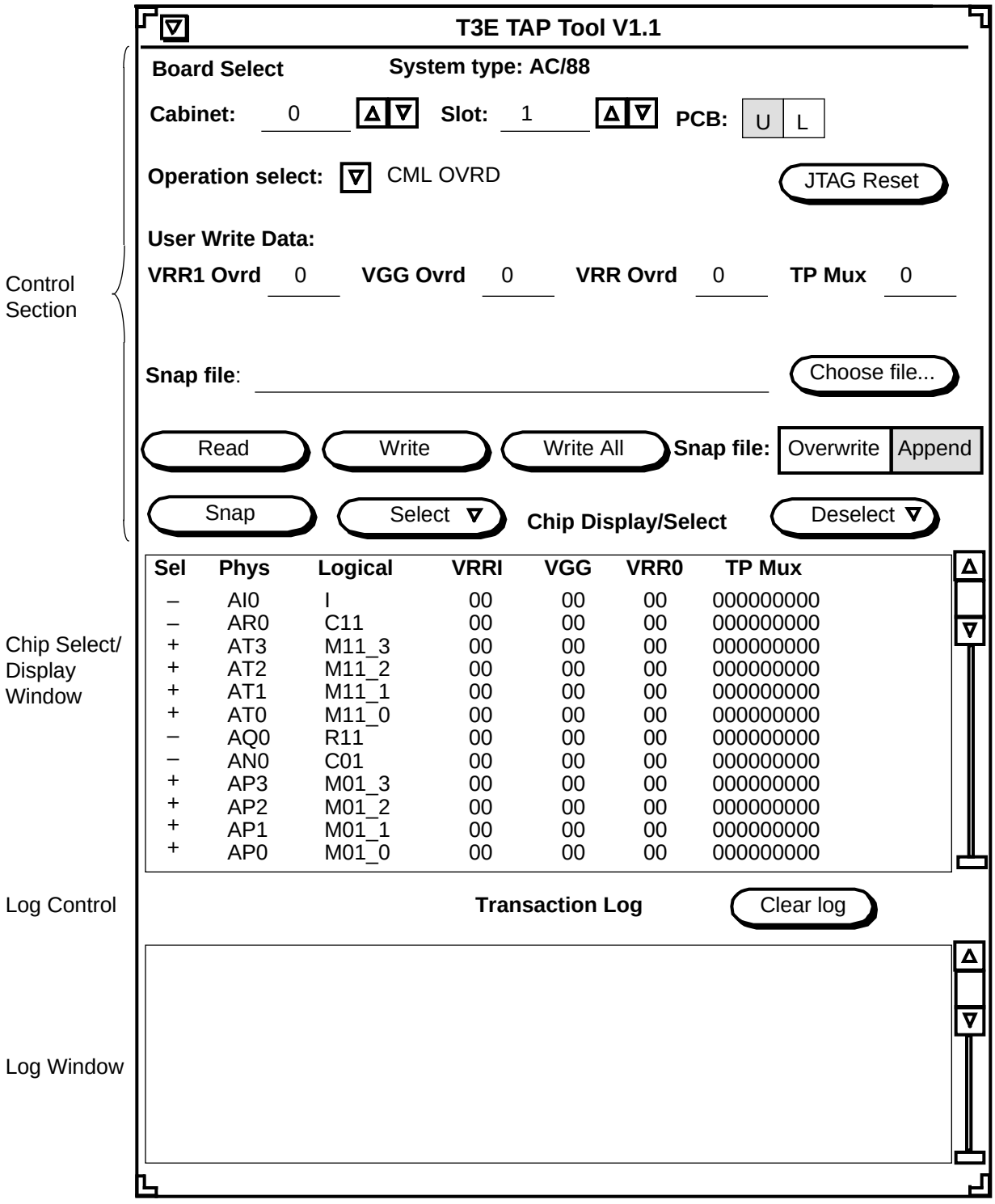
CRAY T3E TAP Tool (t3etap)

NOTE: This document applies to all versions of t3etap up to version 1.1.

The SWS-based test access port (TAP) debugger program, t3etap, is a utility that allows you to exercise various functions of the TAP controller and boundary scan registers in the CRAY T3E system; you can select the TAP register and the group of options to operate on, enter test patterns, and issue scan operations. Depending on the register that you select, t3etap can read data from the register or scan data into the register. t3etap displays the results on the screen or writes the results to an output file.

The T3E TAP Tool window controls all of the functions of the t3etap program. Figure 33 shows a snapshot of this window. It consists of several sections; the following text describes these sections.

Figure 33. T3E TAP Tool Window



Control Section

The control section, which is located in the top portion of the window, contains the main program controls.

Board Select and System Type

The Board Select fields (cabinet number, slot number, and PCB letter) identify the module where you want t3etap to execute. The T3E TAP Tool window provides choices that are limited to valid values for the configured system type.

NOTE: The cabinet and slot numbers are decimal values. Cabinet numbering begins with 0; slot numbering begins with 1.

The System Type field identifies the system as an air-cooled (AC) system or a liquid-cooled (LC) system and indicates the number of PEs. t3etap extracts this information from the system configuration information; you cannot alter this information from the T3E TAP Tool window.

Operation Select

The Operation Select field identifies the function that you want t3etap to execute. Table 1 lists the function choices and identifies the types of operation that are valid for each function. Table 1 also indicates whether the output appears on the screen of the SWS or in a file. Functions that are marked as “file output” always send their output to a file rather than to the screen. Functions marked “file input” require their input to be taken from a file rather than from information that the user inputs.

Table 1. Supported TAP Register Functions

Function	Read	Write	Write All	File Output	File Input
SDR		Valid	Valid		
DEVICE ID	Valid				
PLL_CLK_OK	Valid				
CML_OVRD	Valid	Valid	Valid		
UART	Valid	Valid			
RAMBIST		Valid	Valid		
RAMDUMP	Valid			Valid	
INTERNAL SCAN	Valid	Valid		Valid	Valid
SYSTEM SCAN RESET		Valid			

Most operations are not supported by all of the option types. Only the options that support the current operation appear in the option list.

The SYSTEM SCAN RESET function is not a true TAP operation; it initiates the special built-in scan clear sequence. When this function executes, t3etap ignores the option selection.

User Input Area

The user input area, which is located directly below the operation select, allows you to input information when you select a writable register. Figure 33 shows inputs for the CML_OVRD function. After you enter the desired values, write the data to the system. When you select a non-writable function, the user input area is not visible. When you select a function that requires an output file, the user input area displays the message << OUTPUT FILE IS REQUIRED BY THIS FUNCTION >>.

Input/Snap and Output Files

The control section provides two lines: one line for an input file name and one line for an output file name. You may enter either a file name or a path name. When you provide the file name, t3etap places the file in the current directory (the directory from which you started t3etap). To determine alternative file names, click on the Choose file button. A popup window appears that lists file names and directories. If you pick a file name from this window, insert the full path name on the line.

The functions listed in Table 1 that require an output file will not execute until you provide a file name. The output file name is also used by the window snap function.

The internal scan operation is the only operation that requires an input data file when it writes to the hardware. This input data file is an ASCII file that contains one or more sets of scan input data (TDI). The TDI entries are indexed by option; the options are numbered in the order in which they appear in the option display. Each entry uses the following format:

```
TD[n] = <data>

[<data>...]
```

The index n identifies the option. The data consists of a string of one or more hex digits with no spaces. t3etap places these hex digits in the TDI array. If the data provided is shorter than the actual TDI bit string, t3etap fills the remainder with zeros. For increased readability, you may break the data into

multiple lines; t3etap ignores newline characters within the data string. t3etap terminates the data when the first character it encounters is not a newline or hex digit. The TD entries may be in any order and unused options do not need entries.

NOTE: t3etap uses this format when it reads the internal scan data from the hardware into a file. This allows t3etap to feed the output file directly back in as an input file. When t3etap writes an internal scan data file, it includes a TD entry for every option. For the options that do not support internal scan and for the options that are deselected, t3etap enters a single zero value into the TD entry.

Operation Controls

The Read, Write, and Write All buttons initiate the currently selected function. These buttons are only enabled when you select a valid function.

NOTE: Regardless of the current board selection, the Write All button operates on all boards in the system except the scan master. To write a function to all boards (including the scan master), select the scan master and perform a normal write to it after applying the write all function. The scan master is always in slot 1 of cabinet 0.

The Snap button copies the current option window display to an output file. The Snap file setting determines whether the file is appended to the output file or the file overwrites the output file. The Snap button is inactive for functions that write their output directly to a file.

The Select button selects all of the options in the Chip Select/Display window. The Deselect button deselects all of the options in the Chip Select/Display window.

Chip Select/Display Window

This window lists all of the options that support the currently selected operation. t3etap uses the first column of the display to select the option(s) that it will operate on. The options preceded by a dash (–) are deselected; the options preceded by a plus sign (+) are selected.

You can select or deselect options by clicking on the Select button or the Deselect button; or by using the mouse buttons. The Select and Deselect buttons allow you to select or deselect all options of a certain type or all options in the list. The three mouse buttons operate as follows:

- The left (select) button toggles the selection
- The middle (adjust) button turns a selection on
- The right (menu) button turns a selection off

In order for the mouse to work, point the cursor at the + or – character. You can also hold the mouse button down and drag the mouse up or down to operate on more than one line. As the pointer approaches the top or bottom of the window, the view scrolls up or down automatically.

The Chip Select/Display window contains several other columns of information: the physical name of the options, the logical name of the options, VRRI, VGG, VRR0, and TP Mux. You cannot change this information.

NOTE: You can change the length of the Chip Select/Display window from the default of 16 lines. To change the length, add the following entry in your Xdefaults file (normally $HOME/.Xdefaults):

```
t3etap.chipWinLength:      new_length
```

`new_length` is an integer value between 2 and 30. Any other values cause t3etap to print a warning and use the default setting. After adding the line to your Xdefaults file, execute the command **`xrdb -merge .Xdefaults.`** This command applies your change.

Transaction Log Window

This window records each operation you perform and the board on which it was performed. The window also lists whether the operation succeeded or failed. The SYSTEM SCAN RESET function prints several lines as it performs various functions. The Clear button clears the log contents. You can save the log to a file by using the standard menu of the window. (Access the standard menu by pressing the menu button with the pointer over the window).

Initiating t3etap by Using t3ems

1. Bring up t3ems.

   At the prompt, type **`t3ems`**

   NOTE: t3ems is located in the /opt/CYRIdiag/t3e/bin directory.

2. Select the t3etap test from the Tools menu.

   The T3EMS Scan Tool Options window appears on the screen (refer to Figure 34).

3. Make the appropriate option selections.

   TCK cycle width
   This option overrides the default TCK pulse width. This value can be any number between 3 and 60.

   GigaRing host
   This option selects the host system.

   GigaRing port
   This option selects the I/O port.

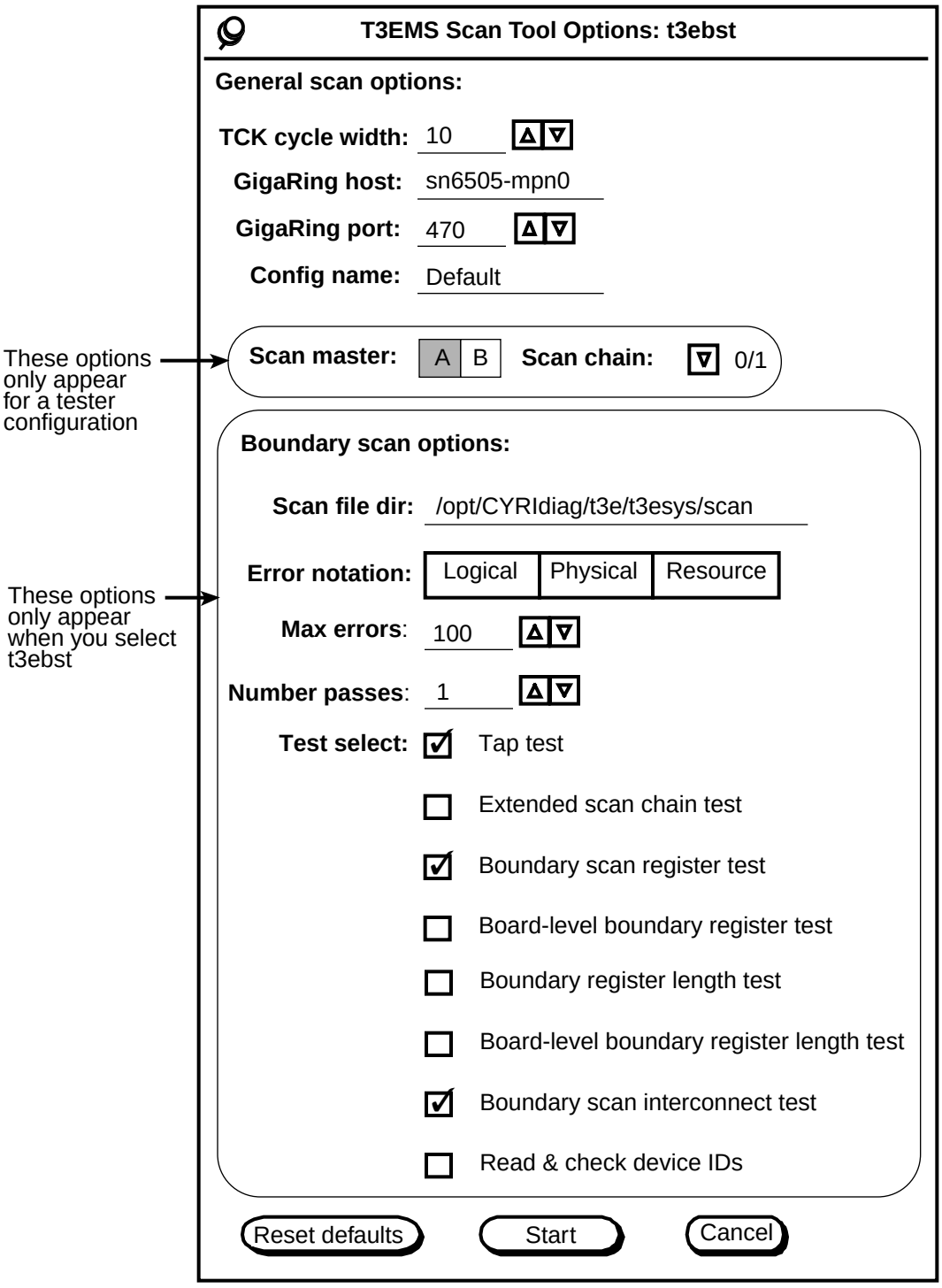
   Config_name
   This option selects a configuration file that t3etap will load. By default, t3etap loads a configuration named Default.

   Scan master
   This option selects the scan master PCB and the scan chain for the A (top) PCB. This option is only available when you are running t3etap on a module in a test vehicle.

4. Click on Start to start the t3etap test.

   Clicking on this button starts the t3etap test. t3ems directs the status and error information to the log window.

Figure 34. T3EMS Scan Tool Options Window



Initiating t3etap by Using Command Line Syntax

1. Change to the /opt/CYRIdiag/t3e/bin directory.

   At the prompt, type:

   `cd /opt/CYRIdiag/t3e/bin`

2. Enter the `t3etap` command with desired options.

   At the prompt, type:

   `t3etap [-B] [-r] [-c tck_width] [-i input_data_path] [-s tv_bd+chain] [-G host[:port]] [-C config_name] [-H hdw_rev] [-n node_id] [-l chip_win_length]`

   The `t3etap` command accepts the following options:

   `-B`
   This option prevents t3etap from reading the BST revision during the startup sequence.

   `-r`
   This option causes t3etap to execute a scan reset sequence only; t3etap does not bring up the user interface.

   `-c tck_width`
   This option changes the value of the TCK pulse width. This value can be any number between 3 and 60; the default value is 3.

   `-i input_data_path`
   This option allows you to bring up t3etap using a different scan directory than the default scan directory (/opt/CYRIdiag/t3e/t3esys/scan). Use this option only when you know how to generate customized data bases.

   `-s tv_bd+chain`
   This option defines the scan master and the scan chains for a module that is being tested in a test vehicle.

   This option uses the following format:

   ```
   <SM>+<top PCB chain#>
   ```

   `<SM>` is the scan master board (u or a for upper, l or b for lower).

   `<top PCB chain#>` is an even scan chain number (0, 2, ..., 14). The odd-numbered scan chain directly relates to the even-numbered chain. For example, when the `<def>` is `b+4`, the B PCB of slot 1 is scan master; the top PCBs use scan chain 4 and the bottom PCBs use scan chain 5.

The default format is `u+0`. (The A PCB of slot 1 is the scan master; the top PCBs use chain 0 and the bottom PCBs use chain 1.)

`-G host[:port]`
This option overrides the default host name and port number. t3etap uses the host name and port number to connect to the GigaRing server process. The default host name is "localhost" (assuming that the server is running on the same host as t3etap) and the default port number is 470. Normally, the port number should not have to be changed; therefore, the port number is optional.

`-C config_name`
This option selects a configuration file that t3etap will load. By default, t3etap loads a configuration file named Default.

`-H hdw_rev`
This option selects Pass 1 hardware (1) or Pass 2 hardware (2). The default value is 2.

`-n node_id`
This option specifies the GigaRing node ID for the scan node. This value overrides the value saved in the system configuration file and is a hexadecimal number with no special prefix.

`-l chip_win_length`
This option sets the length of the Chip Select/Display window. The default value is 16 lines; a value of 0 causes the window to be the maximum size (all options are displayed).

After you start t3etap, t3etap calls a scan initialization routine that sets up data structures and reads the system configuration file to determine whether the system is an air-cooled system or a liquid-cooled system, a system or a tester, and to determine the number of PEs in the system.

t3etap also performs initial scan tests. When a failure occurs, t3etap prints the error information and terminates without displaying the main interface window. When the initial scan tests are successful, t3etap prints information about the test results and displays the main window shown in Figure 33.

NOTE: The system configuration database server must be running and have the correct system setup for t3etap to function properly. When the system configuration server it is not set up correctly, use t3ems to correct the system type and the number of PEs. After you make the corrections, restart t3etap.

Index

I

J

M

N

O

P

R

S

T

W

X