Memory Configuration

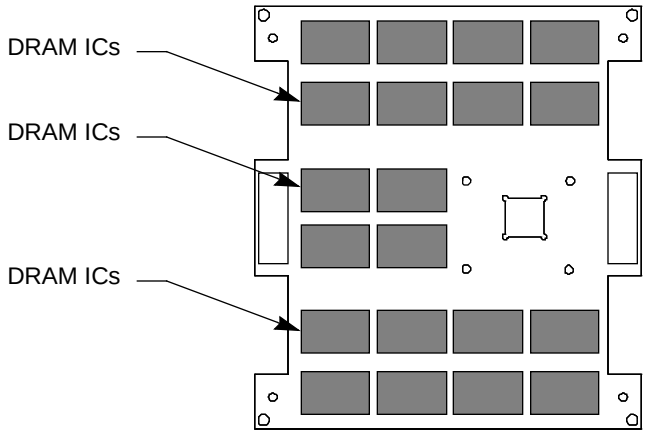
HMM-147-0

Memory Hardware Components

Two hardware components perform memory functions: the dynamic random access memory (DRAM) integrated circuits (ICs) and the M options.

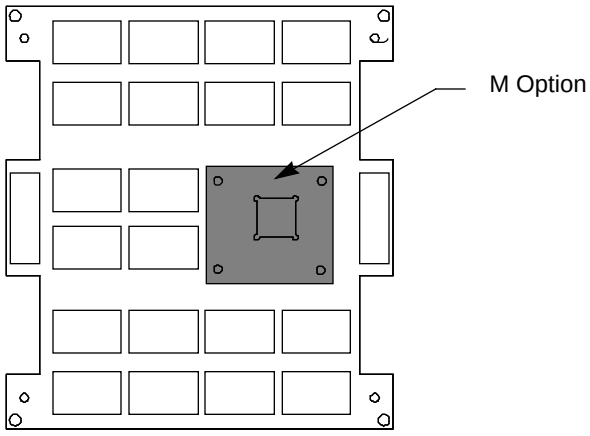
The DRAM ICs are the actual memory ICs. They are divided into 8 banks of memory. Figure 1 shows the location of the 20 DRAM ICs on one daughter card printed circuit board (PCB).

Figure 1. DRAM ICs on a Daughter Card PCB



The M options are part of the support circuitry that controls memory references (refer to Figure 2). Each M option controls functions for 2 banks of DRAM on one daughter card PCB. For example, M-option 0 controls functions for banks 0 and 4. M-option 2 controls functions for banks 2 and 6.

Figure 2. M Option on a Daughter Card PCB



Timing Parameters

Software must set several timing parameters for the DRAM ICs. These parameters control the following items.

- Row address strobe (RAS)
- Column address strobe (CAS)
- Write enable (WE)
- Output enable (OE)

Software controls the DRAM timing parameters by setting bits of the M option DRAM configuration M[3 : 0]_DRAM_CFG) registers to the appropriate values. Each M option has one M_DRAM_CFG register. Table 1 shows the bit format of the M[3 : 0]_DRAM_CFG registers. All values in the table are measured in system clock (sysclk) periods.

Table 1. M[3 : 0]_DRAM_CFG Registers Bit Format

Bits	Name	Description
<1 : 0>	TRP	RAS precharge value 00 = 3 cps 10 = 5 cps 01 = 4 cps 11 = 6 cps
<3 : 2>	TRAS	RAS pulse width 00 = 4 cps 10 = 6 cps 01 = 5 cps 11 = 7 cps
<5 : 4>	TCP	CAS precharge value 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
<7 : 6>	TCAS	CAS pulse width 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
<9 : 8>	TWP	WE pulse width 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
<11 : 10>	TOE	OE pulse width 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
<13 : 12>	TRCD	RAS to CAS delay 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
<15 : 14>	TDH	Write data hold 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
<17 : 16>	TCSR	CAS to RAS refresh delay 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
<19 : 18>	CAC	Access time from leading edge of CAS 00 = 1 cps 10 = 3 cps 01 = 2 cps 11 = 4 cps
20	WT_DLY	When set to 1, this bit delays the same page write references by 1 clock period.
21	EXT_CAS	When set to 1, this bit delays all CAS signals by 0.5 clock periods (cps).
22	EXT_RAS	When set to 1, this bit delays all RAS precharge signals by 0.5 clock periods.
23	RD_PAST _CAS	When set to 1, this bit extends the go read data past the CAS
<63 : 24>	Not applicable	These bits are not used.

NOTE: Software should follow an auxiliary register write with an auxiliary register read to ensure that no negative side effects occur after the write.

Access Control

Software may set several parameters that control access to the DRAM ICs. The parameters control the following items.

- Memory references
- Memory address limit check
- IC configuration
- Output channel control
- Refresh rate

Software controls the access control parameters by setting bits of the M option configuration (M[3 : 0]_CFG) register to the appropriate value. Each M option has one M_CFG register. The following subsections describe the access control parameters of the M[3 : 0]_CFGregisters.

Memory References

Software can enable or disable two types of memory references: read ahead references and simultaneous bank references. Read ahead references temporarily store data from memory into a buffer in anticipation of a request for the data. Simultaneous bank references occur when 2 banks of memory are referenced at the same time.

In addition to enabling or disabling types of memory references, software can enable or disable reference scheduling. Reference scheduling reorders memory requests according to a priority table that is stored in the M option.

Software controls the memory reference parameters by setting bits <2 : 0> of the M[3 : 0]_CFG registers to the appropriate values. Table 2 shows the bit format of bits <2 : 0> of the M[3 : 0]_CFG registers.

Table 2. Memory References Bits of the M[3 : 0]_CFGRegisters

Bit	Name	Description
0	REF_SCH	When set to 1, this bit disables reference scheduling.
1	RD_AHD	When set to 1, this bit disables read ahead references
2	SIM_BKS	When set to 1, this bit enables simultaneous bank references.

Memory Address Limit Check

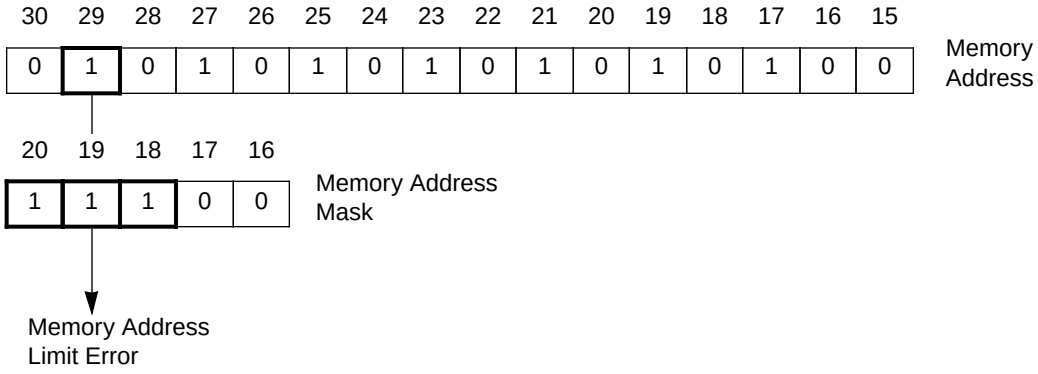
Software can enable or disable a memory address limit check. The memory address limit check determines whether a memory address is larger than a software-specified value and, if it is, indicates that an error occurred. Software enables the memory address limit check by setting a bit in the M option error (M[3 : 0]_ERR) registers.

Software specifies the maximum value for a memory address by setting the memory address mask to the appropriate value. The memory address mask is a mask that the support circuitry applies to bits <30 : 26> of a memory address. If a bit of the memory address mask is set to 1 and the corresponding bit of the memory address is set to 1, an error has occurred.

As an example, Figure 3 shows a sample memory address mask and a memory address that would cause an error. For clarity, Figure 3 does not show all of the bits for the memory address.

Bits <20 : 16> of the M[3 : 0]_CFG register contain the memory address mask.

Figure 3. Sample Memory Address Mask



IC Configuration

Software can set parameters that indicate the IC types. Software does this by setting bits <8 : 6> (MEM_CFG bits) of the M[3 : 0]_CFG registers to the appropriate value (refer to Table 3).

Table 3. Memory Configuration Bits of the M[3 : 0]_CFG Registers

MEM_CFG Bits (Bits <8 : 6>)	Size	IC Type
000	64 Mbytes	1M x 16 Chip select 0 only
001	128 Mbytes	1M x 16
010	256 Mbytes	2(1M x 16)
011	512 Mbytes	4(2M x 8)
100	256 Mbytes	4M x 16 Chip select 0 only
101	512 Mbytes	4M x 16
110	1,024 Mbytes	2 (4M x 16)
111	2,048 Mbytes	4 (8M x 8)

Output Channel Control

Software can enable or disable the memory output channel. To do this, software sets bit 3 (DIS_OUT_CH bit) of the M[3 : 0]_CFG registers to the appropriate value (refer to Table 4). Software may disable the output channel to test memory buffers.

Table 4. Output Channel Control Bit of the M[3 : 0]_CFG Registers

Bit	Name	Description
3	DIS_OUT_CH	When set to 1, this bit disables the output channel.

Refresh Control

Software can enable or disable memory refresh and can also set the length of time between refresh requests. To enable or disable memory refresh requests, software sets the refresh enable (REFRESH_EN) bit (bit 4) of the M[3 : 0]_CFG registers to the appropriate value (refer to Table 5).

To set the length of time between refresh requests, software sets bits <47 : 32> (RFRSH_RATE bits) of the M[3 : 0]_CFG registers to the appropriate values (refer again to Table 5).

Table 5. Refresh Bits of the M[3 : 0]_CFG Registers

Bits	Name	Description
4	REFRESH_EN	When set to 1, this bit enables memory refresh.
<47 : 32>	RFRSH_RATE	Indicates the length of time (in clock periods) between refresh requests. The minimum value is 40(hex). For 1M x 16 parts, use 516(hex). For 4-high stack parts, use 28B(hex).

Error Control

Software can enable or disable single-bit memory error correction and can also control the function of the M[3 : 0]_ERR[2] and M[3 : 0]_ERR[3] registers. To enable or disable single-bit memory error correction, software sets the single-bit error enable (SBE_EN) bit (bit 5) of the M[3 : 0]_CFG registers to the appropriate value (refer to Table 6).

To control the function of the M[3 : 0]_ERR[2] and M[3 : 0]_ERR[3] registers, software sets the enable all packets (EN_ALL_P) bit (bit 9) of the M[3 : 0]_CFG registers to the appropriate value (refer again to Table 6).

Table 6. Error Control Bits of the M[3 : 0]_CFG Registers

Bits	Name	Description
5	SBE_EN	When set to 1, this bit enables single-bit memory error correction.
9	EN_ALL_P	When set to 1, this bit enables the capture of all channel packets into the M_ERR[2] and M_ERR[3] registers. When set to 0, this bit disables the capture of all channel packets into the M_ERR[2] and M_ERR[3] registers. In this case, only valid channel requests are captured. Data and idle packets are not captured.

Refresh Reset

Software may reset the memory refresh timing counters. To do this, software writes any value to the M option reset refresh (M[3 : 0]_RESET_REFRESH) registers. Each M option has one M[3 : 0]_RESET_REFRESH register.

Table 7. M[3 : 0]_RESET_REFRESH Register Assignments

Register	Banks
M[0]_RESET_REFRESH	Banks 0 and 4
M[1]_RESET_REFRESH	Banks 1 and 5
M[2]_RESET_REFRESH	Banks 2 and 6
M[3]_RESET_REFRESH	Banks 3 and 7

The write buffer in the microprocessor may merge two, three, or four write commands to M_RESET_REFRESH registers into one operation. When this occurs, synchronized refresh sequencing occurs across four, six, or eight banks of memory, respectively.

Address Compare

Software may signal the support circuitry to compare a software-specified address to the address that the support circuitry is processing and generate an interrupt based on the results of the comparison. To do this, software uses the M option address compare (M[3 : 0]_ADDR_CMP) registers. Table 8 shows the bit format of the M[3 : 0]_ADDR_CMP registers.

Table 8. M[3 : 0]_ADDR_CMP Registers Bit Format

Bits	Name	Description
<5 : 0>	Not applicable	These bits are not used.
<30 : 6>	CMP_ADDR	The support circuitry compares these bits to bits <30 : 6> of a memory or register address that it is processing.
31	MODE	When set to 0, this bit signals the support circuitry to set an interrupt in the M[3 : 0]_ERR0 register when the support circuitry performs a write to a register with an address that matches the CMP_ADDR bits. When set to 1, this bit signals the support circuitry to set an interrupt in the M_ERR0 register when the support circuitry performs any functions with an address that matches the CMP_ADDR bits.
<63 : 32>	Not applicable	These bits are not used.

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